

# NTMS4801N

## MOSFET – Power, N-Channel, SO-8 30 V, 12 A

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- This is a Pb-Free Device

### Applications

- DC-DC Converters
- Synchronous MOSFET
- Printers

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	30	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	9.9	A
		$T_A = 70^{\circ}\text{C}$		7.9	
Power Dissipation $R_{\theta JA}$ (Note 1)		$T_A = 25^{\circ}\text{C}$	$P_D$	1.41	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	$I_D$	7.5	A
		$T_A = 70^{\circ}\text{C}$		6.0	
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^{\circ}\text{C}$	$P_D$	0.8	W
Continuous Drain Current $R_{\theta JA}$ , $t \leq 10$ s (Note 1)		$T_A = 25^{\circ}\text{C}$	$I_D$	12	A
		$T_A = 70^{\circ}\text{C}$		9.6	
Power Dissipation $R_{\theta JA}$ , $t \leq 10$ s (Note 1)		$T_A = 25^{\circ}\text{C}$	$P_D$	2.1	W
Pulsed Drain Current		$T_A = 25^{\circ}\text{C}$ , $t_p = 10 \mu\text{s}$		$I_{DM}$	35
Operating Junction and Storage Temperature			$T_J$ , $T_{stg}$	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	2.1	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^{\circ}\text{C}$ , $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 14$ A <sub>pk</sub> , $L = 1.0$ mH, $R_G = 25 \Omega$ )			$E_{AS}$	98	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

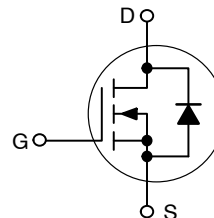


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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	9.0 m $\Omega$ @ 10 V	12 A
	12.5 m $\Omega$ @ 4.5 V	

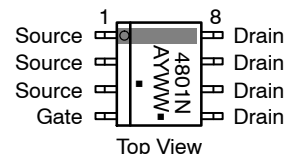
### N-Channel



### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



4801N = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4801NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**THERMAL RESISTANCE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	88.5	°C/W
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	60.5	
Junction-to-Foot (Drain)	$R_{\theta JF}$	23	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	156	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surfaced mounted on FR4 board using 1 in sq pad size.
2. Surfaced mounted on FR4 board using the minimum recommended pad size.

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			7.0		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 85^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

**ON CHARACTERISTICS** (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			6.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		7.0	9.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		9.5	12.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5\text{ V}, I_D = 12\text{ A}$		26		S

**CHARGES, CAPACITANCES AND GATE RESISTANCE**

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		1630	2201	pF
Output Capacitance	$C_{oss}$			288	389	
Reverse Transfer Capacitance	$C_{rss}$			150	225	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 12\text{ A}$		12.2	14	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.8		
Gate-to-Source Charge	$Q_{GS}$			5.1		
Gate-to-Drain Charge	$Q_{GD}$			4.4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 12\text{ A}$		25		nC

**SWITCHING CHARACTERISTICS** (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 6.0\text{ }\Omega$		10.5		ns
Rise Time	$t_r$			3.7		
Turn-Off Delay Time	$t_{d(off)}$			29		
Fall Time	$t_f$			9.8		

**DRAIN-SOURCE DIODE CHARACTERISTICS**

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$	$T_J = 25^\circ\text{C}$		0.73	1.0	V
			$T_J = 125^\circ\text{C}$		0.6		

# NTMS4801N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### DRAIN-SOURCE DIODE CHARACTERISTICS

Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 2.1\text{ A}$		22		ns
Charge Time	$t_a$			11		
Discharge Time	$t_b$			11		
Reverse Recovery Charge	$Q_{RR}$			13		nC

### PACKAGE PARASITIC VALUES

Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.66		nH
Drain Inductance	$L_D$			0.20		nH
Gate Inductance	$L_G$			1.5		nH
Gate Resistance	$R_G$			1.1	1.8	$\Omega$

- Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

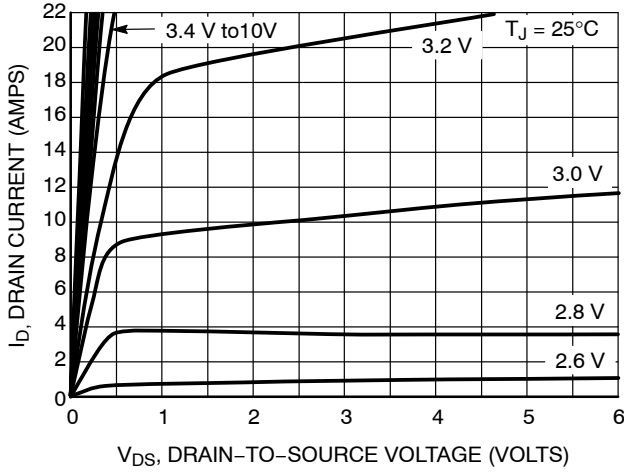


Figure 1. On-Region Characteristics

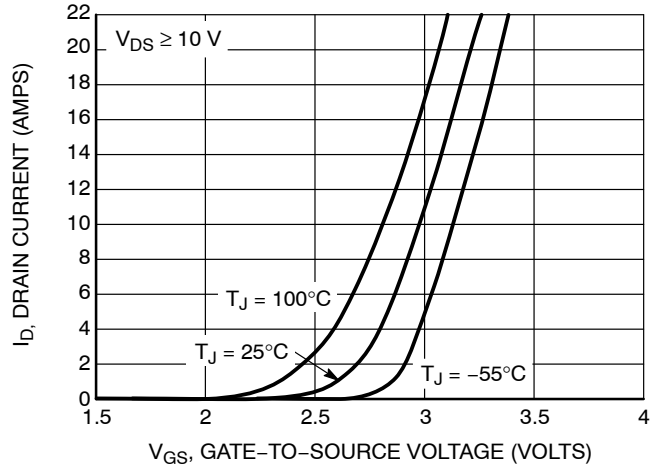


Figure 2. Transfer Characteristics

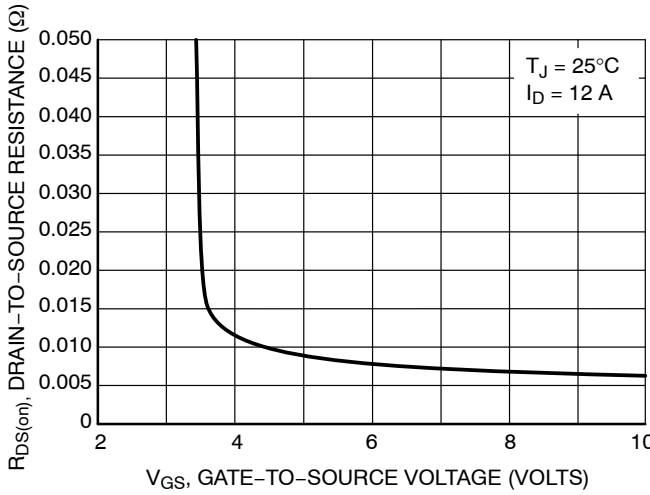


Figure 3. On-Resistance vs. Gate-to-Source Voltage

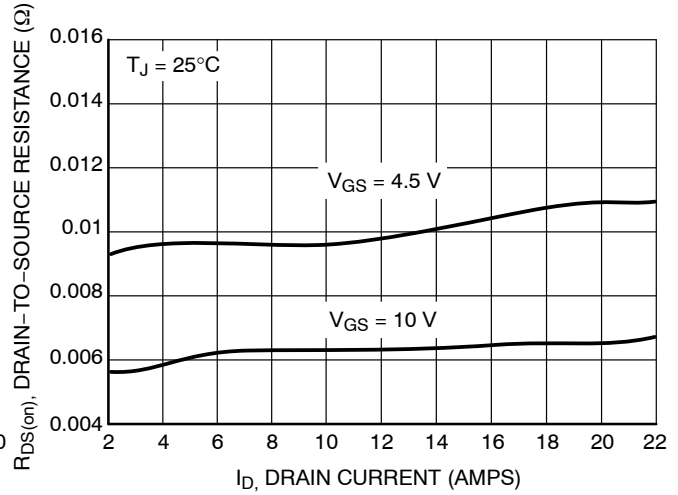


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

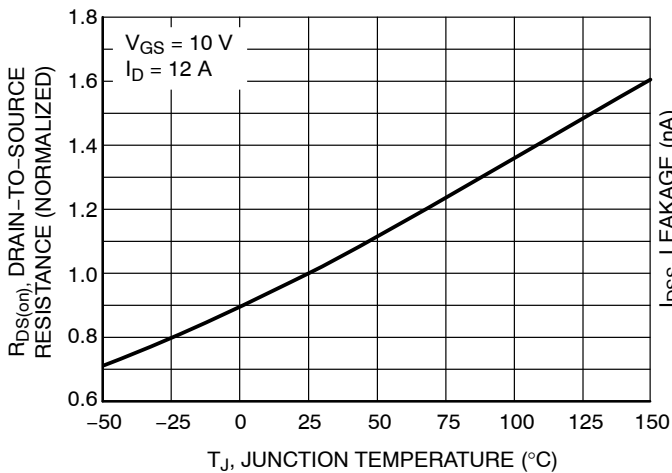


Figure 5. On-Resistance Variation with Temperature

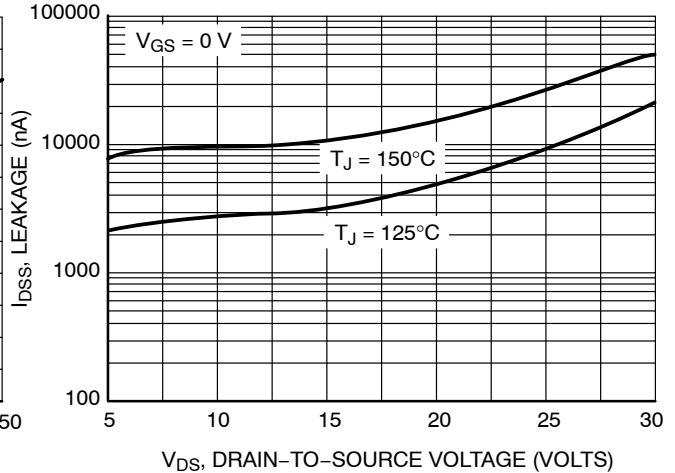


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

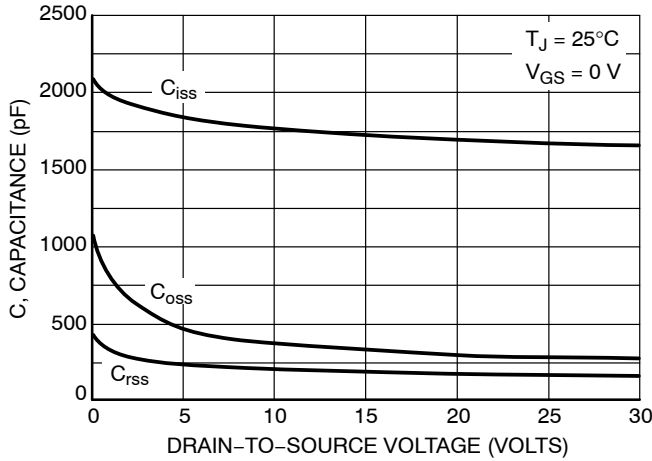


Figure 7. Capacitance Variation

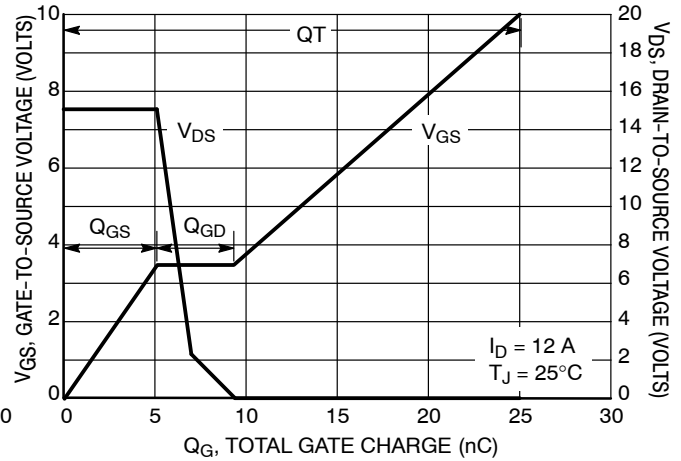


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

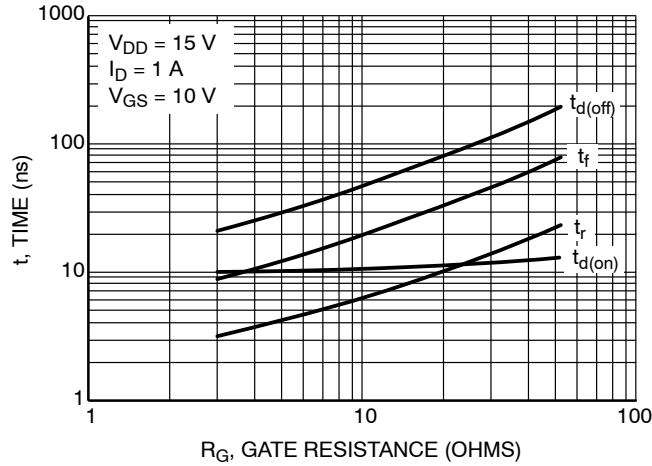


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

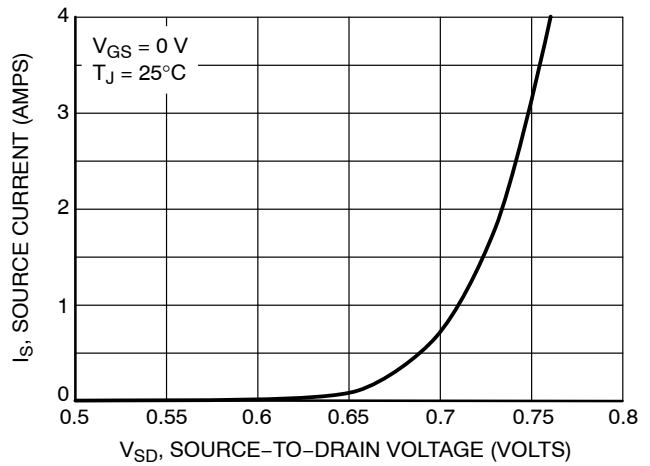


Figure 10. Diode Forward Voltage vs. Current

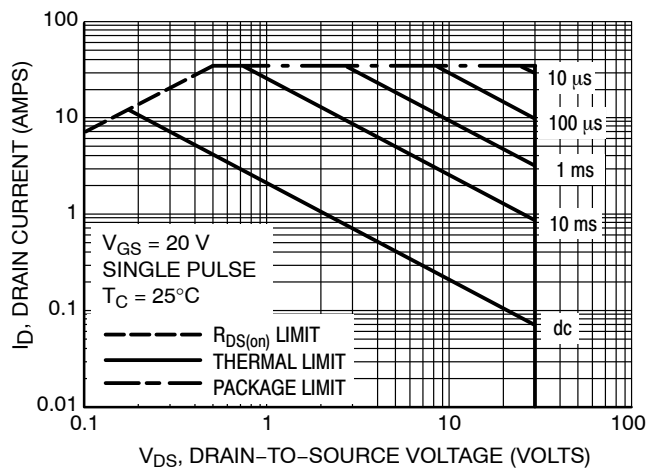


Figure 11. Maximum Rated Forward Biased Safe Operating Area

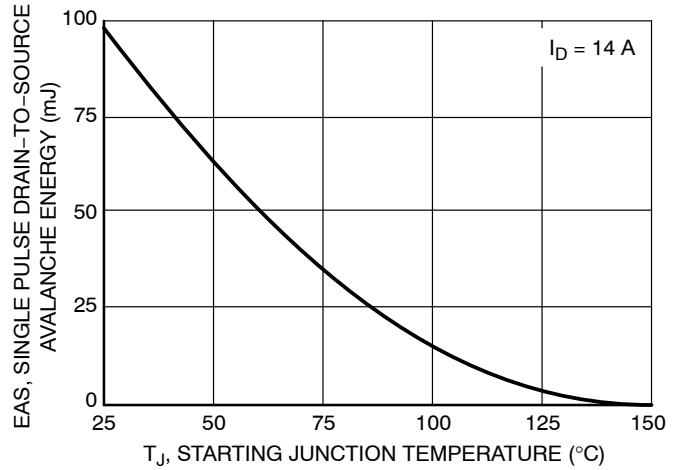


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

<b>STYLE 1:</b> PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	<b>STYLE 2:</b> PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	<b>STYLE 3:</b> PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	<b>STYLE 4:</b> PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
<b>STYLE 5:</b> PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	<b>STYLE 6:</b> PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	<b>STYLE 7:</b> PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	<b>STYLE 8:</b> PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
<b>STYLE 9:</b> PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	<b>STYLE 10:</b> PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	<b>STYLE 11:</b> PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	<b>STYLE 12:</b> PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
<b>STYLE 13:</b> PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	<b>STYLE 14:</b> PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	<b>STYLE 16:</b> PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
<b>STYLE 17:</b> PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	<b>STYLE 18:</b> PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	<b>STYLE 19:</b> PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	<b>STYLE 20:</b> PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
<b>STYLE 21:</b> PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	<b>STYLE 22:</b> PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	<b>STYLE 23:</b> PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	<b>STYLE 24:</b> PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
<b>STYLE 25:</b> PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	<b>STYLE 26:</b> PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	<b>STYLE 27:</b> PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	<b>STYLE 28:</b> PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
<b>STYLE 29:</b> PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	<b>STYLE 30:</b> PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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