TE3-LIU™
Line Interface Unit for DS3, STS1 and E3

PEF 3452 Version 1.3

Wired Communications

Infineon technologies

Never stop thinking.

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PEF 3452
PRELIMINARY

Revision History:	**2001-12-05**	DS1
Previous Version:	Preliminary Data Sheet TE3-LIU V1.2, 2001-07, DS3	

Page	Subjects (major changes since last revision)
24	**Chapter 4.1.4**
27	**Table 10**
28	**Figure 12**

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PRELIMINARY

Preface

The PEF 3452 (TE3-LIU™) is a flexible line interface unit for a wide area of telecommunication and data communication applications. The device is addressed to fulfill all requirements to build a DS3, STS-1 or E3 line interface.

Organization of this Document

This Preliminary Data Sheet is organized as follows:

- **Overview**
  Gives a general description of the product, lists the key features, and presents some typical applications.
- **Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.
- **Functional Description**
  Describes the functional blocks and principle operation modes.
- **Interface Description**
  Describes the device interfaces.
- **Operational Description**
  Shows the operation modes and how their initialization.
- **Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.
- **Package Outlines**
  Shows the mechanical values of the device package.
- **Appendix**
- **Index**

PRELIMINARY

Related Documentation

This document refers to the following international standards
(in alphabetical/numerical order):

ACA TS016 (general requirements for Australia)

CTR-24/TBR-24 (E3 requirements)

ETS 300 166 (E3 transmit return loss)

ITU-T G.703 (E3 pulse mask, B3ZS/HDB3 code, E3 receive return loss)

ITU-T G.751 (jitter requirements E3)

ITU-T G.775 (loss of signal definition)

ITU-T G.823 (jitter requirements E3)

ITU-T G.824 (jitter requirements DS3)

ITU-T O.151 (pseudo random binary sequence (PRBS) definition)

GR-253-CORE (STS-1 jitter requirements)

GR-499-CORE (DS3 pulse mask, DS3 jitter requirements)

ANSI T1.102 (STS-1 pulse mask)

ANSI T1.102 Annex B (DS3 monitoring)

ANSI T1.231 (maintenance functions, defect definitions)

ANSI T1.404 (DS3 pulse mask)

MIL-STD 883D (ESD requirements)

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Please provide in the *subject* of your e-mail:
device name (TE3-LIU™), device number (PEF 3452), device version (Version 1.3),

and in the *body* of your e-mail:
document type (Preliminary Data Sheet), issue date (2001-12-05) and document revision number (DS1).

1 Overview

The TE3-LIU™ PEF 3452 Line Interface Unit is used to connect a DS3/STS-1 or E3 framer device to an analog transmission line. The line interface fulfills the relevant standards for DS3 (44.736 Mbit/s), STS-1 (51.840 Mbit/s) and E3 (34.368 Mbit/s) systems.

The TE3-LIU™ comes in a P-MQFP-44-2 package (SMD) to save a significant amount of board space. The integrated jitter attenuation further reduces overall system complexity and cost.

This CMOS 3.3 V low power device contains an integrated pulse shaper to drive any line length within the range of up to 1100 ft. without the need for external length selection (Line Build Out).

The hardware configuration mode allows low cost systems with flexible device setting without the need for a microprocessor.

An optional microprocessor mode allows the connection to a standard microprocessor bus to control hardware settings.

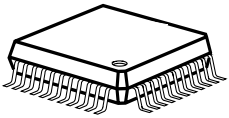
PRELIMINARY

Line Interface Unit for DS3, STS1 and E3 TE3-LIU™

PEF 3452

Version 1.3

1.1 Features



P-MQFP-44-2

- Generic analog interface for all DS3/STS-1/E3 applications
- Single chip solution for receive and transmit direction
- 3.3 V low power device
- Integrated receive equalization network
- Integrated noise and crosstalk filter
- Clock and data recovery using an integrated PLL with ultra-low intrinsic jitter
- Transmit clock duty cycle correction PLL
- No external components required for clock and data recovery and receive equalizer
- DSX receive line monitor (additional 20 dB gain according to ANSI T1.102)
- Low transmitter output impedances for high transmit return loss
- Disable function of the analog transmit line outputs
- Transmit pulse shaper to fulfill requirements of ANSI T1.404, Telcordia GR-499-CORE, ANSI T1.102 and ITU-T G.703 (E3)
- Maximum line length up to 1100 ft. (using standard coaxial cable, for example AT&T 728A, 734A or 734D)
- External line length selection (LBO) is not required
- Jitter specifications of GR-499-CORE and ITU-T G.823 are met
- Integrated jitter attenuation PLL and buffer in transmit direction
- Dual or single rail digital inputs and outputs from/to the framer interface
- Selectable line codes (HDB3 (E3), B3ZS (DS3/STS-1), AMI)
- Analog and digital loss of signal detection and indication
- Automatic RDOP/RDON blanking option in case of LOS
- Bipolar violation indication
- Local loop and remote loop for diagnostic purposes
- Insertion of alarm indication signal ("all ones")
- Flexible hardware or software controlled device configuration
- Device power down function

Type	Package
PEF 3452 H V1.3	P-MQFP-44-2

Hardware Interface Mode

- DS3/STS-1 or E3
- Line Coding (E3: HDB3 or AMI; DS3/STS-1: B3ZS or AMI)
- Transmitter disable
- Power down
- Remote loop
- Local loop
- Single/dual rail operation
- Receive clock edge selection
- Transmit clock edge selection
- Transmit "all ones"
- Receive line monitoring mode
- Automatic RDOP/RDON blanking option
- Jitter attenuation
- Loss of signal indication
- Bipolar violation indication

Microprocessor Interface Mode

- Microprocessor bus compatible interface
- Hardware control lines directly accessible

General

- CMOS device
- P-MQFP-44-2 package (body size 10 mm $\times$ 10 mm, lead pitch 0.8 mm)
- Single power supply: 3.3 V ± 5%
- 5V-tolerant digital input lines
- Temperature range of -40°C to +85°C
- Low power device

Applications

- Interface for SONET/DS3 and E3 network equipment
- WAN gateways
- CSU/DSU
- Multiplexers
- Digital crossconnect systems
- DS3/STS-1/E3 Test Equipment

1.2 Logic Symbol

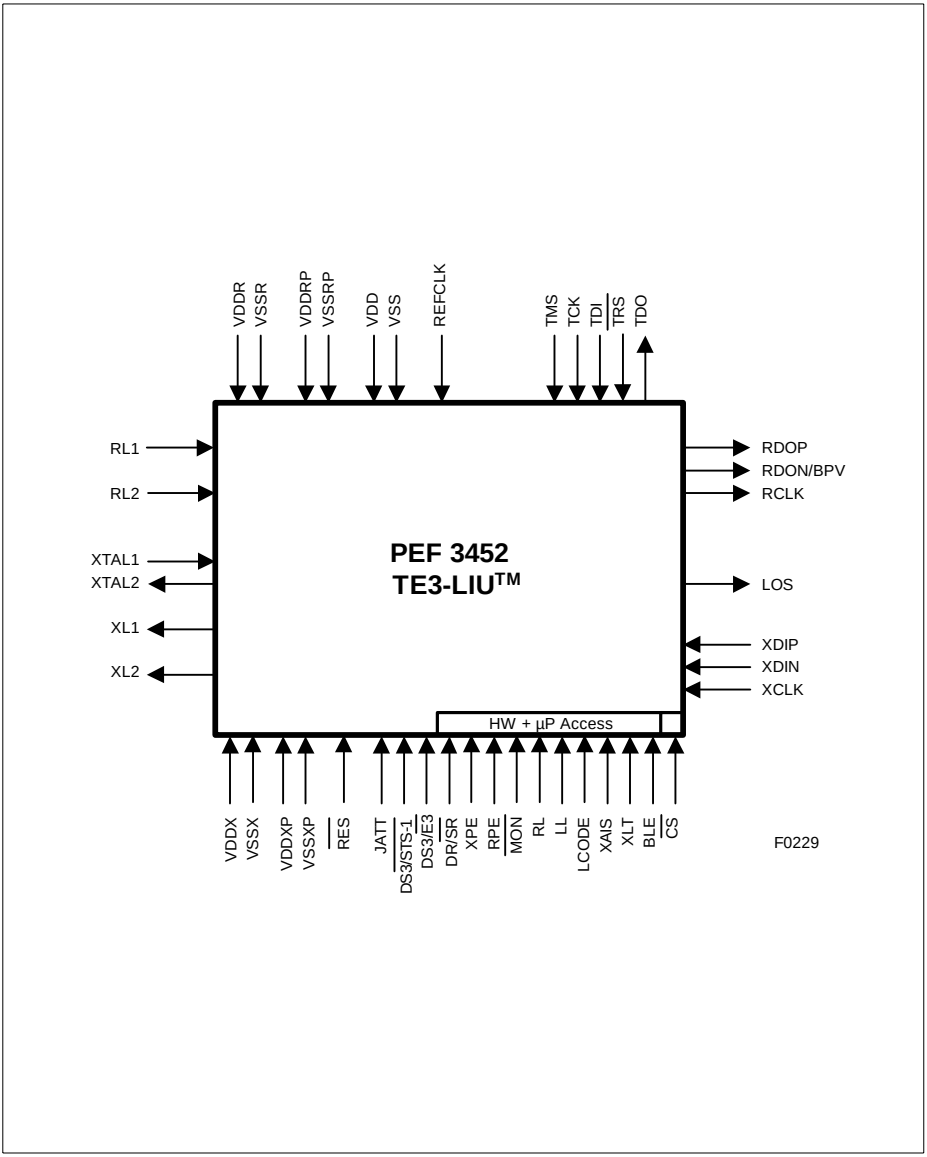


Figure 1 Logic Symbol

1.3 Typical Applications

Figure 2 to **Figure 4** show typical applications using the TE3-LIU™.

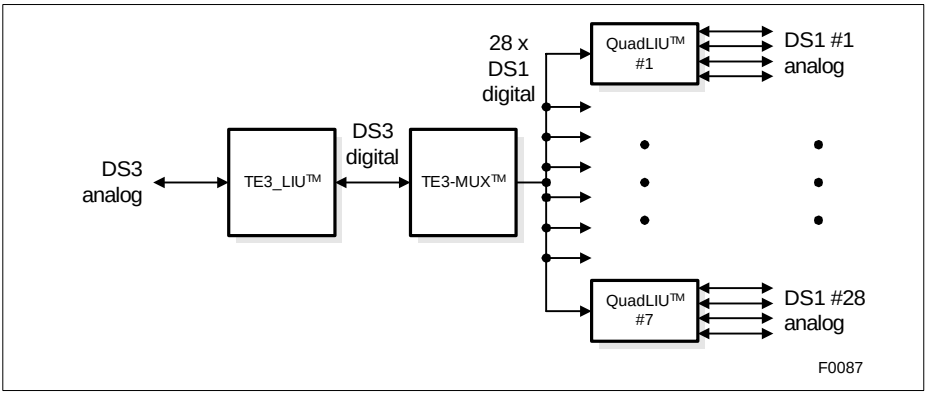


Figure 2 T3/T1 Multiplexer Application

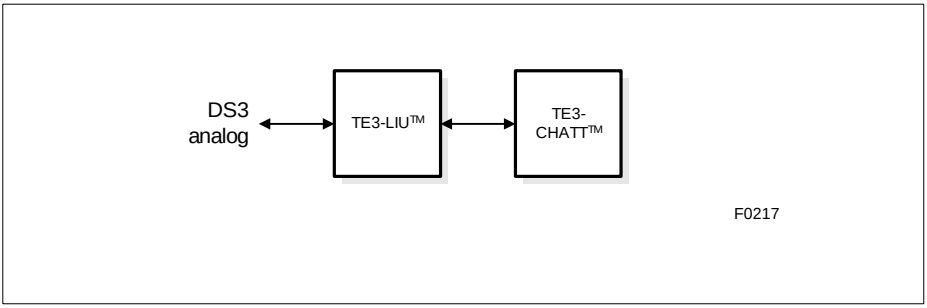


Figure 3 Channelized T3 Link Layer Application

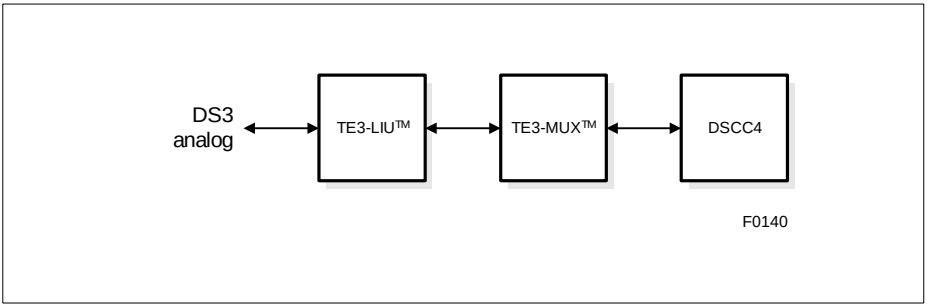


Figure 4 Unchannelized T3 Link Layer Application

*Note: TE3-MUX™ (PEB 3445) is an M13 **MU**ltiple**X**er/demultiplexer with an integrated DS3 framer*

*QuadLIU™ (PEB 22504) is a **4**-channel **L**ine **I**nterface **U**nit for E1/T1/J1*

*DSCC4™ (PEB 20534) is a 4-channel **S**erial **C**ommunication **C**ontroller*

*TE3-CHATT™ (PEB 3456) is a **CHA**nnelized **T**3 **T**ermination with DS3 Framer, M13 Multiplexer, T1/E1 Framers and 256 Channel HDLC/PPP controller*

2 Pin Descriptions

2.1 Pin Diagram

P-MQFP-44-2 (top view)

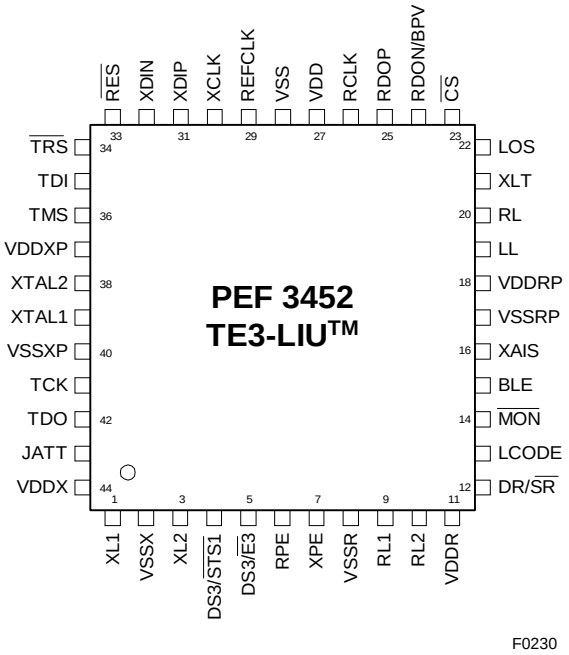


Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Interface Pin Functions

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
		Receive Direction	
9	RL1	I (analog)	**Line Receiver 1** Analog input from the external transformer (receive bipolar ring). The signal at RL1 must be coded according to B3ZS or HDB3.
10	RL2	I (analog)	**Line Receiver 2** Analog input from the external transformer (receive bipolar tip). The signal at RL1 must be coded according to B3ZS or HDB3.
25	RDOP	O	**Receive Data Output/Positive** Received data at RL1/2 is sent on RDOP/ RDON to the framer interface. Data is clocked with the rising or falling edge of RCLK, depending on RPE. In single rail mode (DR/SR=0), data is sent in NRZ format.
24	RDON	O	**Receive Data Output/Negative** If dual rail data format is selected, the negative data signal is output on RDON/ BPV.
	BPV		**Bipolar Violation** If single rail data format is selected, the bipolar violation indication signal is output on RDON/BPV. BPV is synchronized on RCLK.
26	RCLK	O	**Receive Clock** Receive Clock extracted from the incoming data pulses. The active clock edge is determined by RPE. During LOS, a clock signal is generated internally and driven on RCLK (derived from REFCLK).

Table 1 Interface Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
		Transmit Direction	
1	XL1	O (analog)	**Transmit Line 1** (transmit bipolar ring) Analog output to the external transformer. XL1 can be switched into inactive mode.
3	XL2	O (analog)	**Transmit Line 2** (transmit bipolar tip) Analog output to the external transformer. XL2 can be switched into inactive mode.
31	XDIP	I + PU	**Transmit Data In/Positive** Transmit data received from the framer interface to be output on XL1/2. NRZ or dual rail positive data has to be provided at XDIP. Latching of data is done with the rising or falling transitions of XCLK, depending on XPE.
32	XDIN	I + PU	**Transmit Data In/Negative** If dual rail format is selected, negative data signal is read from XDIN. If single rail data format is selected, data on XDIN is ignored. Latching of data is done with the rising or falling transitions of XCLK, depending on XPE.
30	XCLK	I + PU	**Transmit Clock** Input of the working clock for the transmitter. The active clock edge is determined by XPE. DS3: 44.736 MHz STS-1: 51.840 MHz E3: 34.368 MHz To fulfill e.g. ITU-T G.832 a clock accuracy of 20 ppm is required. For correct function a clock signal has always to be supplied to XCLK.

Table 1 Interface Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
		Global Clock Reference	
29	REFCLK	I	**Reference Clock** REFCLK is the basic internal clock. It must be stable during reset and operation. This clock is also used to synchronize the receive PLL in case of no signal. The clock frequency depends on the target application: DS3: 44.736 MHz STS-1: 51.840 MHz E3: 34.368 MHz To fulfill e.g., ITU-T G.832 a clock accuracy of 20 ppm is required.
39	XTAL1	I	**Jitter Attenuation Reference** Connection for an external pullable crystal. DS3: 14.912 MHz STS-1: 17.280 MHz E3: 11.456 MHz If jitter attenuation is disabled (default), XTAL1 is internally driven to a fixed level (not floating).
38	XTAL2	O	

Table 2 Control Pin Functions

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
33	$\overline{\text{RES}}$	I	**Hardware Reset** A low signal at this pin forces the device into reset state.
23	$\overline{\text{CS}}$	I + PU	**Chip Select** 0 = hardware control signals are switched through 1 = hardware control signals are ignored
5	DS3/$\overline{\text{E3}}$	I + PU	**DS3/STS-1 or E3 Select** Primary mode selection. This signal has to be stable during reset and may not change afterwards. It must not be connected to a µP bus. 0 = E3 1 = DS3 or STS-1 (see DS3/$\overline{\text{STS-1}}$)
4	DS3/$\overline{\text{STS-1}}$	I + PU	**DS3 or STS-1 Select** Primary mode selection. This signal has to be stable during reset and may not change afterwards. It must not be connected to a µP bus. 0 = STS-1 1 = DS3
13	LCODE	I + PU	**Line Code Select** for receive and transmit direction E3: 0 = AMI 1 = HDB3 DS3/STS-1: 0 = AMI 1 = B3ZS
16	XAIS	I + PU	**Transmit Alarm Indication** 0 = no AIS 1 = AIS all-ones insertion

Table 2 Control Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
20	RL	I + PU	**Remote Loop Switching** 0 = no loop 1 = Remote Loop[1)]
19	LL	I + PU	**Local Loop Switching** 0 = no loop 1 = Local Loop[1)]
21	XLT	I + PU	**Transmitter inactive** 0 = transmitter enabled 1 = transmitter disabled (outputs 1.5 V common mode voltage)
14	$\overline{\text{MON}}$	I + PU	**Line Monitoring Mode** 0 = additional 20 dB gain at RL1/RL2 1 = normal
15	BLE	I + PU	**Blanking Enable** 0 = detected signal is switched through even in case of LOS 1 = all-zero signal is sent on RDOP/RDON in case of LOS, REFCLK is used to drive RCLK
12	DR/$\overline{\text{SR}}$	I + PU	**Dual Rail/Single Rail Select** The framer interface is operated either in dual rail or single rail mode. In single rail mode, the BPV signal is output on RDON/ BPV and input on XDIN is ignored. 0 = single rail 1 = dual rail
6	RPE	I + PU	**RCLK Positive Edge Selection** 0 = RDOP, RDON are clocked with negative (falling) edge of RCLK 1 = RDOP, RDON are clocked with positive (rising) edge of RCLK
7	XPE	I + PU	**XCLK Positive Edge Selection** 0 = XDIP, XDIN are clocked with negative (falling) edge of XCLK 1 = XDIP, XDIN are clocked with positive (rising) edge of XCLK

Table 2 Control Pin Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
43	JATT	I + PD	**Jitter Attenuation Enable** This signal has to be stable during reset and may not change afterwards. It must not be connected to a µP bus. 0 = no jitter attenuation (default if left open) 1 = jitter attenuation in transmit direction
22	LOS	O	**Loss of Signal Indication** 0 = correct signal 1 = loss of signal LOS is synchronized on RCLK. During LOS, a clock signal is generated internally and driven on RCLK.

1) If RL=LL=1, the device is set into power down mode.

Table 3 Power Supply Pins

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
11	V_{DDR}	S (analog)	**Positive Power Supply** for the analog receiver
8	V_{SSR}	S (analog)	**Power Supply Ground** for the analog receiver
44	V_{DDX}	S (analog)	**Positive Power Supply** for the analog transmitter
2	V_{SSX}	S (analog)	**Power Supply Ground** for the analog transmitter
18	V_{DDRP}	S (analog)	**Positive Power Supply** for the analog receiver PLL
17	V_{SSRP}	S (analog)	**Power Supply Ground** for the analog receiver PLL
37	V_{DDXP}	S (analog)	**Positive Power Supply** for the analog transmitter PLL
40	V_{SSXP}	S (analog)	**Power Supply Ground** for the analog transmitter PLL
27	V_{DD}	S	**Positive Power Supply** for digital subcircuits and the digital receiver output
28	V_{SS}	S	**Power Supply Ground** for digital subcircuits and the digital receiver output

Table 4 Test Pins[1)]

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
34	$\overline{\text{TRS}}$	I + PU	**TAP Controller Reset** Active low test controller reset; this pin must be connected to $\overline{\text{RST}}$ or V_{SS}
35	TDI	I + PU	**Test Data Input**
36	TMS	I + PU	**Test Mode Select**
41	TCK	I + PU	**Test Clock**
42	TDO	O	**Test Data Output**

1) These pins are used for factory test only; boundary scan mode is not provided.

Note: PU = input or input/output comprising an internal pullup device
PD = input or input/output comprising an internal pulldown device

To override the internal pullup (pulldown) by an external pulldown (pullup), a resistor value of 47 kΩ is recommended.

Unused pins containing pullups or pulldowns can be left open.

3 Functional Description

3.1 Functional Overview

The TE3-LIU™ device contains analog and digital functional blocks, which are configured and controlled by direct hardware or microprocessor control.

The main interfaces are

- Receive Line Interface
- Transmit Line Interface
- Framer Interface
- Hardware Interface

The main internal functional blocks are

- Analog line receiver with noise & crosstalk filter, equalizer network and clock/data recovery
- Analog line driver with programmable pulse shaper
- Central clock generation module
- Jitter attenuator
- Maintenance functions (e.g., loop switching local or remote)
- Hardware/microprocessor control interface

3.2 Block Diagram

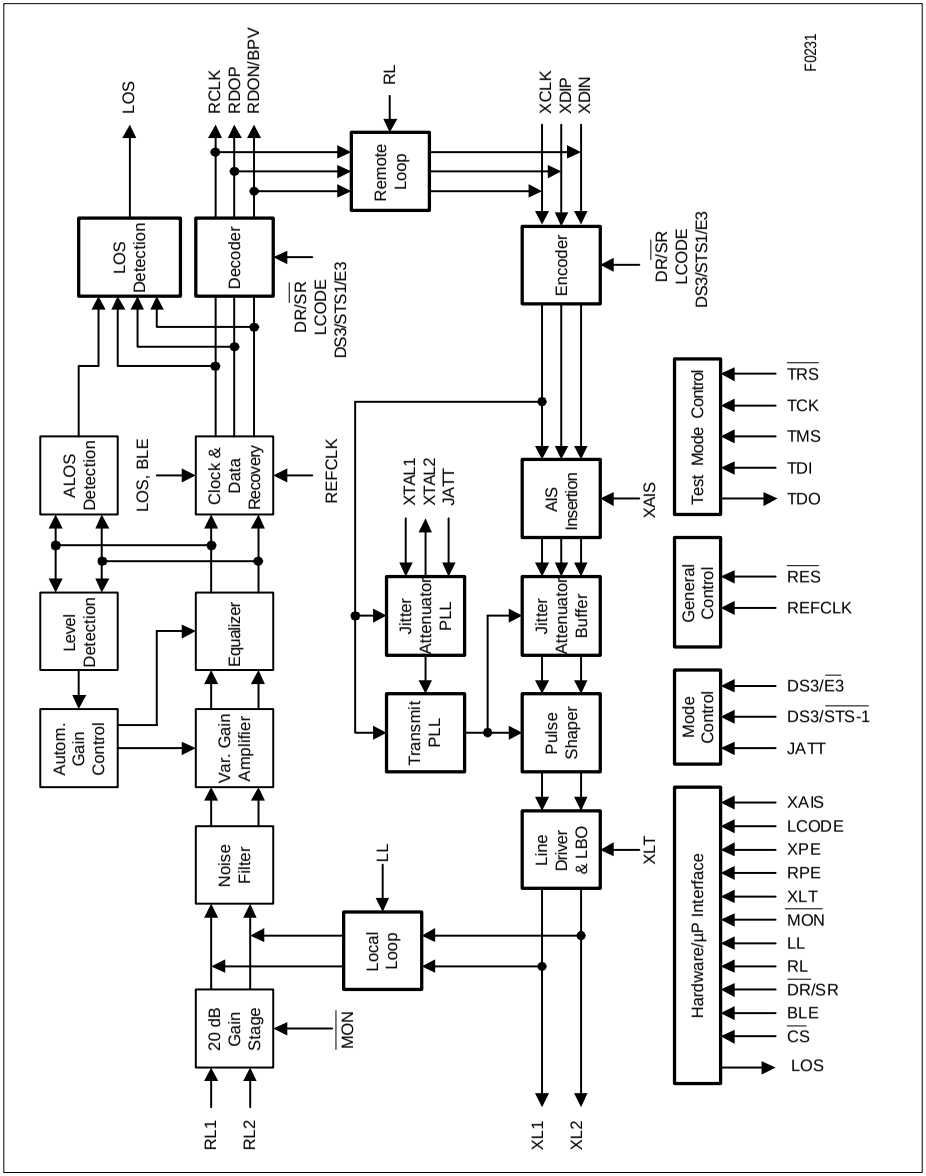


Figure 6 Block Diagram

3.3 Functional Blocks

3.3.1 Hardware Control Unit

All hardware control signals except DS3/$\overline{E3}$, DS3/$\overline{STS\text{-}1}$ and JATT are gated by $\overline{CS}$. All other control signals are gated by $\overline{CS}$ to allow an easy connection to a microprocessor (µP) data bus. DS3/$\overline{E3}$, DS3/$\overline{STS\text{-}1}$ and JATT may not be connected to a data bus. If direct hardware control without µP is intended, $\overline{CS}$ has to be connected to V_{SS}.

After reset all control input values are cleared. The default control values (driven by internal pullups) are activated after $\overline{CS}$ = low is applied for the first time after reset.

Table 5 Hardware Control Functions

Device Function	Control Signal
Selection of E3 or DS3/STS-1 mode[1)]	DS3/$\overline{E3}$ 0 = E3 1 = DS3 or STS-1[2)]
Selection of DS3 or STS-1 mode[1)]	DS3/$\overline{STS\text{-}1}$ 0 = STS-1 1 = DS3[2)] This pin is ignored, if E3 mode is selected by DS3/$\overline{E3}$ = 0
Dual rail select	DR/$\overline{SR}$ 0 = single rail data on RDOP and XDIP 1 = dual rail data on RDOP/RDON and XDIP/XDIN[2)]
Receive clock edge selection	RPE 0 = data change on negative edge 1 = data change on positive edge[2)]
Transmit clock edge selection	XPE 0 = data change on negative edge 1 = data change on positive edge[2)]
Selection of line coding	LCODE 0 = AMI 1 = HDB3 (E3)[2)] 1 = B3ZS (DS3/STS-1)[2)]
Send AIS (all-ones alarm indication signal)	XAIS 0 = no insertion 1 = AIS insertion[2)]

Table 5 Hardware Control Functions (cont'd)

Device Function	Control Signal
Select remote loop	RL 0 = normal operation 1 = remote loop
Select local loop	LL 0 = normal operation 1 = local loop
Select power down mode	LL & RL 00 = normal operation 01 = remote loop operation 10 = local loop operation 11 = power down[2)]
Blanking enable	BLE 0 = data signal is switched through even in case of LOS 1 = all-zero signal is transmitted on RDOP/RDON in case of LOS using RCLK derived from REFCLK[2)]
Line monitoring mode	$\overline{\text{MON}}$ 0 = additional 20 dB gain stage activated 1 = normal amplifier setting[2)]
Transmitter inactive mode	XLT 0 = normal operation 1 = inactive[2)3)4)]
Jitter attenuation enable	JATT 0 = jitter attenuation disabled[2)] 1 = jitter attenuation enabled

1) to be selected while reset is active ($\overline{\text{RST}}$ = 0)

2) default, if pin is left open and $\overline{\text{CS}}$ has been asserted at least once

3) outputs 1.5 V common mode voltage

4) connecting of $\overline{\text{CS}}$ to VSS or asserting $\overline{\text{CS}}$ in parallel to $\overline{\text{RES}}$ suppresses spurious output on XL1/2

Table 6 Hardware Indication Signals

Device Function	Indication Signal
Indicate LOS (loss of signal)	LOS 0 = normal signal 1 = loss of signal
Indicate BPV (bipolar violation)	BPV 0 = no violation 1 = bipolar violation Available in single rail mode only on pin RDON/BPV.

4 Interface Description

4.1 Receiver

4.1.1 Standard Receiver Application

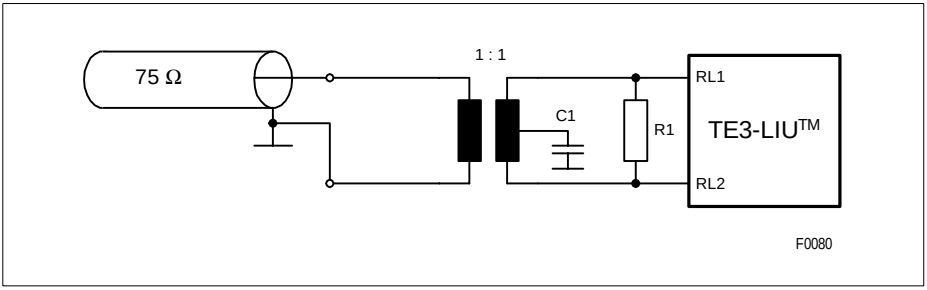


Figure 7 Receiver Configuration

Table 7 External Component Values for Receiver

Parameter	Characteristic Line Impedance [Ω]		
	DS3	STS-1	E3
	75		
R_1 (± 1 %) [Ω]	75		
C_1 (± 20 %) [nF]	100		
$t_2 : t_1$	1 : 1		

The external components are the same for DS3, STS-1 and E3 applications.

4.1.2 Line Monitoring Application

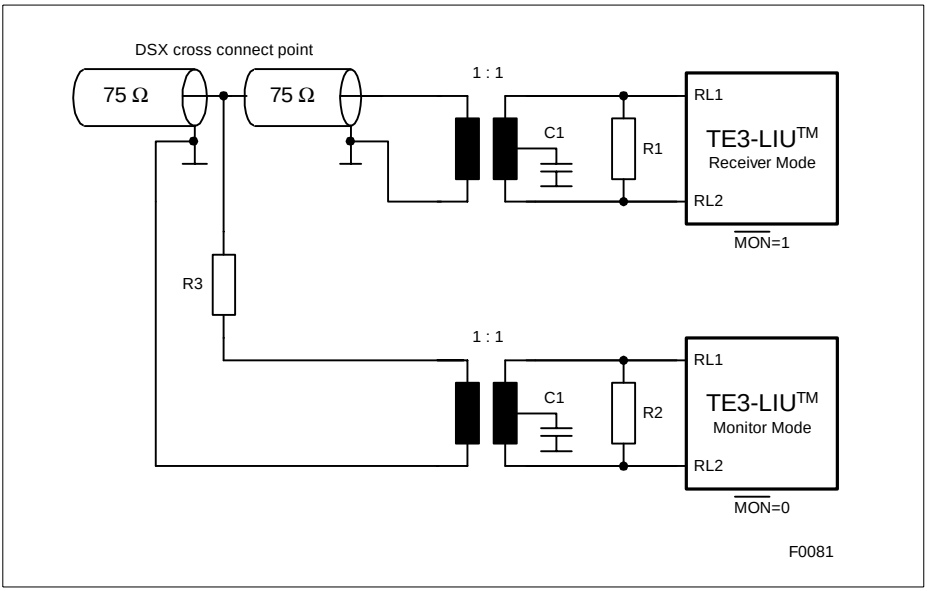


Figure 8 DS3 Line Monitoring

Table 8 External Component Values for DS Line Monitoring

Parameter	Values
R_1 (± 1 %) [Ω]	75
R_2 (± 1 %) [Ω]	47
R_3 (± 1 %) [Ω]	470
C_1 (± 20 %) [nF]	100
$t_2 : t_1$	1 : 1

The external components are according to ANSI T1.102 Annex B. The dimensions given above lead to a signal level at the monitor device input of approximately -20 dB below the level at the receiver device.

Similar configurations using the line monitoring mode are possible in STS-1 or E3 applications.

4.1.3 Receive Line Interface

The receive line interface consists of a pre-amplifier, a noise and crosstalk filter, a variable gain amplifier and an equalizer followed by the clock and data recovery.

The noise and crosstalk filter reduces distortions within the incoming analog signal. The VGA amplifies the analog signal and the equalizer compensates the frequency dependent line attenuation. Digital signal levels are formed within the retiming block of the clock and data recovery.

Receive return loss requirements of ITU-T G.703 are fulfilled as required for E3 operation.

Table 9 E3 Receive Return Loss

Frequency Range		Return Loss
from [kHz]	to [kHz]	[dB]
860	1720	12
1720	34368	18
34368	51550	14

The equalizer contains an additional 20 dB gain stage, which is used in line monitoring mode to amplify resistively attenuated signals.

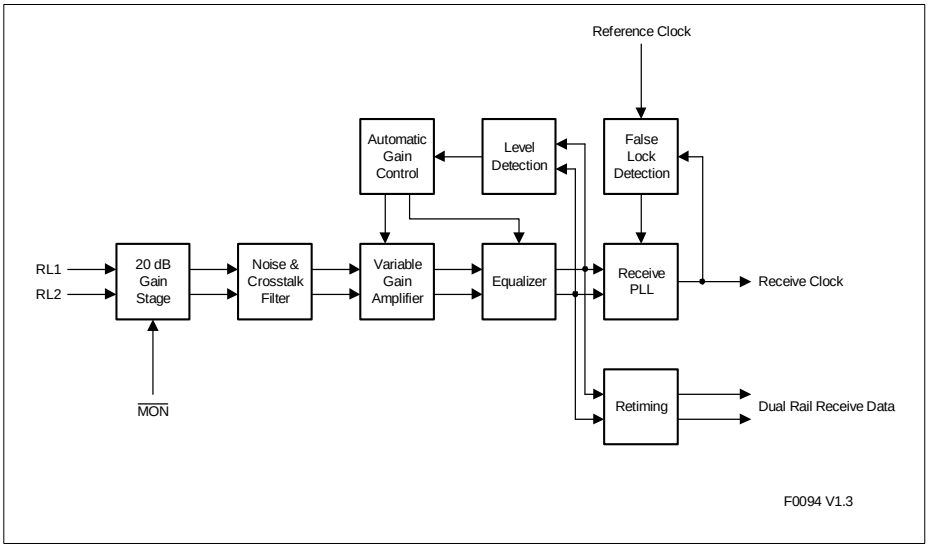


Figure 9 Receive Clock System

4.1.4 Receive Clock and Data Recovery

The receive clock and data recovery extracts the route clock RCLK from the digital data stream and converts the data stream into a dual rail bit stream. The clock and data recovery needs a reference clock to keep the PLL stable during times without data signal at RL1/RL2. The clock that is output on pin RCLK is the recovered clock of the signal provided on RL1/RL2 and has a duty cycle close to 50 %. The intrinsic jitter generated in the absence of any input jitter is defined in **Chapter 4.1.8**. The PLL reference clock is generated internally without the need for external components.

4.1.5 Receive Line Coding

In E3 applications the HDB3 and the AMI coding is provided for the data received from the ternary interface. In DS3/STS-1 mode the B3ZS and AMI code is supported. In B3ZS or AMI code all code violations are detected and indicated.

4.1.5.1 AMI Code

The AMI code is defined as a dual rail data signal, where the combinations 00 ("0"), 10 ("+1") and 01 ("-1") are valid. No subsequent "+1" or "-1" bits are allowed, these will be detected as bipolar violations and indicated on pin RDON/BPV, if single rail mode is selected (according to ANSI T1.231 chapter 7.1).

The received AMI data stream is either switched transparently to the framer interface as dual rail data or converted into a single rail data stream.

4.1.5.2 B3ZS Code

In the B3ZS line code each block of three consecutive zeros is replaced by either of two replacements codes which are B0V and 00V, where B represents a pulse which applies to the bipolar rule ("+1" or "-1") and V represents a bipolar violation (two consecutive "+1" or "-1" bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

The receive line decoder decodes the incoming B3ZS data signal and changes the replacement patterns to the original three-zeros pattern. Pattern sequences violation these rules are reported as bipolar violation errors.

Data output to the framer interface can be selected to be either dual rail or single rail.

4.1.5.3 HDB3 Code

In the HDB3 line code each block of four consecutive zeros is replaced by either of two replacements codes which are B00V and 000V, where B represents a pulse which applies to the bipolar rule ("+1" or "-1") and V represents a bipolar violation (two consecutive "+1" or "-1" bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

The receive line decoder decodes the incoming HDB3 data signal and changes the replacement patterns to the original three-zeros pattern. Pattern sequences violation these rules are reported as bipolar violation errors.

Data output to the framer interface can be selected to be either dual rail or single rail.

4.1.6 Alarm Handling

The receive line interface includes the alarm detection for loss of signal (LOS). LOS is indicated either if an analog or a digital loss of signal condition is detected.

During LOS a clock signal is sent on RCLK. The clock is internally derived from REFCLK.

4.1.6.1 DS3 LOS Definition

Detection and recovery of digital LOS defects in DS3 mode is done according to ANSI T1.231:

An LOS defect occurs when 175 contiguous pulse positions with no pulses of either positive or negative polarity at the line interface are detected. An LOS defect is terminated upon detecting an average pulse density of at least 33% over a period of 175 contiguous pulse positions following the receipt of a pulse. An LOS defect shall not be terminated if, at the end of the pulse-position interval, any subintervals of 100 pulse positions contain no pulses of either polarity.

4.1.6.2 STS-1 LOS Definition

Detection and recovery of digital LOS defects in STS-1 mode is defined in ANSI T1.231 (chapter 8.1.2.1.1) as follows:

An LOS defect occurs upon detection of no transitions on the incoming signal (before descrambling) for time T, where $2.3 \leq T \leq 100$ µs.

The LOS defect is terminated after a time period equal to the greater of 125 µs or $2.5 \times T'$ containing no transition-free interval of length T', where $2.3 \leq T' \leq 100$ µs.

4.1.6.3 E3 LOS Definition

Analog LOS is detected, if the signal level on pins RL1/2 drops below a fixed level ("B") for a certain period. Loss of signal level "B" is defined to be between 15 and 35 dB below normal signal level "A". If the signal exceeds 35 dB for 175 contiguous pulse periods, analog LOS defect is indicated.

Analog LOS defect is cleared, if the signal exceeds a threshold of 15 dB below nominal level for 175 contiguous pulse periods ($10 \leq N \leq 255$). See ITU-T G.775 for reference.

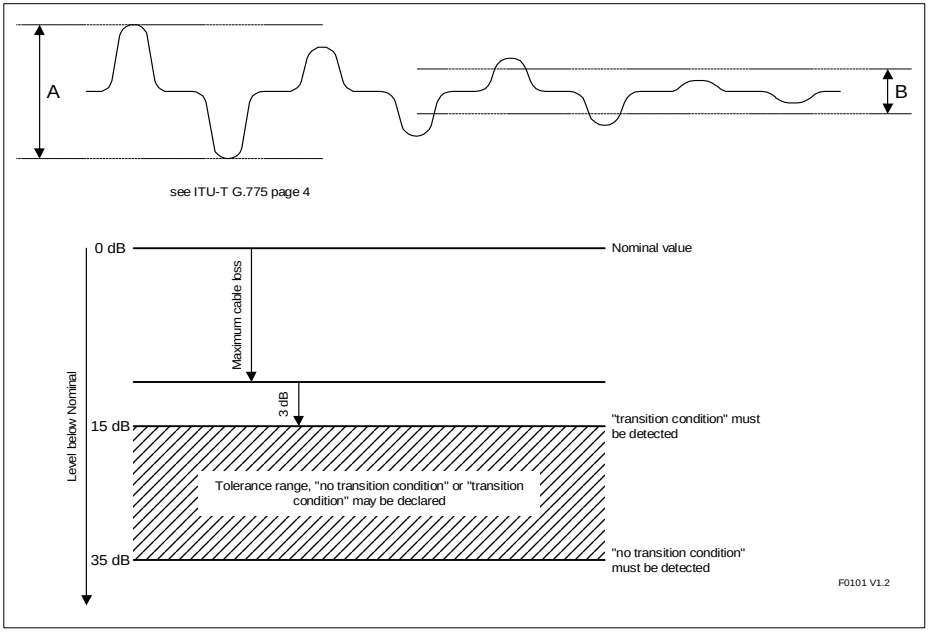


Figure 10 E3 Loss of Signal Definition

4.1.7 Jitter Tolerance

The TE3-LIU™ receiver's tolerance to input jitter complies to and exceeds the relevant international standards. Especially the requirements of Telcordia GR-499-CORE (DS3), ITU-T G.824 (DS3), GR-253-CORE (STS-1) and ITU-T G.823 (E3) are fulfilled and exceeded. **Figure 11** and **Table 10** show the different input jitter specifications. Low frequency jitter is called "wander", where the defined border between jitter and wander is 10 Hz for DS3/E3 and 100 Hz for STS-1.

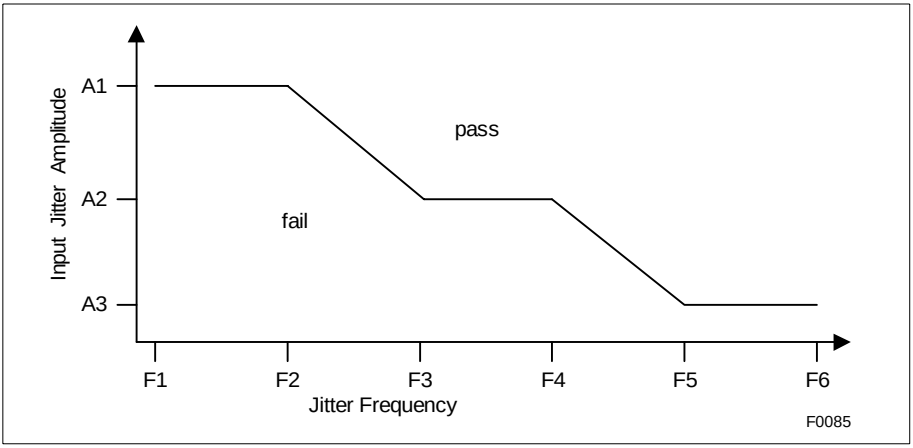


Figure 11 Jitter Tolerance Principle

Table 10 Input Jitter Requirements

Reference	A1	A2	A3	F1	F2	F3	F4	F5	F6
	[UI_{PP}]			[Hz]					
GR-499-CORE, Category I	5	0.1	not def.	10	2300	60×10^3	300×10^3	not def.	not def.
GR-499-CORE, Category II	10	0.3	not def.	10	669	22.3×10^3	300×10^3	not def.	not def.
GR-253-CORE, Category II	15	1.5	0.15	10	30	300	2×10^3	20×10^3	not def.
ITU-T G.823 & ETSI TBR24	1.5	0.15	not def.	100	1000	10×10^3	800×10^3	not def.	not def.
ITU-T G.824	18 µs	5	0.1	not def.	1.2×10^{-5}	10	600	30×10^3	400×10^3

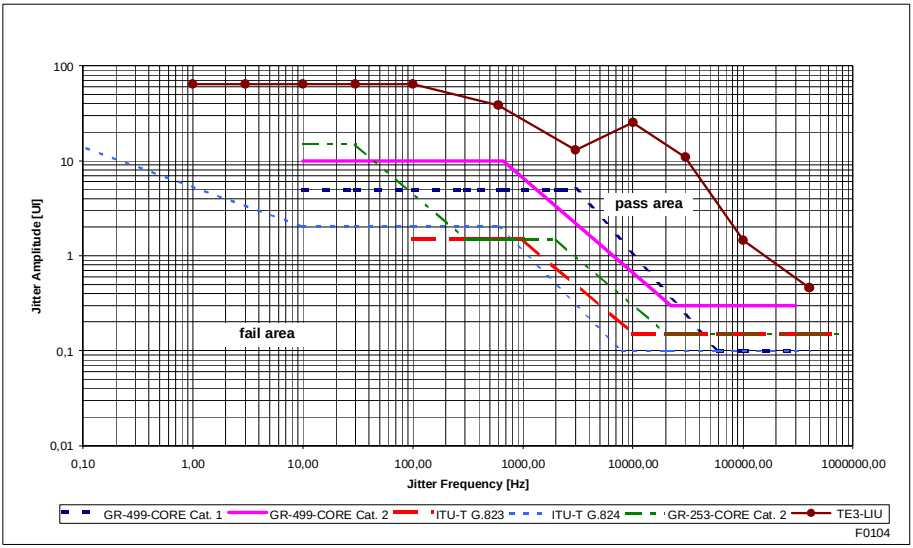


Figure 12 Jitter Tolerance

GR-499-CORE Jitter Tolerance Requirements (DS3)

The input jitter tolerance is defined as the minimum amplitude of sinusodial jitter at a given frequency that when modulating the signal at an equipment input port results in more than 2 errored seconds in a 30-second measurement interval. Requirements on input jitter tolerances are then given in terms of a jitter tolerance mask, which represents the minimum acceptable jitter tolerances for a specified range of jitter frequencies.

There are two different jitter tolerance masks defined for Category I (SONET interfaces) and Category II (non-SONET interfaces) equipment.

GR-253-CORE Jitter Tolerance Requirements (STS-1)

For Category I interfaces, the same requirements are used as defined in GR-499-CORE. For Category II interfaces that are specified as having reduced jitter tolerance, shall tolerate, as a minimum, input jitter applied according to the mask given in **Table 10**.

4.1.8 Receive Output Jitter

The intrinsic jitter of the receiver output signal RDOP/RDON/RCLK (if no input jitter is applied) is

- E3: < 0.06 UI
- DS3: < 0.08 UI
- STS-1: < 0.10 UI

4.2 Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- generation of AMI, B3ZS (DS3/STS-1) or HDB3 (E3) coded signals
- all-ones generation (alarm indication signal)

4.2.1 Transmit Line Interface

The received data stream on pins XDIP (single rail data) or XDIP/XDIN (dual rail data) is converted into a ternary signal which is output on pins XL1 and XL2. In E3 mode the HDB3 and AMI line code are supported, in DS3/STS-1 mode the B3ZS and AMI is supported.

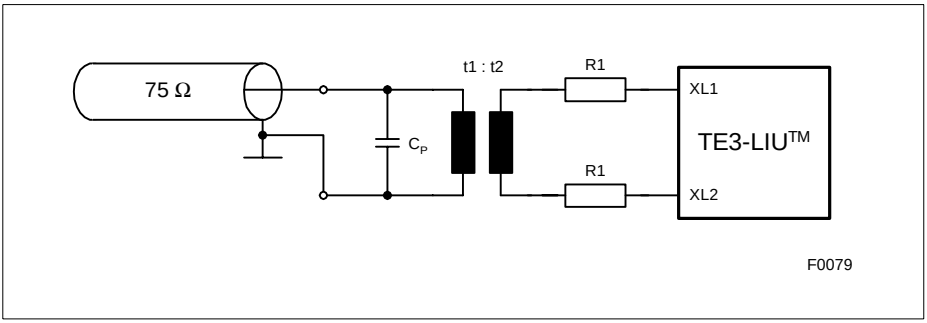


Figure 13 Transmitter Configuration

Table 11 External Component Values for Transmitter

Parameter	Characteristic Line Impedance [Ω]		
	DS3	STS-1	E3
	75		
R_1 (± 1 %) [Ω]	37.5[1)]		
C_p [pF]	37[2)]		
$t_2 : t_1$	1 : 1		

1) This value refers to an ideal transformer without any parasitics. Any transformer resistance or other parasitic resistances have to be taken into account when calculating the final value for the output serial resistors.

2) This value includes all parasitic capacitances on the secondary side of the transformer.

The external components are the same for DS3, STS-1 and E3 applications. Transmit return loss requirements for E3 defined in ETS 300 166 are fulfilled. Pulse mask

requirements according to ANSI T1.102 (at cross connect point, up to 450 ft.) are fulfilled.

Note: An additional capacitor on the primary or secondary side of the transformer may be required in some applications to improve the pulse mask, if the parasitic capacitances of the PCB are very small.

Table 12 E3 Transmit Return Loss

Frequency Range		Return Loss[1)]
from [kHz]	to [kHz]	[dB]
860	1720	6
1720	51550	8

1) measured with an unframed PRBS 2^{15}-1 pattern

4.2.2 Transmit Clock System

The supplied transmit clock XCLK is duty-cycle corrected by an internal PLL circuit to provide a 50% clock signal to the internal line driver unit. The pulse shaper working frequency is fourfold of the XCLK frequency.

If the transmit clock XCLK is failing, an all-zero signal is generated automatically.

If AIS insertion is selected, the output signal is referenced to REFCLK.

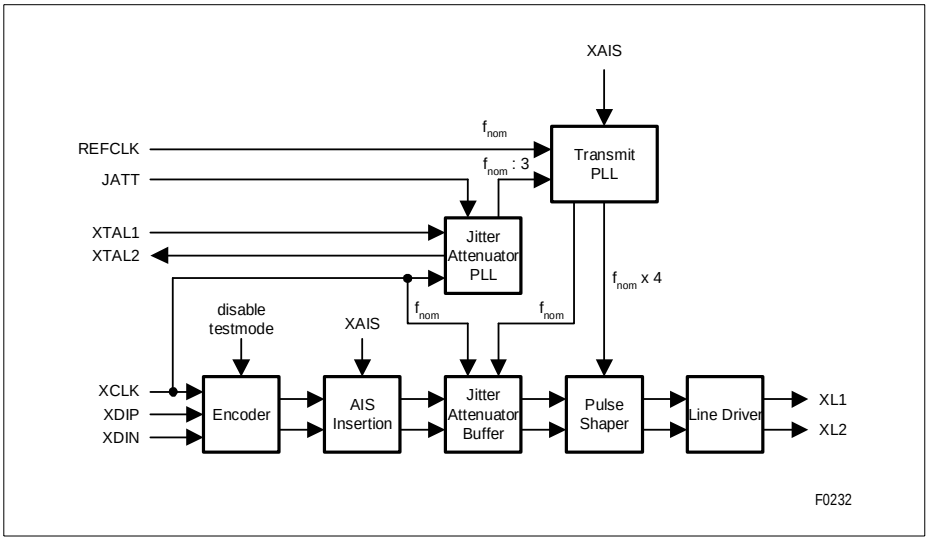


Figure 14 Transmit Clock System

4.2.3 Jitter Attenuation

Jitter is reduced in transmit direction, if the jitter attenuator is activated (JATT = 1). The JATT control signal enables/disables the jitter attenuation PLL and activates/bypasses the buffer.

The jitter attenuator consists of a buffer and a PLL. The jitter attenuation PLL delivers a "jitter free" clock (nominal frequency divided by 3, see **Table 13**) to the transmit PLL which generates the buffer read clock. The jitter attenuation PLL uses a pullable crystal and supports a tuning range of ± 150 ppm.

The jitter attenuator uses a 64-bit dual rail buffer and fulfills the requirements of GR-499-CORE and GR-253-CORE as shown in **Figure 15**. This covers the requirements of ITU-T G.751, G.752 and G.755 as well.

To avoid the need for a high frequency crystal, the reference clock for the jitter attenuation PLL is only one third of the nominal frequency. A detailed block diagram of the transmit clocking is given in **Figure 14**.

Table 13 Jitter Attenuation PLL Operation Frequencies

Operation mode	Jitter Attenuation PLL Input Frequency	Jitter Attenuation PLL Output Frequency	Crystal Frequency
DS3	44.736 MHz	14.912 MHz	14.912 MHz
STS-1	51.840 MHz	17.280 MHz	17.280 MHz
E3	34.368 MHz	11.456 MHz	11.456 MHz

Further requirements for the external crystal are found in **Table 21** on **page 45**.

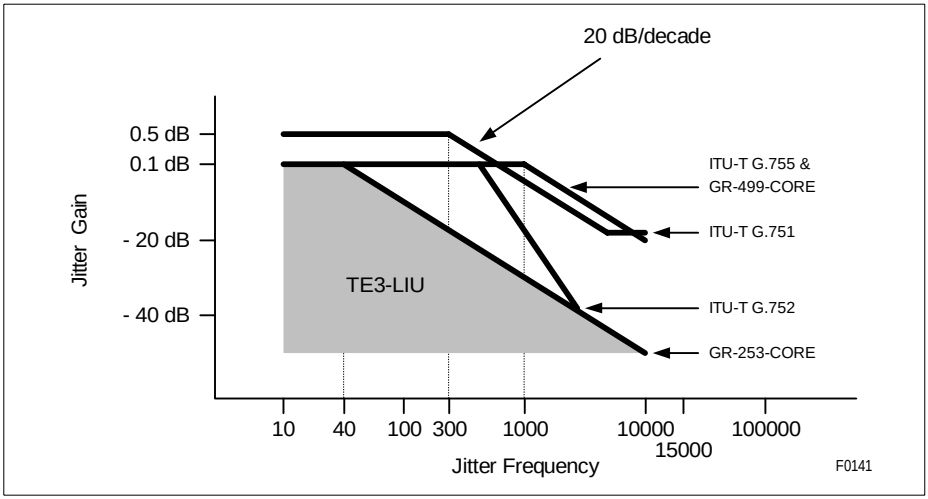


Figure 15 Jitter Attenuation Characteristic

4.2.4 Intrinsic Jitter

The TE3-LIU™ transmit PLL generates an output jitter which fulfills the requirements as specified in **Table 14** below.

Table 14 Transmit Output Jitter

Specification	Measurement Filter Bandwidth		Output Jitter[1)]
	Lower Cutoff	Upper Cutoff	
GR-499-CORE (DS3)	10 Hz	300 kHz	< 1.0 UI_{PP}
			< 0.3 UI_{rms}
ANSI T1.404 (DS3)	10 Hz	400 kHz	< 0.5 UI_{PP}
	30 kHz	400 kHz	< 0.05 UI_{PP}
GR-253-CORE (STS-1)	12 kHz	400 kHz	< 1.0 UI_{PP}
			< 0.3 UI_{rms}
ETSI TBR24 (E3)	100 Hz	800 kHz	< 0.4 UI_{PP}
	10 kHz	800 kHz	< 0.15 UI_{PP}

1) Measured with maximum input jitter applied (see **Figure 12**).

4.2.5 Pulse Shaper

The internal pulse shaper generates the required pulse shapes for E3, DS3 and STS-1 signals according to ANSI T1.102, T1.404, Telcordia GR-499-CORE and ITU-T G.703).

The specific pulse mask is fulfilled at the crossconnect point at a distance of 0 to 450 ft. to the transmitter (DS3 requirement).

The maximum line length between a TE3-LIU™ transmitter and TE3-LIU™ receiver is 1100 ft. for a coaxial cable of AT&T type 728A, 734A or 734D.

4.2.6 Transmit Line Coding

4.2.6.1 AMI Code

The AMI code is defined as a dual rail data signal, where the combinations 00 ("0"), 10 ("+1") and 01 ("-1") are valid. Additionally no subsequent "+1" or "-1" bits are allowed (bipolar violations). A dual rail data stream is passed transparently, even if it contains bipolar violations. A single rail data stream is encoded to a correct AMI coded bipolar data stream without zero code suppression.

4.2.6.2 B3ZS Code

In the B3ZS line code each block of three consecutive zeros is replaced by either of two replacements codes which are B0V and 00V, where B represents a pulse which applies to the bipolar rule ("+1" or "-1") and V represents a bipolar violation (two consecutive "+1" or "-1" bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

The transmit line encoder detects three-zeros pattern sequences and changes them to the appropriate replacement pattern.

Although B3ZS coding is normally used with single rail NRZ data, the transmit line encoder accepts either dual rail or single rail data. Bipolar violations in an incoming dual rail data stream are converted to valid data pulses.

4.2.6.3 HDB3 Code

In the HDB3 line code each block of four consecutive zeros is replaced by either of two replacements codes which are B00V and 000V, where B represents a pulse which applies to the bipolar rule ("+1" or "-1") and V represents a bipolar violation (two consecutive "+1" or "-1" bits). The replacement code is chosen in a way that there is an odd number of valid B pulses between consecutive V pulses to avoid the introduction of a DC component into the analog signal.

The transmit line encoder detects three-zeros pattern sequences and changes them to the appropriate replacement pattern.

Although HDB3 coding is normally used with single rail NRZ data, the transmit line encoder accepts either dual rail or single rail data. Bipolar violations in an incoming dual rail data stream are converted to valid data pulses.

4.2.7 AIS Insertion

An unframed all-ones signal can be inserted into the transmitted data stream. To fulfill the required accuracy, a reference clock of ± 20 ppm is needed on pin REFCLK.

If local loop configuration and AIS insertion is selected together, the AIS signal is looped back to RDOP/RDON.

4.3 Framer Interface

The interface to the receive framer is realized by RDOP, RDON and RCLK. Data at RDOP/N are clocked off with either the rising (RPE=1) or falling edge (RPE=0) of RCLK.

Alternatively a single rail signal can be selected to be output on pin RDOP (DR/$\overline{\text{SR}}$=0). Bipolar violation indications are output on pin RDON/BPV in this case.

Data from the framer interface are sampled at XDIP and XDIN on the active edge of the XCLK. The active edge can be the rising (XPE=1) or falling edge (XPE=0) of XCLK.

Alternatively a single rail signal can be used on pin XDIP (DR/$\overline{\text{SR}}$=0).

Note: Selection of dual rail/single rail mode is common to receive and transmit direction.

See **Figure 24** on **page 47** and **Figure 25** on **page 48** for details.

4.4 Maintenance Functions

4.4.1 Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 are routed back to the line outputs XL1/2. As in normal mode they are also processed by the synchronizer and then sent to the framer interface. Data passes the decoder and encoder circuit. The recovered receive clock is used to drive the transmit pulse shaper.

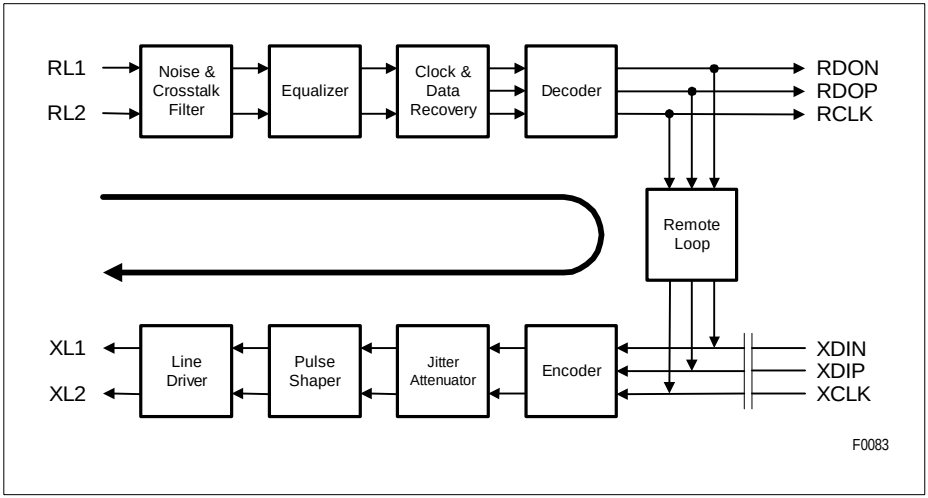


Figure 16 Remote Loop Signal Flow

Note: If remote loop and local loop are selected simultaneously, the device will be set into power down mode.

Note: The jitter attenuator can be switched off optionally.

4.4.2 Local Loop

The local loopback mode disconnects the receive lines RL1/2 from the receiver. Instead of the signals coming from the line data provided by system interface is routed through the analog receiver back to the framer interface. The transmit bit stream is sent to the transmit line unchanged. If XAIS=1 is selected, the transmit data stream is replaced by an all-ones signal and looped back.

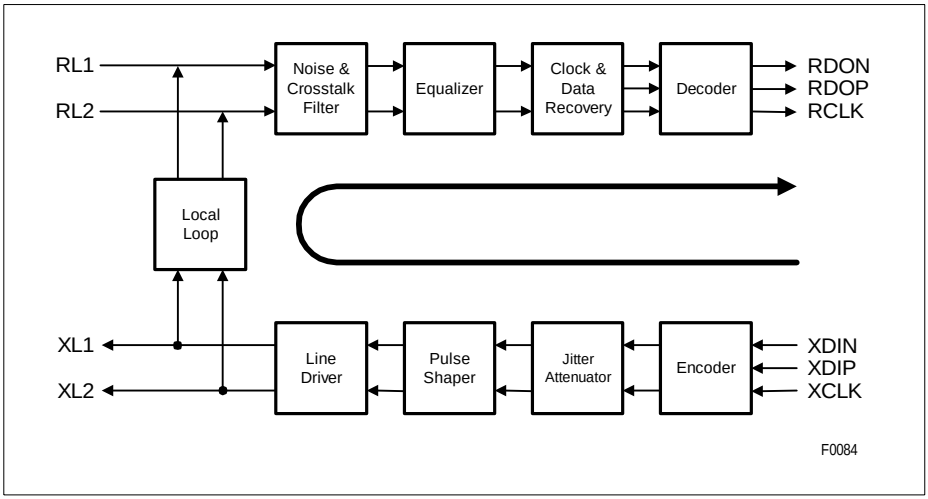


Figure 17 Local Loop Signal Flow

Note: If remote loop and local loop are selected simultaneously, the device will be set into power down mode.

Note: The jitter attenuator can be switched off optionally.

5 Operational Description

5.1 Operational Overview

The TE3-LIU™ can be operated in three principle modes, which are either E3, DS3 or STS-1 mode. This basic operation mode selection has to be stable before the reset signal goes inactive.

The device is programmable by pin selection. Direct connection to a microprocessor data bus is possible by using the chip select pin ($\overline{CS}$) as a write strobe.

5.2 Device Reset

The TE3-LIU™ is forced to the reset state if a low signal is input on pin $\overline{RES}$ (for minimum period see page 42). During reset, all output stages are in a high impedance state, all internal flip-flops are reset.

The basic device mode (DS3, STS-1 or E3, jitter attenuation) has to be selected during reset to enable the internal PLLs to adjust.

After reset all control input values are cleared. The default control values (driven by internal pullups) are activated after $\overline{CS}$ = low is applied for the first time after reset.

5.3 Device Power Down

The TE3-LIU™ can be set into power down state to reduce power consumption, if not active. Power down mode is selected by setting RL=LL=1. Receive and transmit circuits are switched off including internal PLLs and transmit line driver. Recovery from power down mode is achieved by clearing either of RL or LL (RL = 0 and/or LL = 0). After recovery from power down, the internal PLLs need to stabilize again. REFCLK must be active to recover from power down mode.

Internal pullup resistors are not switched off during power down to prevent open input lines from floating.

Note: If switching directly from local loop to remote loop or vice versa, make sure that there is no signal overlap, which would set the device into power down mode unintentionally.

5.4 Transmit Line Inactive

If the transmitter is not used, it can be switched into inactive mode by setting XLT=1. During inactive state the common mode voltage of 1.5 V is output on XL1 and XL2. The transmit PLL is not stopped and output can be enabled again by XLT=0 without wait time.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 15 Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
IC supply voltage (digital)	V_{DD}	– 0.4 to 4.5	V
IC supply voltage receive (analog)	V_{DDR}	– 0.4 to 4.5	V
IC supply voltage transmit (analog)	V_{DDX}	– 0.4 to 4.5	V
Voltage on any output pin with respect to ground	V_{SO}	– 0.4 to 4.5	V
Voltage on any input pin with respect to ground	V_{SI}	– 0.4 to 5.5	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Operating Range

Table 16 Power Supply Range

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{DD} V_{DDR} V_{DDX} V_{DDRP} V_{DDXP}	3.13	3.46	V	3.3 V ± 5%
Digital input voltages	V_{ID}	0	5.25	V	5.0 V + 5%
Ground	V_{SS} V_{SSR} V_{SSX} V_{SSRP} V_{SSXP}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled. All V_{DD} pins have to be connected to the same voltage level, All V_{SS} pins have to be connected to ground level.

Note: Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and 3.3V supply voltage.

6.3 DC Characteristics

Table 17 DC Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.4	0.8	V	
Input high voltage	V_{IH}	2.0	5.25	V	
Output low voltage	V_{OL}		0.45	V	I_{OL} = + 4 mA[1)]
Output high voltage	V_{OH}	2.4		V	I_{OH} = – 4 mA [1)]
Average power supply current	I_{DD}	110 (typ.)		mA	typical (DS3, PRBS, JATT enabled, 3.3 V)
		155 (typ.)			worst case (STS-1, JATT enabled, AIS, 3.46 V)
Input leakage current	I_{IL11}		1	µA	$V_{IN} = V_{DD}$[2)]
Input leakage current	I_{IL12}		1	µA	$V_{IN} = V_{SS}$[2)]
Input pullup current	I_{IPU}	2	25	µA	$V_{IN} = V_{SS}$
		5 (typ.)			
Input pulldown current	I_{IPU}	– 2	– 25	µA	$V_{IN} = V_{DD}$
		-5 (typ.)			
Transmitter leakage current	I_{TL}		1	mA	XL1/2 = V_{DDX}, XLT = 1
			1	mA	XL1/2 = V_{SSX}, XLT = 1
			200	µA	XL1/2 = 1.50 V[3)], XLT = 1
Transmitter output impedance	R_X	5 (typ.)		Ω	applies to XL1and XL2[4)]
Differential peak voltage of a mark (at XL1/XL2)	V_X		2.0	V	
Receiver differential peak voltage of a mark (at RL1/RL2)	V_R		V_{DDR}+0.3	V	RL1, RL2
Receiver input impedance	Z_R	tbd.		kΩ	[3)]

Table 17 DC Parameters (cont'd)

Parameter (cont'd)	**Symbol**	**Limit Values**		**Unit**	**Notes**
		min.	**max.**		
Receiver sensitivity	S_{RSH}	0	tbd.	dB	RL1, RL2
Analog loss of Signal threshold E3	V_{LOS3}	-35	– 15	dB	

1) applies to all output pins except analog pins XL1/XL2

2) Input leakage currents of pins containing internal pullup devices are measured in a testmode which switches off the pullups.

3) test against common mode voltage, parameter not tested in production

4) parameter not tested in production

6.4 AC Characteristics

6.4.1 Reset

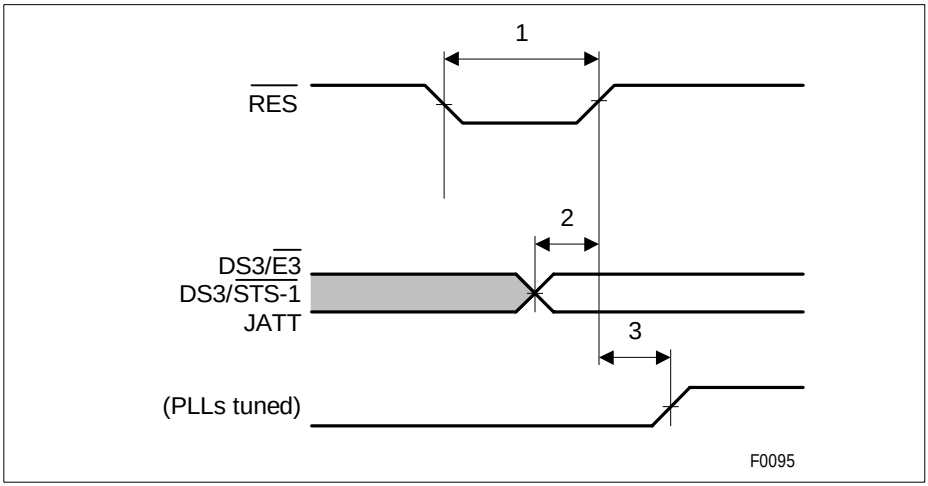


Figure 18 Reset Timing

Table 18 Reset Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	$\overline{\text{RES}}$ pulse width low	10		µs
2	DS3/$\overline{\text{E3}}$, DS3/$\overline{\text{STS-1}}$, JATT to $\overline{\text{RES}}$ setup time	5		ns
3	PLL startup time		1000	µs

Note: REFCLK must be active during reset.

6.4.2 Reference Clock

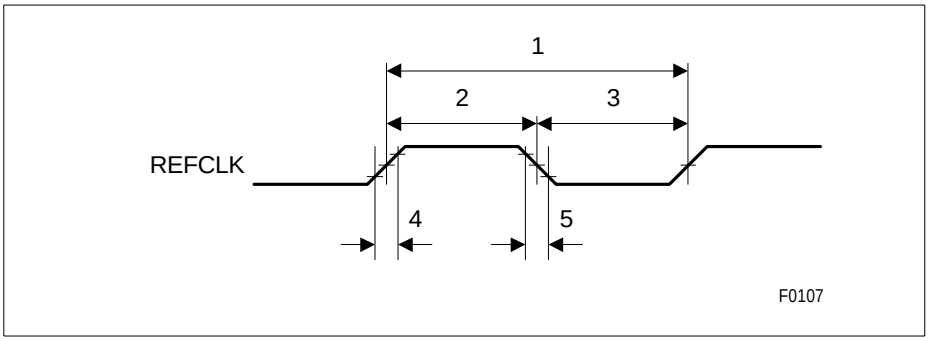


Figure 19 Reference Clock Timing

Table 19 REFCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	REFCLK period E3		29.1		ns
	REFCLK period DS3		22.4		ns
	REFCLK period STS-1		19.3		ns
2	REFCLK high	20		80	%
3	REFCLK low	20		80	%
4	REFCLK rise time			4[1)]	ns
5	REFCLK fall time			4[1)]	ns
	Clock accuracy			20[2)]	ppm

1) not tested in production

2) if DS3-AIS function is not required, 200 ppm is sufficient to guarantee correct receive PLL function

6.4.3 Jitter Attenuator Reference Clock

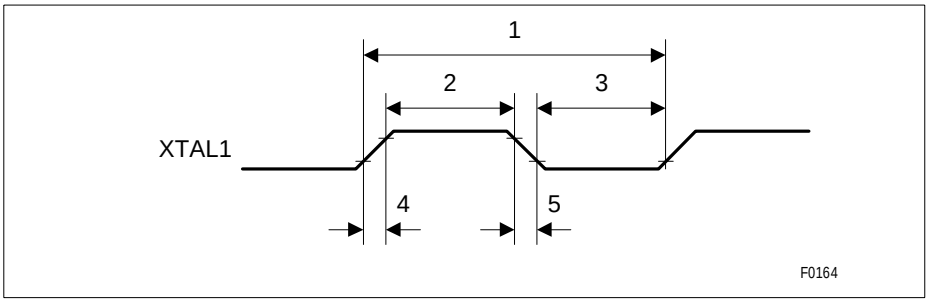


Figure 20 XTAL Clock Timing

Table 20 XTAL Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	XTAL1/2 period E3		87.29		ns
	XTAL1/2 period DS3		67.06		ns
	XTAL1/2 period STS-1		57.87		ns

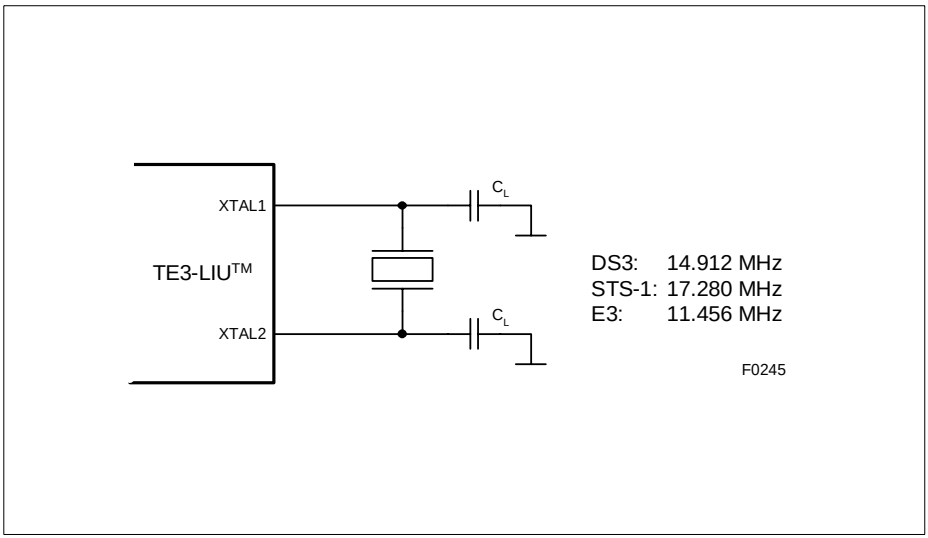


Figure 21 Recommended Crystal Circuit

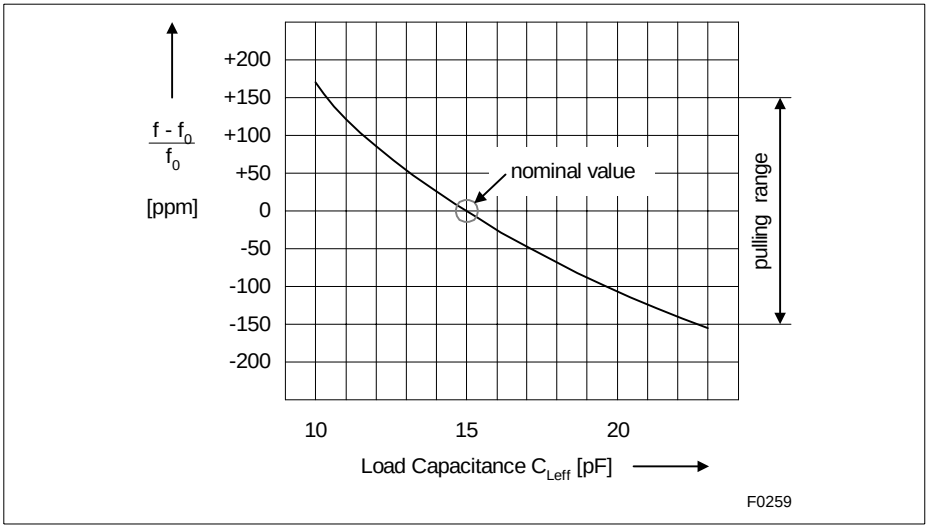


Figure 22 Crystal Pulling Range

Table 21 XTAL Crystal Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	Crystal nominal frequency DS3		14.912		MHz
	Crystal nominal frequency STS-1		17.280		MHz
	Crystal nominal frequency E3		11.456		MHz
2	Crystal motional capacitance C_1		25		fF
3	Crystal shunt capacitance C_0		7		pF
4	Crystal load capacitance C_{Leff} [1)]		15		pF
5	Crystal resonance resistance R_r			30	Ω
6	Internal parasitic load capacitance C_{Lint}		7.5		pF

1) This value includes the capacitance of the external capacitors (C_{Lext}) plus all internal (C_{Lint}) and external parasitic capacitances (C_{Lpara}). The value of the external capacitor has to be chosen depending on the printed circuit board layout. A typical value for C_L is 0 to 10 pF, C_L should be adapted to the parasitics to achieve a symmetrical pulling range.

Note: $C_{Leff} = C_{Lext} + C_{Lint} + C_{Lpara}$
$C_{Lext} = 0.5 \times C_L$

6.4.4 Microprocessor Control

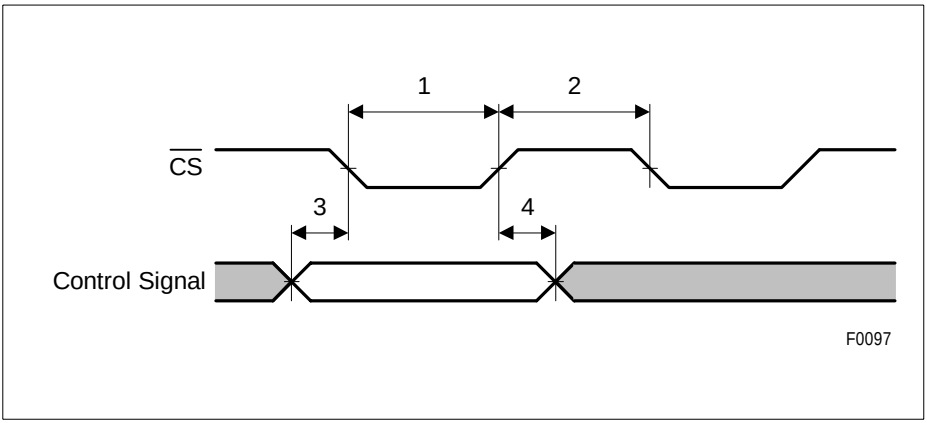


Figure 23 Chip Select Timing

Table 22 Chip Select Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	$\overline{CS}$ pulse width low	$2.5 \times T_{RCLK}$		
	E1	73		ns
	DS3	56		ns
	STS-1	50		ns
2	$\overline{CS}$ pulse width high	$2.5 \times T_{RCLK}$		
	E1	73		ns
	DS3	56		ns
	STS-1	50		ns
3	Control Signal Setup Time	10		ns
4	Control Signal Hold Time	10		ns

6.4.5 Transmit Input Timing

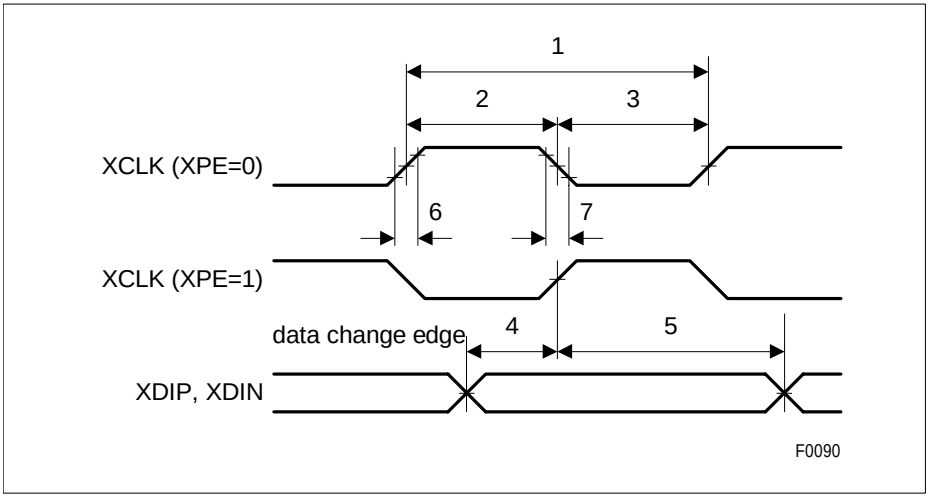


Figure 24 XCLK Input Timing

Table 23 XCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	XCLK period E3		29.1		ns
	XCLK period DS3		22.4		ns
	XCLK period STS-1		19.3		ns
2	XCLK high	30		70	%
3	XCLK low	30		70	%
4	XDIP, XDIN setup time	2			ns
5	XDIP, XDIN hold time	2			ns
6	XDIP, XDIN, XCLK rise time			1[1)]	ns
7	XDIP, XDIN, XCLK fall time			1[1)]	ns
8	Clock accuracy			20[2)]	ppm

1) not tested in production

2) if DS3-AIS function is not required, 200 ppm is sufficient to guarantee correct PLL function

6.4.6 Receive Output Timing

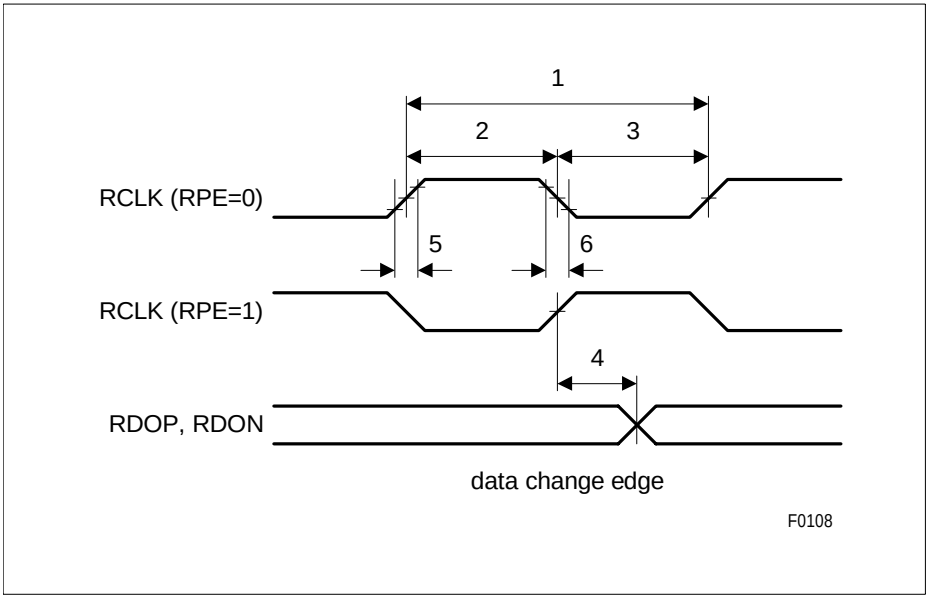


Figure 25 RCLK Output Timing

Table 24 RCLK Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	RCLK period E3		29.1[1)]		ns
	RCLK period DS3		22.4[1)]		ns
	RCLK period STS-1		19.3[1)]		ns
2	RCLK high	40	50	60	%
3	RCLK low	40	50	60	%
4	RDOP, RDON delay time	0	1	2[2)]	ns
5	RDOP, RDON, RCLK rise time		2	5[2)]	ns
6	RDOP, RDON, RCLK fall time		2	5[2)]	ns

1) applies only while the receiver PLL is locked to a valid signal on RL1/RL2, e.g., not in case of LOS

2) not tested in production

6.4.7 Pulse Templates

6.4.7.1 Pulse Template E3

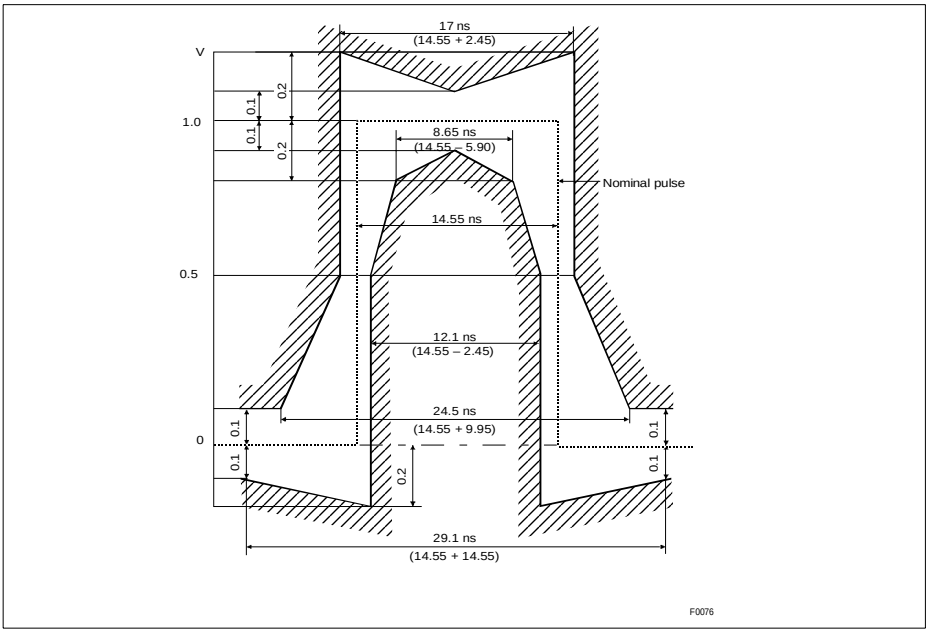


Figure 26 E3 Pulse Shape at Transmitter Output

Table 25 E3 Pulse Mask[1)]

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
	Nominal peak voltage of a mark (pulse)		1.0		V
	Peak voltage of a space (no pulse)	- 0.1		0.1	V
	Nominal pulse width		14.55		ns
	Amplitude ratio of positive to negative pulses[2)]	0.95		1.05	
	Pulse width ratio of positive to negative pulses[3)]	0.95		1.05	

1) measured at the output port without transmission line and 75Ω load;
bit sequence: 0000000(+1)0000000(-1)0000000(+1)0000000(-1)...

2) at the center of a pulse interval

3) at the nominal half amplitude

6.4.7.2 Pulse Template DS3

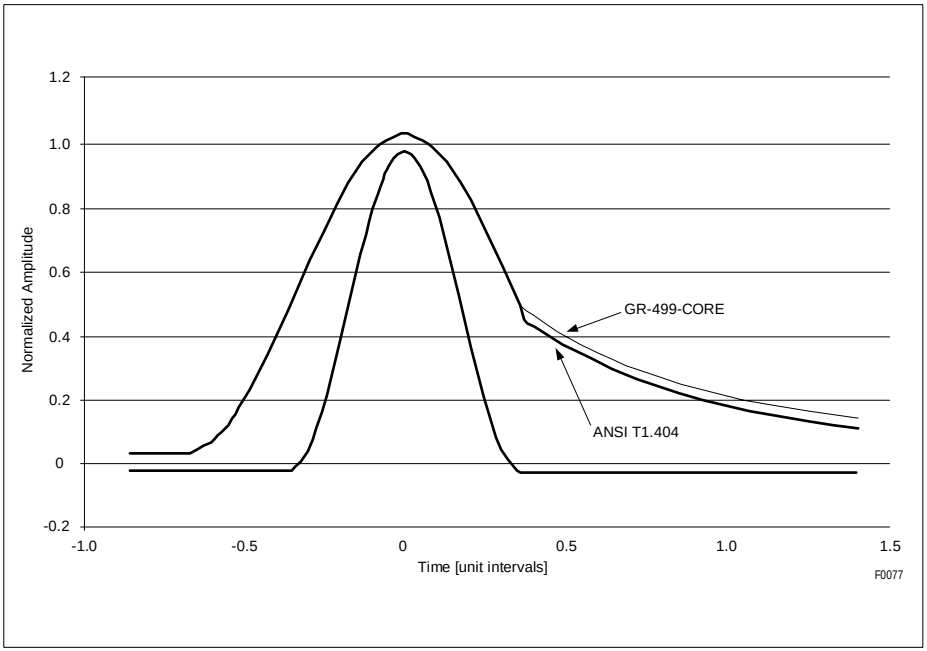


Figure 27 DS3 Pulse Shape at the Cross Connect Point (450 ft.)

Table 26 DS3 Pulse Mask (ANSI T1.404, GR-499-CORE)[1)]

Absolute Voltage Level (100 % Value)	
min.	**max.**
0.36 V	0.85 V

1) bit sequence: 0000000(+1)0000000(-1)0000000(+1)0000000(-1)...

Table 27 DS3 Pulse Mask (ANSI T1.404)

Lower Curve	
Time	**Equation**
T ≤ -0.36	-0.03
-0.36 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
T ≥ +0.36	-0.03

Upper Curve	
Time	**Equation**
T ≤ -0.68	+0.03
-0.68 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
T ≥ +0.36	$0.05 + 0.407 \times e^{-1.84[T - 0.36]}$

Table 28 DS3 Pulse Mask (GR-499-CORE)

Lower Curve	
Time	**Equation**
-0.85 ≤ T ≤ -0.36	-0.03
-0.36 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
+0.36 ≤ T ≤ +1.4	-0.03

Upper Curve	
Time	**Equation**
-0.85 ≤ T ≤ -0.68	+0.03
-0.68 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
+0.36 ≤ T ≤ +1.4	$0.08 + 0.407 \times e^{-1.84[T - 0.36]}$

6.4.7.3 Pulse Template STS-1

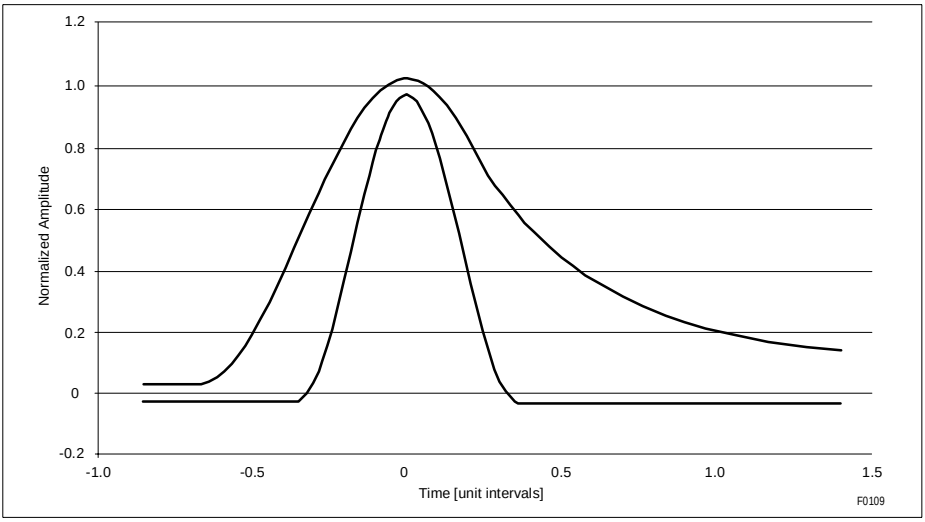


Figure 28 STS-1 Pulse Shape at the Cross Connect Point (450 ft.)

Table 29 STS-1 Pulse Mask[1)]

Signal Power	
min.	**max.**
- 2.7 dBm	+ 4.7 dBm

1) bit sequence: (+1)0(-1)0(+1)0(-1)...

Table 30 STS-1 Pulse Mask (ANSI T1.102)

Lower Curve	
Time	**Equation**
-0.85 ≤ T ≤ -0.38	-0.03
-0.38 ≤ T ≤ +0.36	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
+0.36 ≤ T ≤ +1.4	-0.03

Upper Curve	
Time	**Equation**
-0.85 ≤ T ≤ -0.68	+0.03
-0.68 ≤ T ≤ +0.26	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
+0.26 ≤ T ≤ +1.4	$0.1 + 0.61 \times e^{-2.4[T - 0.26]}$

6.5 Capacitances

Table 31 Pin Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input capacitance[1)]	C_{IN}	5	10	pF	
Output capacitance[1)]	C_{OUT}	8	15	pF	all except XL1, XL2
Output capacitance[1)]	C_{OUT}	8	20	pF	XL1, XL2

1) not tested in production

6.6 Package Characteristics

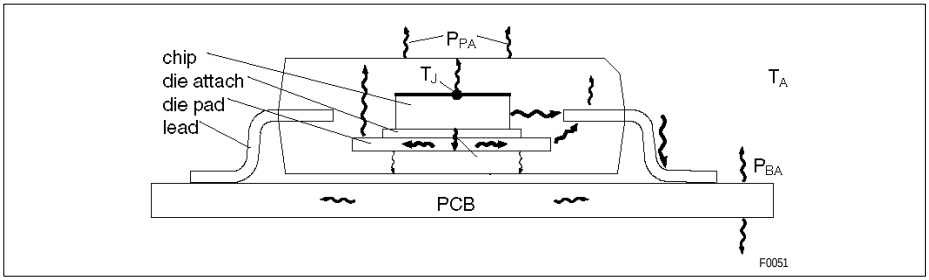


Figure 29 Thermal Behavior of Package

Table 32 Package Characteristic Values

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance[1)] Junction to Ambient	R_{thJA}		63		K/W	single layer PCB, 30%/11 µm metallization, 1W, no convection
Thermal Resistance[2)] Junction to Case	R_{thJC}		15		K/W	
Junction Temperature	R_j			125	°C	

1) $R_{thJA} = (T_{junction} - T_{ambient})/Power$
not tested in production

2) $R_{th}JC = (T_{junction} - T_{case})/Power$
not tested in production

6.7 Test Configuration

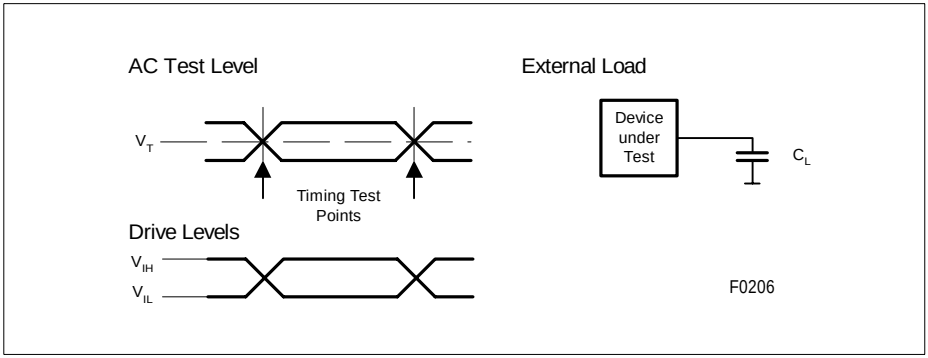


Figure 30 Input/Output Waveforms for AC Testing

Table 33 AC Test Conditions

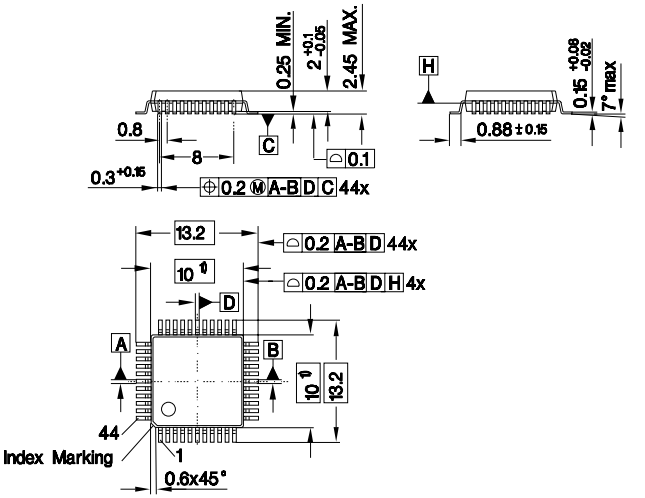
Parameter	Symbol	Test Values	Unit	Notes
Load Capacitance 1	C_{L1}	50	pF	digital outputs except RDOP, RDON, RCLK
Load Capacitance 2	C_{L2}	15	pF	digital outputs RDOP, RDON and RCLK
Load Capacitance 3	C_{L3}	50	pF	analog line output XL1, XL2
Input Voltage high	V_{IH}	2.4	V	all except RL1, RL2
Input Voltage low	V_{IL}	0.4	V	all except RL1, RL2
Test Voltage	V_T	$V_{DD}/2$	V	all except XL1, XL2
Output Test Load	R_L	75 ± 5%	Ω	XL1, XL2
Rise Times	T_R	10 - 90	%	not tested in production
Fall Times	T_F	90 - 10	%	

Note: Typical characteristics are mean values expected over the production spread. If not specified otherwise, typical characteristics apply at T_A = 25 °C and V_{DD} = 3.3V.

Note: Capacitance values include all parasitics caused by board layout, transformer etc.

7 Package Outlines

P-MQFP-44-2
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

8 Appendix

8.1 Cable Characteristics

Cable characteristics are defined in ANSI T1.102 as shown below.

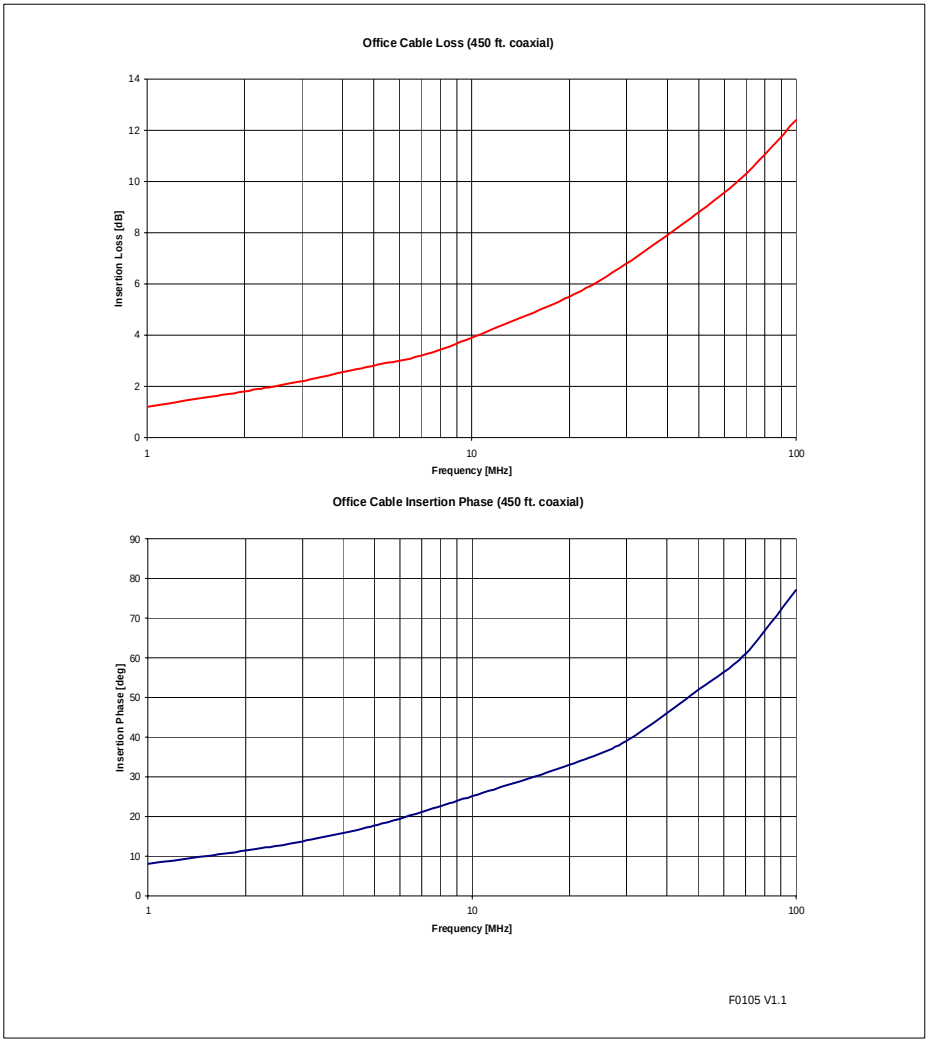


Figure 31 DS3 Cable Characteristics

8.2 Application Example

The following picture shows a typical application circuit (excluding surge protection).

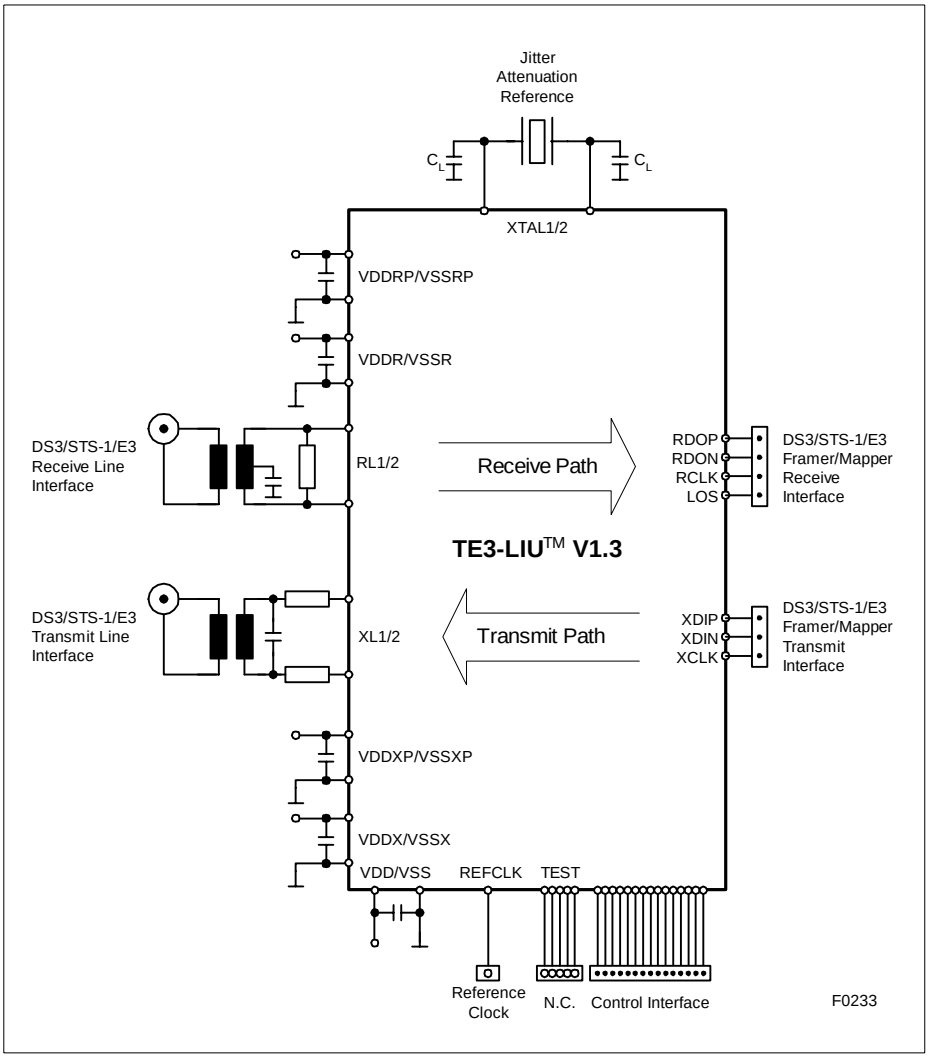


Figure 32 Application Circuit

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PRELIMINARY

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Dr. Ulrich Schumacher

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