



RFD12N06RLE, RFD12N06RLESM RFP12N06RLE

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

January 1994

Features

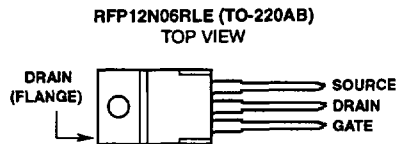
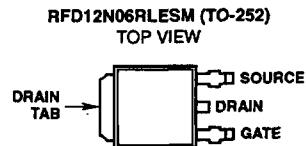
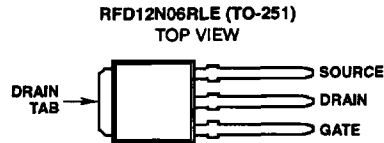
- 12A, 60V
- $r_{DS(on)} = 0.135\Omega$
- Electrostatic Discharge Rated
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drive
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

These N-channel logic-level ESD protected power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic-level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

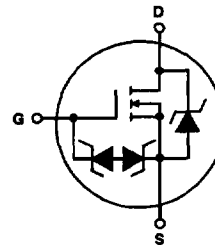
The RFD12N06RLE is supplied in the JEDEC TO-251, RFD12N06RLESM in the JEDEC TO-252, and RFP12N06RLE in the JEDEC TO-220AB plastic package.

Packages



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

		UNITS
Drain-Source Voltage	V_{DS}	60 V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60 V
Continuous Drain Current		
RMS Continuous	I_D	12 A
Pulsed Drain Current	I_{DM}	26 A
Gate-Source Voltage	V_{GS}	+10 -5V
Maximum Power Dissipation		
$T_C = +25^\circ\text{C}$	P_D	40 W
Above $T_C = +25^\circ\text{C}$, Derate Linearly		0.32 W/°C
Single Pulse Avalanche Rating, Refer to UIS SOA Curve Electrostatic Discharge Rating, ESD, MIL-STD-883, Category B(2)		2 KV
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150 °C

Specifications RFD12N06RLE, RFD12N06RLESM, RFP12N06RLE

ELECTRICAL CHARACTERISTICS, Case Temperature (T_c) = 25° C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS		
		RFD12N06RLE RFD12N06RLESM RFP12N06RLE				
		Min	Max			
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 0.25 \text{ mA}$ $V_{GS} = 0 \text{ V}$	60	—	V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 0.25 \text{ mA}$	1	2		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$ $T_c = 150^\circ \text{ C}$	—	1 50	μA	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = +10 \text{ V}$ $V_{GS} = -5 \text{ V}$	—	10 10		
On Resistance	$r_{DS(on)}$	$V_{GS} = 5.0 \text{ V}$, $I_D = 12 \text{ A}$ $V_{GS} = 4.0 \text{ V}$, $I_D = 12 \text{ A}$	—	0.135 0.160	Ω	
Turn-On Time	$t_{(on)}$	See Fig. 13	—	60	ns	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}$, $I_D = 6 \text{ A}$	12 (typ)	—		
Rise Time	t_r	$R_L = 5.0 \Omega$	20 (typ)	—		
Turn-Off Delay Time	$t_{d(off)}$	$I_{g1} = I_{g2} = 0.4 \text{ A}$	24 (typ)	—		
Fall Time	t_f	$V_{GS(clamp)} = +5 \text{ V}$, -0.6 V	12 (typ)	—		
Turn-Off Time	$t_{(off)}$		—	60		
Total Gate Charge	$Q_{g(tot)}$	$V_{GS} = 0-10 \text{ V}$	$V_{DD} = 48 \text{ V}$ $I_D = 12 \text{ A}$ $R_L = 4.0 \Omega$	—	40	nC
Gate Charge at 5 Volts	$Q_{g(5)}$	$V_{GS} = 0-5 \text{ V}$		—	20	
Threshold Gate Charge	$Q_{g(th)}$	$V_{GS} = 0-1 \text{ V}$		—	1.5	
Plateau Voltage	$V_{(plateau)}$	$I_D = 12 \text{ A}$, $V_{DS} = 15 \text{ V}$	—	4.0	V	
Turn-Off Energy Loss per Cycle	E_{off}	$V_{DD} = 30 \text{ V}$, $I_D = 6 \text{ A}$ $L = 0.2 \mu\text{H}$, $I_{g1} = I_{g2} = 0.4 \text{ A}$ $V_{GS(clamp)} = +5.0 \text{ V}$, -0.6 V $R_L = 5.0 \Omega$	—	10	μJ	
Thermal Resistance Junction to Case	$R\theta_{JC}$		—	3.125	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R\theta_{JA}$	TO-251 & TO-252 packages TO-220 package	—	100 80		

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**LOGIC LEVEL
POWER MOSFETS**

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Forward Voltage	V_{SD}	$I_{SD} = 12 \text{ A}$	—	1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 12 \text{ A}$ $dI_F/dt = 100 \text{ A}/\mu\text{s}$	—	200	ns

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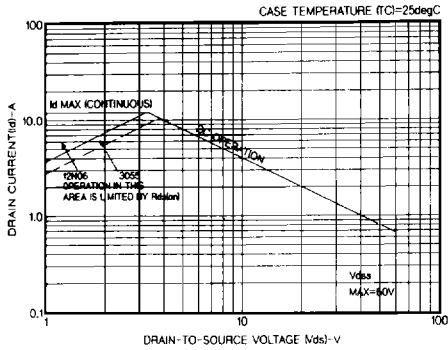


Fig. 1 - Safe-operating area curve. (Curves must be derated linearly with increase in case temperature.)

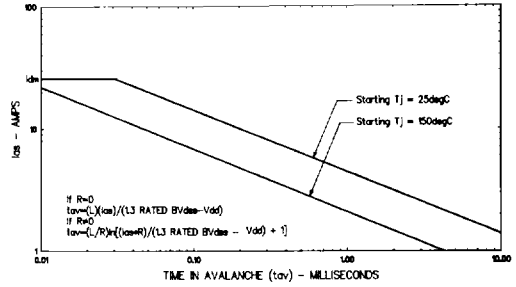


Fig. 2 - Unclamped-inductive-switching. Safe-operating-area. (Single pulse UIS SOA.)

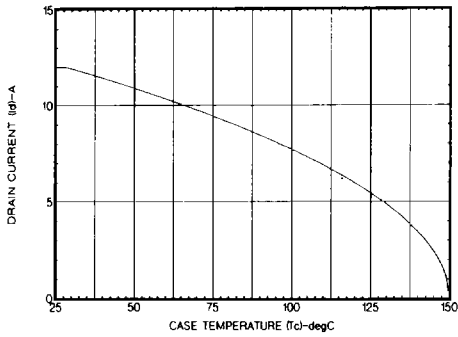


Fig. 3 - Maximum continuous drain current vs. temperature.

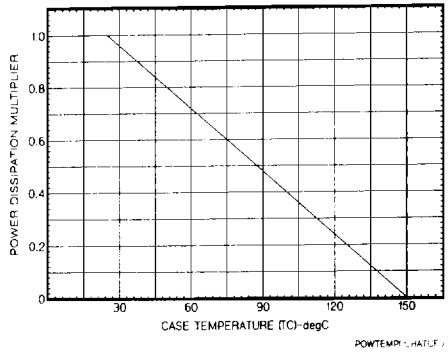


Fig. 4 - Normalized power dissipation vs. temperature derating curve.

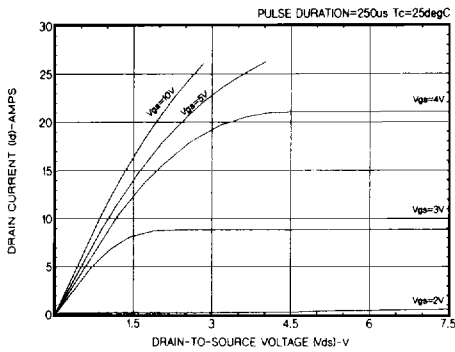


Fig. 5 - Typical saturation characteristics.

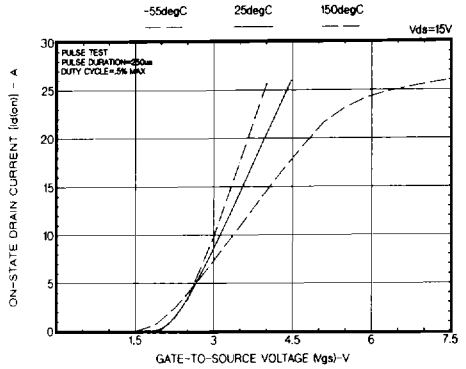


Fig. 6 - Typical transfer characteristics.

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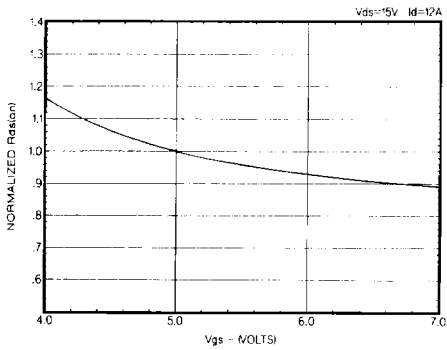


Fig. 7 - Normalized $r_{DS(on)}$ vs. V_{GS} .

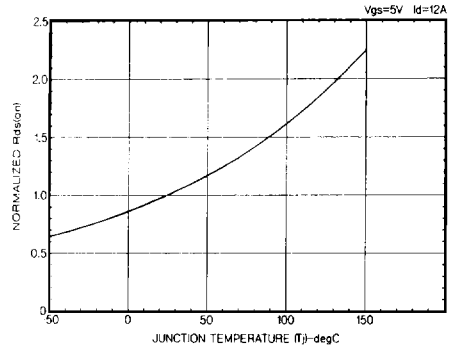


Fig. 8 - Normalized $r_{DS(on)}$ vs. junction temperature.

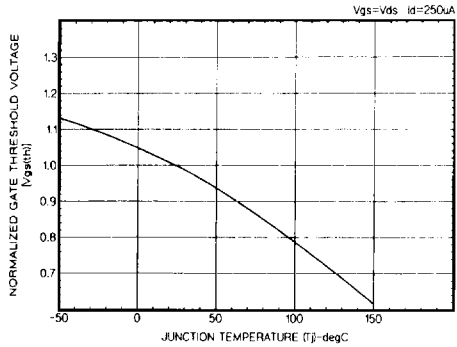


Fig. 9 - Normalized gate threshold voltage vs. temperature.

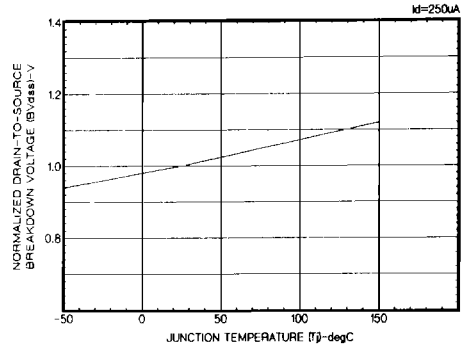


Fig. 10 - Normalized drain source breakdown voltage vs. temperature.

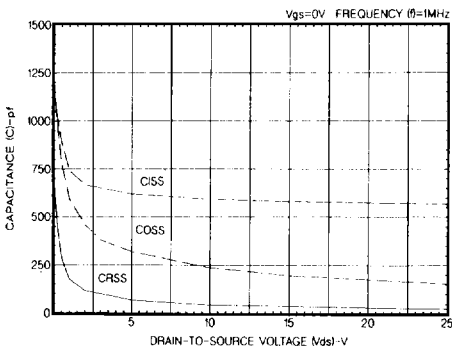


Fig. 11 - Typical capacitance vs. voltage.

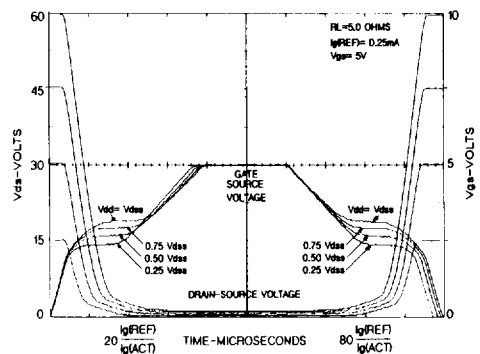
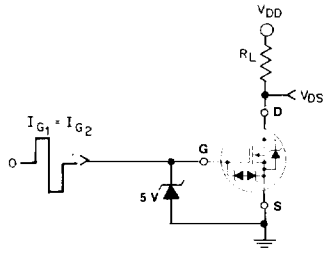


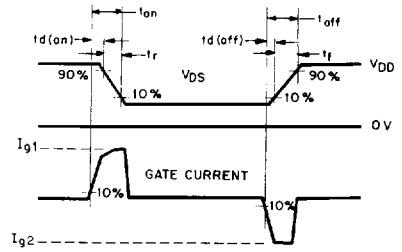
Fig. 12 - Typical switching waveforms for constant gate current. Refer to Harris application notes AN7254 and AN-7260.

**LOGIC LEVEL
POWER MOSFETS**

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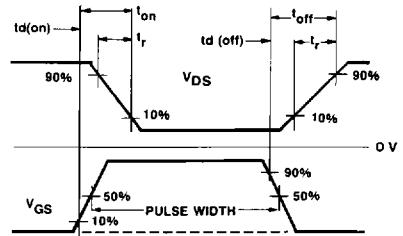
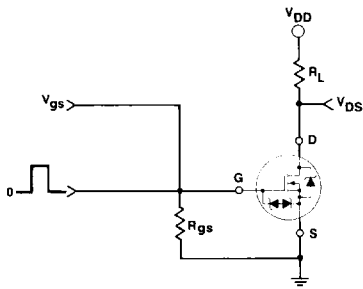


SWITCHING TEST CIRCUIT



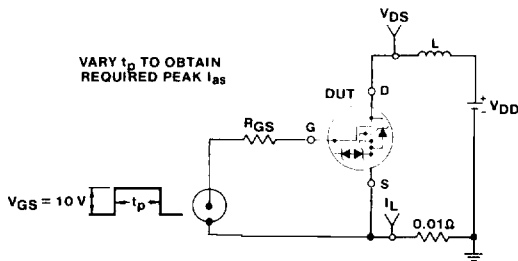
SWITCHING WAVEFORMS

Fig. 13 - Resistive switching.



SWITCHING WAVEFORMS

Fig. 14 - Resistive switching.



VARY t_p TO OBTAIN
REQUIRED PEAK I_{as}

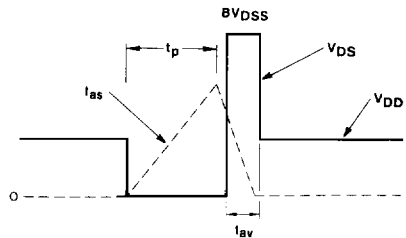


Fig. 15 - Unclamped inductive switching test.