CY2X013

LVDS Crystal Oscillator (XO)

Features

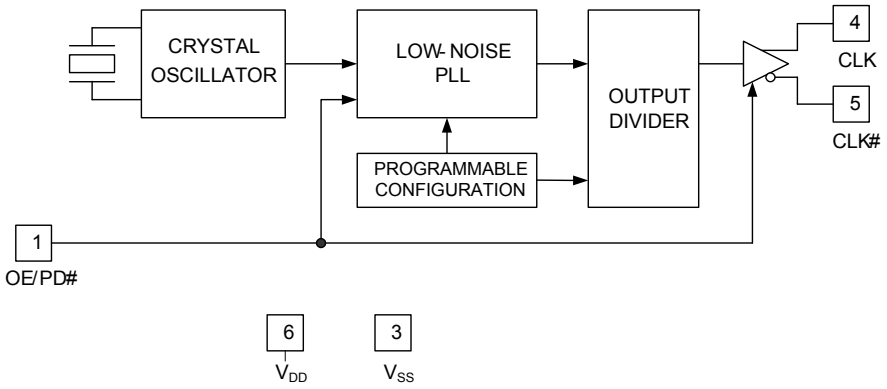
- Low jitter crystal oscillator (XO)
- Less than 1 ps typical root mean square (RMS) phase jitter
- Low-voltage differential signaling (LVDS) output
- Output frequency from 50 MHz to 690 MHz
- Factory-configured or field-programmable
- Integrated phase-locked loop (PLL)
- Output enable (OE) or power-down (PD#) function
- Supply voltage: 3.3 V or 2.5 V
- Pb-free package: 5.0 × 3.2 mm leadless chip carrier (LCC)
- Commercial and industrial temperature ranges

Functional Description

The CY2X013 is a high-performance and high-frequency XO. The device uses a Cypress proprietary low-noise PLL to synthesize the frequency from an integrated crystal.

The CY2X013 is available as a factory-configured device or as a field-programmable device. Factory-configured devices are configured for general use (see Standard and Application-Specific Factory Configurations) or they can be customer-specific.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram – 6-Pin Ceramic LCC

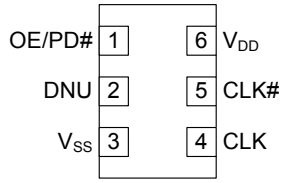


Table 1. Pin Definitions - 6-Pin Ceramic LCC

Pin	Name	I/O Type	Description
1	OE/PD#	CMOS input	Output enable pin: Active HIGH. If OE = 1, CLK is enabled. Power-down pin: Active LOW. If PD# = 0, the device is powered down and the clock is disabled. The functionality of this pin is programmable
4, 5	CLK, CLK#	LVDS output	Differential output clock
2	DNU	–	Do not use: DNU pins are electrically connected, but perform no function
6	V_{DD}	Power	Supply voltage: 2.5 V or 3.3 V
3	V_{SS}	Power	Ground

Standard and Application-Specific Factory Configurations

Part Number	Output Frequency	Pin 1 Function	RMS Phase Jitter (Random)	
			Offset Range	Jitter (Typical)
CY2X013LXI125T	125.00 MHz	OE	1.875 MHz to 20 MHz 12 kHz to 20 MHz	0.34 ps 0.84 ps
CY2X013LXI200T	200.00 MHz	OE	12 kHz to 20 MHz	0.74 ps

Programming Description

The CY2X013 is a programmable device. Prior to being used in an application, it must be programmed with the output frequency and other variables described in Programming Variables. Two different device types are available, each with its own programming flow. They are described in the following sections.

Field Programmable CY2X013F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a PCB. Customers use CyClockWizard™ software to specify the device configuration and generate a joint electron devices engineering council (JEDEC - extension .jed) programming file. Programming of samples and prototype quantities is available using the CyClockWizard software along with a CY3675-CLKMAKER1 CyClockMaker Clock Programmer Kit with a CY3675-LCC6A socket adapter. Cypress's value-added distribution partners also provide programming services. Field-programmable devices are designated with an 'F' in the part number. They are intended for quick prototyping and inventory reduction.

You can download the software and programmer kit hardware from www.cypress.com by clicking the hyperlinks in the previous paragraph.

Factory Configured CY2X013

For ready-to-use devices, the CY2X013 is available with no field programming required. Pre-configured devices (see Standard and Application-Specific Factory Configurations) are available for samples or orders, or a request for a custom configuration can be made. All requests are submitted to the local Cypress field application engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and datasheet with the programmed values. This part number is used for additional sample requests and production orders. The CY2X013 is one-time programmable (OTP).

Programming Variables

Output Frequency

The CY2X013 can synthesize a frequency to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2X013 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2X013 cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

Pin 1: Output Enable (OE) or Power-Down (PD#)

Pin 1 is programmed as either OE or PD#. The OE function is used to enable or disable the CLK output quickly, but it does not reduce core power consumption. The PD# function puts the device into a low-power state, but the wake-up takes longer because the PLL must reacquire the lock.

Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. They have a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyClockWIzard software allows the user to select between and view the expected performance of both options.

Table 2. Device Programming Variables

Variable
Output frequency
Pin 1 function (OE or PD#)
Temperature range (commercial or industrial)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	4.4	V
V_{IN}[1]	Input voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, storage	Non operating	–55	135	°C
T_J	Temperature, junction		–40	135	°C
ESD_{HBM}	Electrostatic discharge (ESD) protection human body model (HBM)	JEDEC Std 22-A114-B	2000	–	V
Θ_{JA}[2]	Thermal resistance, junction to ambient	0 m/s airflow	64		°C / W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3 V supply voltage range	3.0	3.3	3.6	V
	2.5 V supply voltage range	2.375	2.5	2.625	V
T_{PU}	Power-up time for V_{DD} to reach minimum specified voltage (power ramp is monotonic)	0.05	–	500	ms
T_A	Ambient temperature (commercial)	0	–	70	°C
	Ambient temperature (industrial)	–40	–	85	°C

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[3]	Operating supply current	V_{DD} = 3.6 V, OE/PD# = V_{DD}, output terminated	–	–	125	mA
		V_{DD} = 2.625 V, OE/PD# = V_{DD}, output terminated	–	–	120	mA
I_{SB}	Standby supply current	PD# = V_{SS}	–	–	200	µA
V_{OD}	LVDS differential output voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	247	–	454	mV
ΔV_{OD}	Change in V_{OD} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	–	–	50	mV
V_{OS}	LVDS offset output voltage	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	1.125	–	1.375	V
ΔV_{OS}	Change in V_{OS} between complementary output states	V_{DD} = 3.3 V or 2.5 V, R_{TERM} = 100 Ω between CLK and CLK#	–	–	50	mV
I_{OZ}	LVDS output leakage current	Tri-state output, unterminated, measured on one pin while floating the other pin, PD#/OE = V_{SS}	–35	–	35	µA
V_{IH}	Input high voltage		0.7 × V_{DD}	–	–	V
V_{IL}	Input low voltage		–	–	0.3 × V_{DD}	V
I_{IH}	Input high current	Input = V_{DD}	–	–	115	µA
I_{IL}	Input low current	Input = V_{SS}	–	–	50	µA
C_{IN}[3]	Input capacitance, OE/PD# pin		–	15	–	pF

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
3. I_{DD} includes ~4 mA of current that is dissipated externally in the output termination resistors.

AC Electrical Characteristics

The following table lists the AC electrical specifications for this device.[4]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output frequency[5]		50	–	690	MHz
FSC	Frequency stability, commercial devices[6]	V_{DD} = min to max, T_A = 0 °C to 70 °C	–	–	±35	ppm
FSI	Frequency stability, industrial devices[6]	V_{DD} = min to max, T_A = –40 °C to 85 °C	–	–	±55	ppm
AG	Aging, 10 years		–	–	±15	ppm
T_{DC}	Output duty cycle	F <= 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output rise and fall time	20% and 80% of full output swing	–	0.35	1.0	ns
T_{OHZ}	Output disable time	Time from falling edge on OE to stopped outputs (asynchronous)	–	–	100	ns
T_{OE}	Output enable time	Time from rising edge on OE to outputs at a valid frequency (asynchronous)	–	–	120	ns
T_{LOCK}	Startup time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min) or from PD# rising edge	–	–	5	ms
$T_{Jitter(\phi)}$	RMS phase jitter (random)	F_{OUT} = 106.25 MHz (12 kHz to 20 MHz)	–	1	–	ps
		Pre-defined factory configurations[7]	See Note 7			ps

Switching Waveforms

Figure 2. Output Voltage Swing

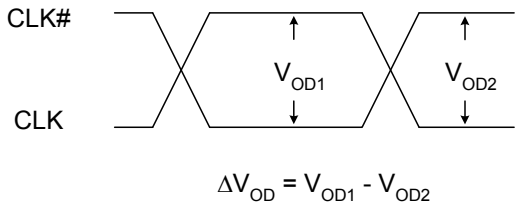
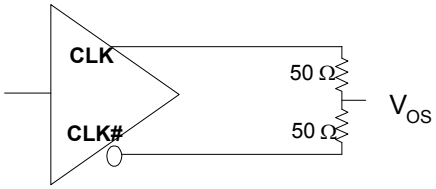


Figure 3. Output Offset Voltage



Notes
4. Not 100% tested, guaranteed by design and characterization.
5. This parameter is specified in the CyClockWizard software.
6. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, and variation from temperature and supply voltage.
7. Typical phase noise specs for factory programmed devices are listed in the Standard and Application-Specific Factory Configurations table on page 2.

Figure 4. Duty Cycle Timing

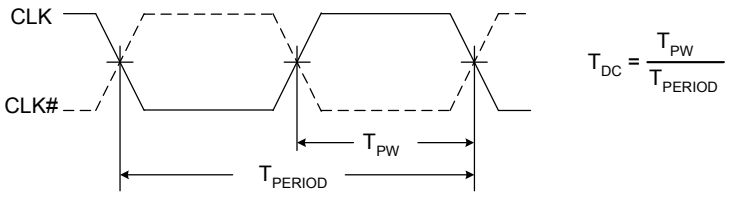


Figure 5. Output Rise and Fall Time

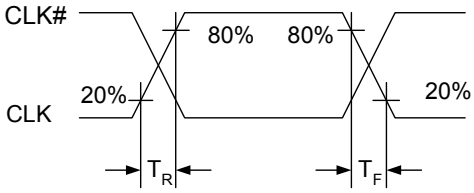
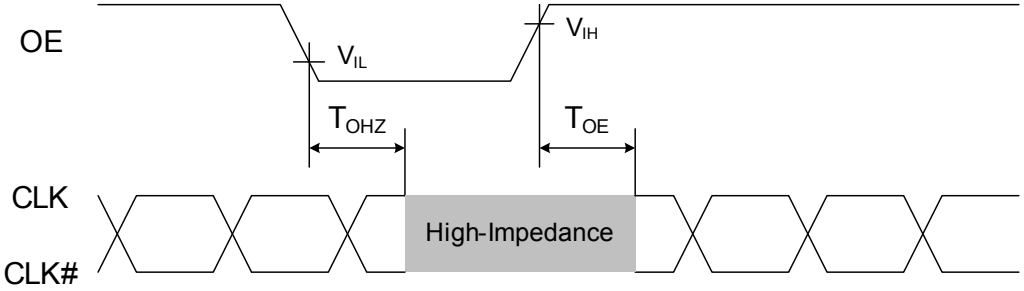
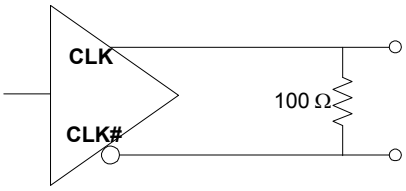


Figure 6. Output Enable and Disable Timing



Termination Circuits

Figure 7. LVDS Termination



Ordering Information

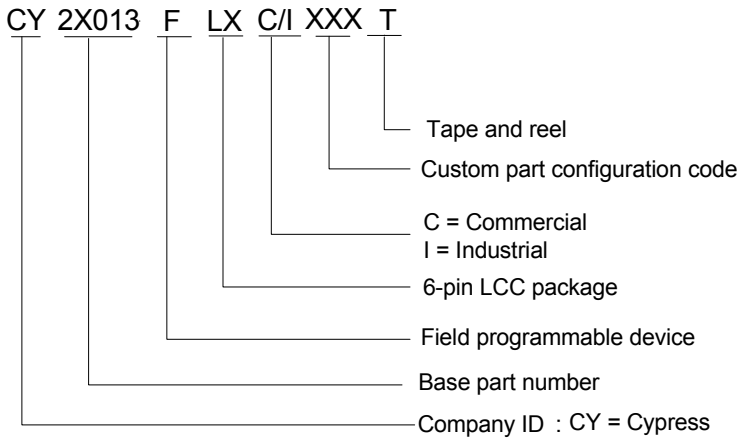
Part Number	Configuration	Package Description	Product Flow
Pb-free			
CY2X013FLXCT	Field-programmable	6-pin ceramic LCC SMD - tape and reel	Commercial, 0 °C to 70 °C
CY2X013FLXIT	Field-programmable	6-pin ceramic LCC SMD - tape and reel	Industrial, –40 °C to 85 °C
CY2X013LXI125T[8]	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Industrial, –40 °C to 85 °C
CY2X013LXI200T[8]	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Industrial, –40 °C to 85 °C

Some product offerings are factory programmed customer specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

Possible Configurations

Part Number[9]	Configuration	Package Description	Product Flow
Pb-free			
CY2X013LXCxxxT	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Commercial, 0 °C to 70 °C
CY2X013LXIxxxT	Factory-configured	6-pin ceramic LCC SMD - tape and reel	Industrial, –40 °C to 85 °C

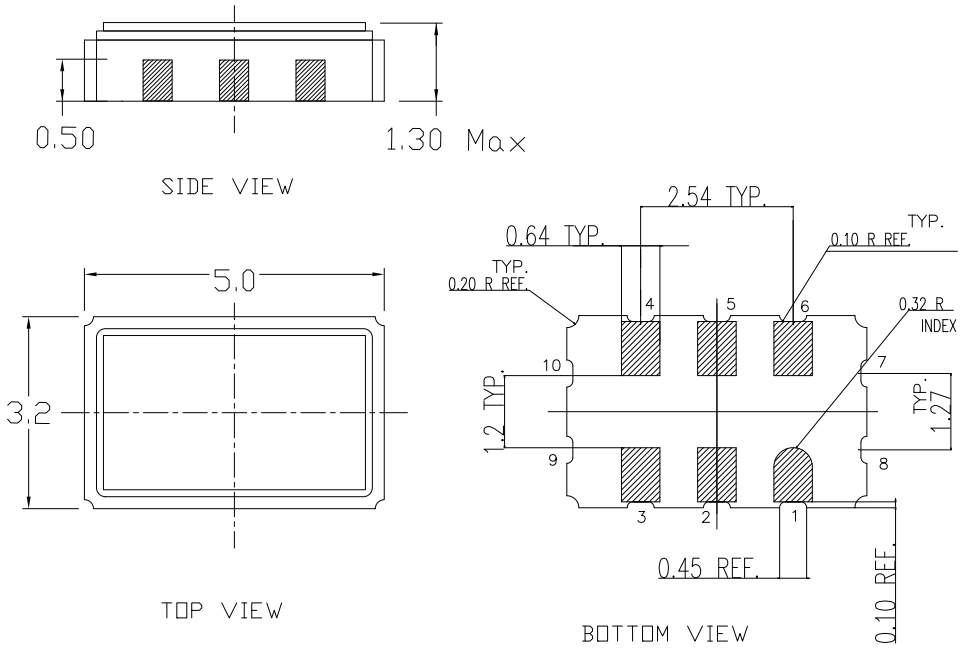
Ordering Code Definitions



Notes
8. Device configuration details are described in the Standard and Application-Specific Factory Configurations table on page 2.
9. "xxx" indicates factory programmed parts based on customer specific configuration. For more details, contact your local Cypress FAE or a sales representative.

Package Diagram

Figure 8. 6-Pin 5.0 × 3.2 mm Ceramic LCC



Dimensions in mm
Kyocera dwg ref KD-VA6432-A
Package Weight ~ 0.12 grams

001-10044 *B

Acronyms

Acronym	Description
ESD	electrostatic discharge
FAE	field application engineer
HBM	human body model
JEDEC	joint electron devices engineering council
LCC	leadless chip carrier
LVDS	Low-voltage differential signaling
OE	output enable
PCB	printed circuit board
PLL	phase-locked loop
RMS	root mean square
XO	crystal oscillator
OTP	one-time programmable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
mA	milliampere
mV	millivolts
MHz	megahertz
ms	millisecond
ns	nanoseconds
pF	picofarads
µA	microamperes
ppm	parts per million
ps	picoseconds
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY2X013 LVDS Crystal Oscillator (XO) Document Number: 001-10261				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	504518	RGL	09/21/06	New data sheet
*A	2705638	KVM/AESA	05/13/09	Removed pull up resistor on pin 1, Pin 2 changed from NC to DNU Added description of frequency range gaps, Removed frequency stability as a programming option; added phase noise / jitter optimization, Max storage temperature changed from 150 to 135°C, Max junction temperature changed from 125 to 135°C, Removed flammability and moisture sensitivity specs, Added thermal resistance data, IDD increased (100mA to 120 mA), conditions changed, and separate spec added for 2.5V supply, Changed IDD values and conditions, Standby current changed from 1mA to 250µA, Changes to IIL and IIH, Added CIN spec, Changed frequency stability and aging specs, Relaxed duty cycle spec added for >450 MHz, Removed period jitter spec, and Revised switching waveform figures
*B	2718898	WWZ	06/15/09	Minor ECN to post data sheet to external web
*C	2768029	KVM	09/18/09	Change V_{OD} limits from 250/450 mV to 247/454 mV Change I_{SB} max from 250 µA to 200 µA Add clause to I_{OZ} Condition column Add max limit for T_R, T_F: 1.0 ns Change T_{OE} max from 100 ns to 120 ns Change T_{LOCK} max from 10 ms to 5 ms
*D	2897691	KVM	03/23/10	Updated data sheet status from Preliminary to Final Updated Ordering Information Added Possible Configurations Updated Package Diagram
*E	2973338	CXQ	07/08/10	Added Standard and Application-Specific Factory Configurations table on page 2. Added phase jitter specs for pre-defined configurations in AC Electrical Characteristics (note 7 refers users to the new table on page 2 for typical specs). Added CY2X013LXI100T, CY2X013LXI122T, CY2X013LXI125T, and CY2X013LXI156T devices to Ordering Information and added note 8 to reference the configuration descriptions for each new device. Changed all references to CyberClocksOnline software to CyClockWizard. Removed section on phase noise versus jitter SW optimization.
*F	3047226	BASH	10/08/10	Added CY2X013LXI062T to Standard and Application-Specific Factory Configurations table on page 2 and to Ordering Information table. Added Acronym and Units of Measure table Updated datasheet as per template
*G	3205939	BASH	03/25/11	Added CY2X013LXI200T to Standard and Application-Specific Factory Configurations table on page 2 and to Ordering Information table.
*H	3846281	PURU	12/19/2012	Updated Standard and Application-Specific Factory Configurations (Removed pruned parts and their details). Updated Ordering Information (Updated part numbers). Updated Package Diagram: spec 001-10044 – Changed revision from *A to *B.

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