



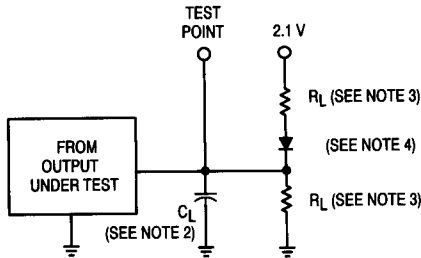
8-Input Data Selector/ Multiplexer With Enable

**ELECTRICALLY TESTED PER:
MIL-M-38510/30905**

The 54LS251 is a high-speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The 'LS251 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process For High-Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Inverting and Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

LOAD CIRCUIT FOR 3-STATE OUTPUT



Pin Names		Loading (Note a)	
		HIGH	LOW
S ₀ -S ₂	Select Inputs	0.5 U.L.	0.25 U.L.
E \bar{O}	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I ₀ -I ₇	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z $\bar{}$	Multiplexer Output	65 U.L.	15 U.L.
Z	Complementary Multiplexer Output	65 U.L.	15 U.L.

NOTE:

- a. One TTL Unit Load (U.L.) = 40 μ A HIGH/1.6mA LOW.

Military 54LS251



AVAILABLE AS:

- 1) JAN: JM38510/30905BXA
- 2) SMD: 7601601
- 3) 883: 54LS251/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

FUNCT.	PIN ASSIGNMENTS			BURN-IN (COND. A)
	DIL 620-09	FLATS 650-05	LCC 756A-02	
I ₃	1	1	2	VCC
I ₂	2	2	3	VCC
I ₁	3	3	4	VCC
I ₀	4	4	5	VCC
Z	5	5	7	VCC
Z $\bar{}$	6	6	8	OPEN
E \bar{O}	7	7	9	GND
GND	8	8	10	GND
S ₂	9	9	12	GND
S ₁	10	10	13	GND
S ₀	11	11	14	GND
I ₇	12	12	15	VCC
I ₆	13	13	17	VCC
I ₅	14	14	18	VCC
I ₄	15	15	19	VCC
VCC	16	16	20	VCC

**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

NOTES:

1. Input pulse characteristics: PRR \leq 1.0 MHz, $t_r = 15$ ns, $t_f \leq 6.0$ ns.
2. $C_L = 50$ pF $\pm 10\%$ for t_{PLH} , t_{PHL} , t_{PZL} and t_{PZH} tests, $C_L = 15$ pF minimum for t_{PHZ} and t_{PLZ} tests. C_L includes scope probe, wiring and stray capacitance.
3. $R_L = 2.0$ k Ω $\pm 5.0\%$.
4. All diodes are 1N3064 or 1N916.
5. The limits specified for $C_L = 15$ pF, and $C_L = 5.0$ pF are guaranteed but not tested.

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TRUTH TABLE													
\overline{EO}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\overline{Z}	Z
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	H	X	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 (Z) = High Impedance (Off)

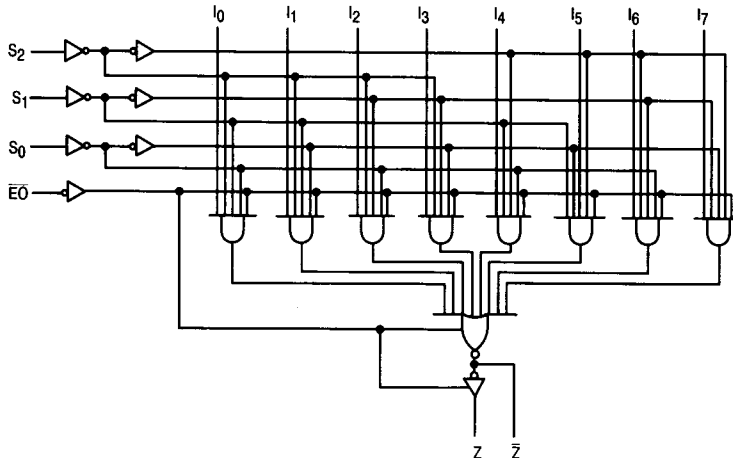
FUNCTIONAL DESCRIPTION

The 'LS251 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of the three Select inputs, S_0, S_1, S_2 . Both assertion and negation outputs are provided. The Output Enable input (\overline{EO}) is active LOW. When it is not activated, the logic function provided at the output is:

$$Z = \overline{EO} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

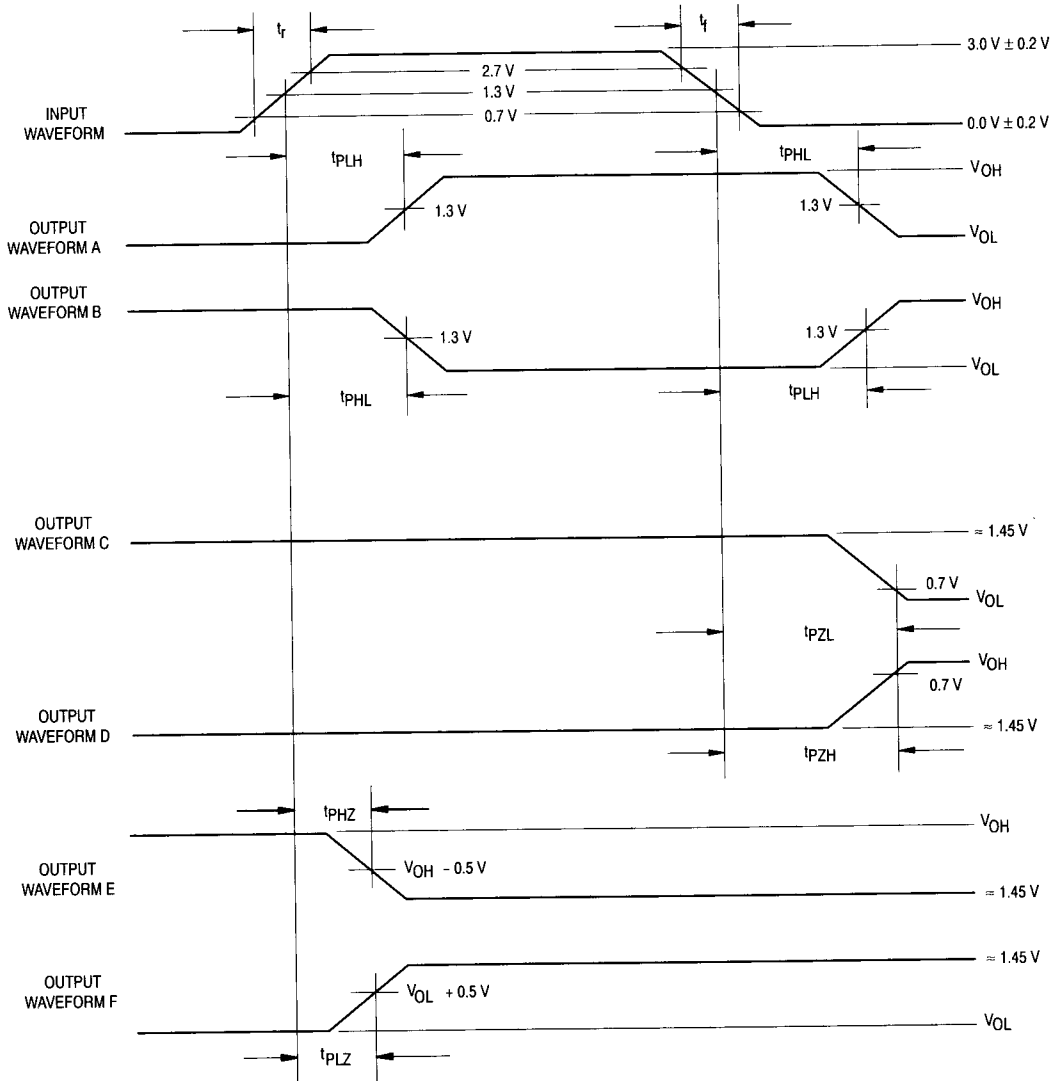
When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows the multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable Voltage.

LOGIC DIAGRAM



54LS251

WAVEFORMS



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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = - 1.0 mA, V _{IH} = 2.0 V, V _{IL} = 0.7 V, S = 0.7 V or 2.0 V, $\bar{E}O$ = 0.7 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V, S = 2.0 V or 0.7 V, $\bar{E}O$ = 0.7 V, V _{IH} = 2.0 V.
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are GND, S = 2.7 V, 5.5 V or GND.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are GND, S = 5.5 V or GND.
I _{IL(I)}	Logical "0" Input Current	- 0.005	- 0.72	- 0.005	- 0.72	- 0.005	- 0.72	mA	V _{CC} = 5.5 V, $\bar{E}O$ = GND, V _{IN} = 0.4 V, S = 5.5 V or GND, other inputs = 5.5 V.
I _{IL($\bar{E}O$)}	Logical "0" Input Current	- 0.002	- 0.15	- 0.002	- 0.15	- 0.002	- 0.15	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), $\bar{E}O$ = 0.4 V.
I _{IL(S)}	Logical "0" Input Current	- 0.1	- 0.34	- 0.1	- 0.34	- 0.1	- 0.34	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs = 5.5 V, $\bar{E}O$ = GND.
I _{OS}	Output Short Circuit Current	- 30	- 130	- 30	- 130	- 30	- 130	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are open, V _{OUT} = GND, $\bar{E}O$ = GND, S = 5.5 V or GND.
I _{OZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, V _{OUT} = 2.7 V, $\bar{E}O$ = 2.0 V, S = 0.7 V or 2.0 V.
I _{OZL}	Output Off Current Low		- 20		- 20		- 20	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, V _{OUT} = 0.4 V, $\bar{E}O$ = 2.0 V, S = 2.0 V or 0.7 V.
I _{CCH}	Power Supply Current		10		10		10	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs).
I _{CCL}	Power Supply Current		12		12		12	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), $\bar{E}O$ = GND.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Data to Z Output	3.0 —	33 28	3.0 —	50 45	3.0 —	50 45	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Data to Z Output	3.0 —	33 28	3.0 —	50 45	3.0 —	50 45	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output Data to Z Output	3.0 —	20 15	3.0 —	30 25	3.0 —	30 25	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PLH2} t _{PLH2}	Propagation Delay /Data-Output Data to Z Output	3.0 —	20 15	3.0 —	30 25	3.0 —	30 25	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PHL5} t _{PHL5}	Propagation Delay /Data-Output Select to Z Output	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PLH5} t _{PLH5}	Propagation Delay /Data-Output Select to Z Output	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PHL6} t _{PHL6}	Propagation Delay /Data-Output Select to Z Output	3.0 —	38 33	3.0 —	57 52	3.0 —	57 52	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PLH6} t _{PLH6}	Propagation Delay /Data-Output Select to Z Output	3.0 —	38 33	3.0 —	57 52	3.0 —	57 52	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PZH1} t _{PZH1}	Propagation Delay /Data-Output Output High-Low	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PZL1} t _{PZL1}	Propagation Delay /Data-Output Output Low-High	3.0 —	45 40	3.0 —	68 63	3.0 —	68 63	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PZH2} t _{PZH2}	Propagation Delay /Data-Output Output High-Low	3.0 —	32 45	3.0 —	48 43	3.0 —	48 43	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PZL2} t _{PZL2}	Propagation Delay /Data-Output Output Low-High	3.0 —	45 40	3.0 —	68 63	3.0 —	68 63	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PHZ1} t _{PHZ1}	Propagation Delay /Data-Output Output High-Low	3.0 —	50 45	3.0 —	75 70	3.0 —	75 70	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PLZ1} t _{PLZ1}	Propagation Delay /Data-Output Output Low-High	3.0 —	35 25	3.0 —	45 40	3.0 —	45 40	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF, R _L = 667 Ω.
t _{PHZ2} t _{PHZ2}	Propagation Delay /Data-Output Output High-Low	3.0 —	60 55	3.0 —	90 85	3.0 —	90 85	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 5.0 pF, R _L = 667 Ω.
t _{PLZ2} t _{PLZ2}	Propagation Delay /Data-Output Output Low-High	3.0 —	35 25	3.0 —	45 40	3.0 —	45 40	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 5.0 pF, R _L = 667 Ω.

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