

## High speed Driver with bootstrapping for dual Power MOSFETs



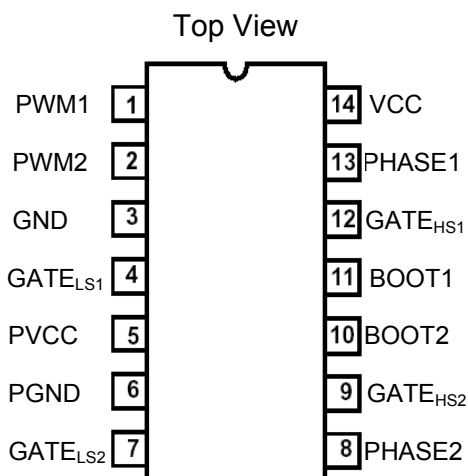
P-DSO-14-3

### Features

- Fast rise and fall times for frequencies up to 2 MHz
- Capable of sinking more than 4 A peak current for lowest switching losses
- Charges the High Side and Low Side MOSFET's gate to 5..12 V according to PVCC setting.
- Adjustable High Side and Low Side MOSFET gate drive voltage via PVCC pin for optimizing ON losses and gate drive losses
- Integrates the bootstrap diode for reducing the part count
- Prevents from cross-conducting by adaptive gate drive control
- High voltage rating on Phase node
- Supports shut-down mode for very low quiescent current through three-state input
- Compatible to standard PWM controller ICs (Intersil, Analog Devices)
- Floating High Side MOSFET drive
- Ideal for multi-phase Desktop CPU supplies on motherboards and VRM's

Type	Package	Marking	Ordering Code
TDA21102	P-DSO-14-3	21102	Q67042-S4244

### Pinout & Description



Number	Name	Description
1	PWM1	Input for the PWM1 controller signal
2	PWM2	Input for the PWM2 controller signal
3	GND	Ground
4	GATE <sub>LS1</sub>	Gate drive output for the N-Channel Low Side MOSFET 1.
5	PVCC	Input to adjust the High Side gate drive
6	PGND	Power ground return for the Low Side Drivers
7	GATE <sub>LS2</sub>	Gate drive output for the N-Channel Low Side MOSFET 2.
8	PHASE2	To be connected to the junction of the High Side and the Low Side MOSFET 2
9	GATE <sub>HS2</sub>	Gate drive output for the N-Channel High Side MOSFET 2.
10	BOOT2	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 2.
11	BOOT1	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 1.
12	GATE <sub>HS1</sub>	Gate drive output for the N-Channel High Side MOSFET 1.
13	PHASE1	To be connected to the junction of the High Side and the Low Side MOSFET 1
14	VCC	Supply Voltage

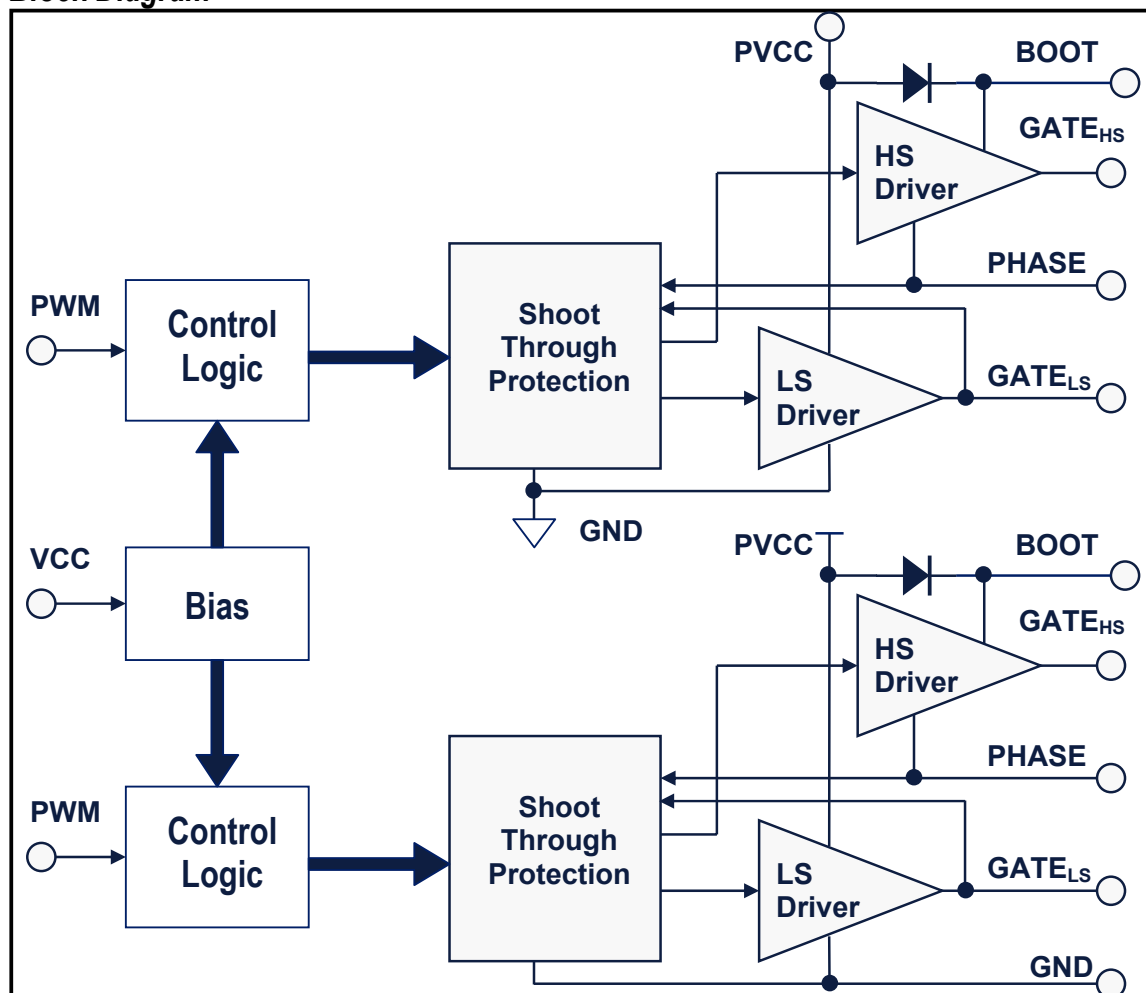
**General Description**

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from input to output, short rise and fall times and the same pin configuration as the HIP6602B. In addition it provides several protection features as well as a shut down mode for efficiency reasons. The high breakdown voltage makes it suitable for mobile applications.

**Target application**

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver's capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM's but also in motor drive and class-D amplifier type applications.

**Block Diagram**



**Absolute Maximum Ratings**

 At  $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Value		Unit	
		Min.	Max.		
Voltage supplied to 'VCC' pin	$V_{VCC}$	-0.3	25	V	
Voltage supplied to 'PVCC' pin	$V_{PVCC}$	-0.3	25		
Voltage supplied to 'PWM' pin	$V_{PWM}$	-0.3	5.5		
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	$V_{BOOT} - V_{PHASE}$	-0.3	25		
Voltage rating at 'PHASE' pin, DC	$V_{PHASE}$	-1	25		
Voltage rating at 'PHASE' pin, $t_{pulse\_max} = 500\text{ns}$ Max Duty Cycle = 2%		-20	30		
Voltage supplied to $GATE_{HS}$ pin referenced to 'PHASE' $T_{pulse\_max} < 100\text{ns}$ , $E < 2\mu\text{J}$	$V_{GATEHS}$	-3.5	$V_{BOOT} + 0.3$		
Voltage supplied to $GATE_{LS}$ pin referenced to 'GND' $T_{pulse\_max} < 100\text{ns}$ , $E < 2\mu\text{J}$	$V_{GATELS}$	-5	$V_{VCC} + 0.3$		
Junction temperature	$T_J$	-25	150		°C
Storage temperature	$T_S$	-55	150		
ESD Rating; Human Body Model			4	kV	
IEC climatic category; DIN EN 60068-1			55/150/56	-	

**Thermal Characteristic**

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-solder joint ( pin 4 )	Rth-JS		40.5		K/W
Thermal resistance, junction-case	Rth-JC		44.7		
Thermal resistance, junction-ambient	Rth-JA		116.2		

**Electrical Characteristic**

 At  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
<b>Supply Characteristic</b>						
Bias supply current	$I_{VCC}$	$f = 1\text{ MHz}$ , NO LOAD $V_{PVCC} = V_{VCC} = 12\text{ V}$		1.3	1.8	mA
Quiescent current	$I_{VCCQ}$	$1.8\text{ V} \leq V_{PWM} \leq 3.0\text{ V}$		3.8	4.9	
Power supply current	$I_{PVCC}$	$f = 1\text{ MHz}$ , NO LOAD $V_{PVCC} = V_{VCC} = 12\text{ V}$		25	33	
Under-voltage lockout		$V_{VCC}$ rising threshold	9.7	10.1	10.5	V
Under-voltage lockout		$V_{VCC}$ falling threshold	7.3	7.6	8.0	V
<b>Input Characteristic</b>						
Current in 'PWM' pin	$I_{PWM\_L}$	$V_{PWM} = 0.4\text{ V}$	-80	115	-150	$\mu\text{A}$
Current in 'PWM' pin	$I_{PWM\_H}$	$V_{PWM} = 4.5\text{ V}$	120	180	250	
Shut down window	$V_{IN\_SHUT}$	$t_{SHUT} > 350\text{ ns}$	1.7		3.1	V
Shut down hold-off time	$t_{SHUT}$	$1.7\text{ V} \leq V_{PWM} \leq 3.1\text{ V}$	100	200	320	ns
PWM pin open	$V_{PWM\_O}$		1.8	2.0	2.2	V
PWM Low level threshold (falling)	$V_{PWM\_L}$				1.4	
PWM High level threshold (rising)	$V_{PWM\_H}$		3.7			
Pulse Width High Side	$t_p$	= Pulse with on PWM pin	40			ns

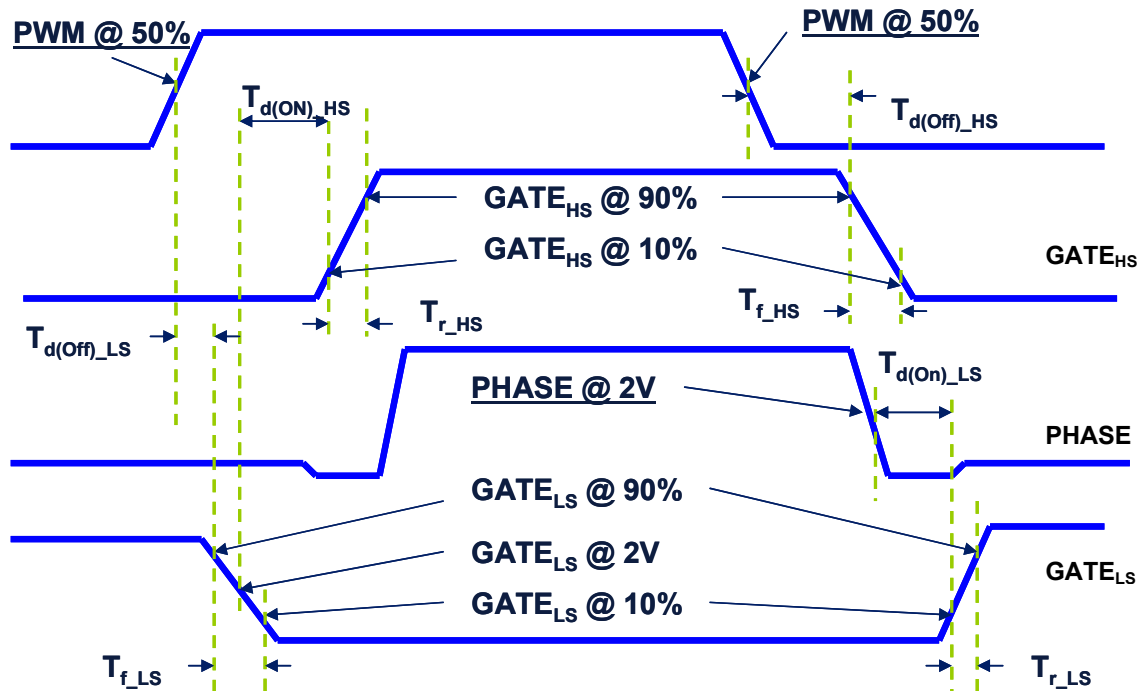
 At  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

<b>Dynamic Characteristic</b>						
Turn-on propagation Delay High Side*	$t_{d(ON)\_HS}$	$P_{PVCC} = V_{VCC} = 12\text{ V}$ $C_{ISS} = 3000\text{ pF}$		18	35	ns
Turn-off propagation delay High Side	$t_{d(OFF)\_HS}$			18	25	
Rise time High Side	$t_r\_HS$			14	28	
Fall time High Side	$t_f\_HS$			14	22	
Turn-on propagation Delay Low Side	$t_{d(ON)\_LS}$			17	23	
Turn-off propagation delay Low Side	$t_{d(OFF)\_LS}$			14	20	
Rise time Low Side	$t_r\_LS$			22	29	
Fall time Low Side	$t_f\_LS$			14	22	

At  $T_j = 125\text{ °C}$ , unless otherwise specified

Dynamic Characteristic					
Turn-on propagation Delay High Side*	$t_{d(ON)_{HS}}$	$P_{PVCC} = V_{VCC} = 12\text{ V}$ $C_{ISS} = 3000\text{ pF}$		22	ns
Turn-off propagation delay High Side	$t_{d(OFF)_{HS}}$			22	
Rise time High Side	$t_{r_{HS}}$			16	
Fall time High Side	$t_{f_{HS}}$			16	
Turn-on propagation Delay Low Side	$t_{d(ON)_{LS}}$			20	
Turn-off propagation delay Low Side	$t_{d(OFF)_{LS}}$			18	
Rise time Low Side	$t_{r_{LS}}$			23	
Fall time Low Side	$t_{f_{LS}}$			16	

**Measurement Timing diagram**



**Operating Conditions**

At T<sub>j</sub> = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pin	V <sub>VCC</sub>		10.8		13.2	V
Voltage supplied to 'PVCC' pin	V <sub>PVCC</sub>		5		13.2	V
Input signal transition frequency	f		0.1		2	MHz
Power dissipation	P <sub>TOT</sub>	T <sub>A</sub> = 25 °C, T <sub>J</sub> = 125 °C		0.9		W
Junction temperature	T <sub>J</sub>		-25		150	°C

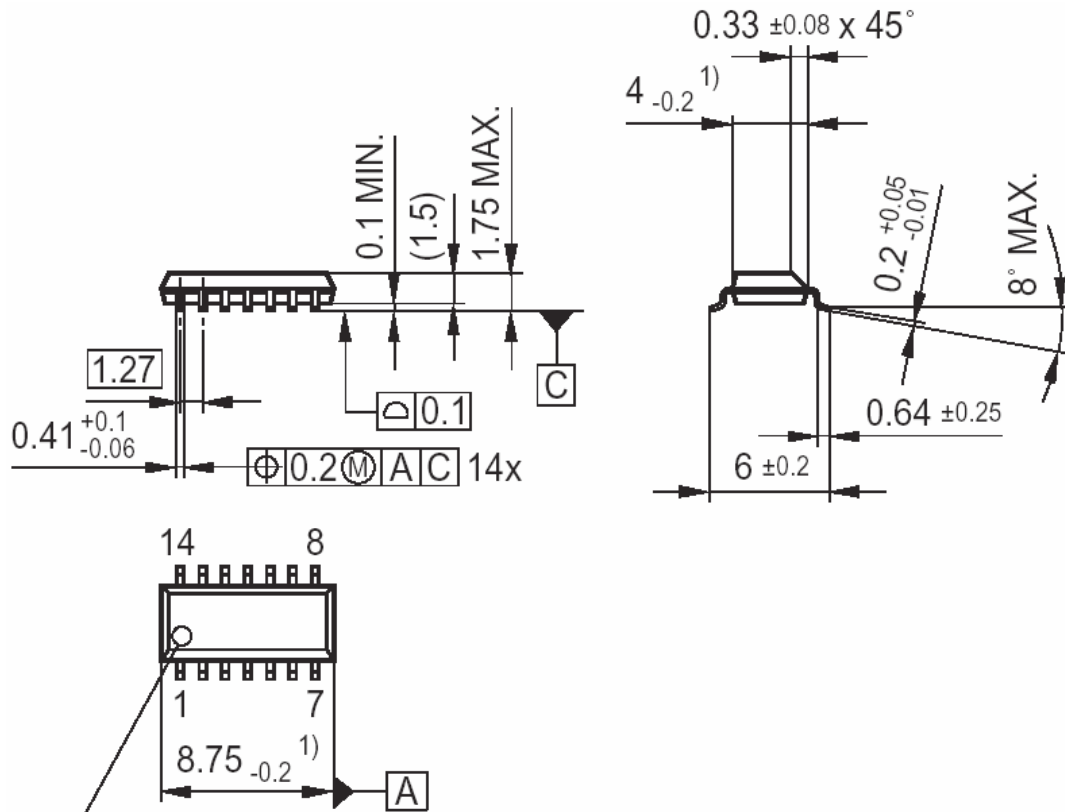
At T<sub>j</sub> = 25 °C, unless otherwise specified

Parameter	Conditions	Values			Unit	
		Min.	Typ.	Max.		
<b>Output Characteristic High Side (HS) and Low Side (LS), ensured by design</b>						
Output Resistance	HS; Source	P <sub>PVCC</sub> = V <sub>VCC</sub> = 12 V I <sub>HS_SRC</sub> = 2 A		1 <sup>(1)</sup>		Ω
	HS; Sink	V <sub>VCC</sub> = 12 V, P <sub>PVCC</sub> = 5V		1	1.3	Ω
	HS; Sink	P <sub>PVCC</sub> = V <sub>VCC</sub> = 12 V		0.9	1.2	Ω
	LS; Source	P <sub>PVCC</sub> = V <sub>VCC</sub> = 12 V I <sub>HS_SRC</sub> = 2 A		1.4 <sup>(2)</sup>		Ω
	LS; Sink	V <sub>VCC</sub> = 12 V, P <sub>PVCC</sub> = 5V		1	1.3	Ω
	LS; Sink	P <sub>PVCC</sub> = V <sub>VCC</sub> = 12 V		1	1.25	Ω
Peak output-current	HS; Source	P <sub>PVCC</sub> = V <sub>VCC</sub> = 12 V	4			A
	HS; Sink	t <sub>P_HS</sub> / Pulse < 20 ns	4			
	LS; Source	t <sub>P_LS</sub> / Pulse < 40 ns	4			
	LS; Sink	D <sub>HS</sub> < 2%, D <sub>LS</sub> < 4%	4			

<sup>1</sup> Incremental resistance V<sub>BOOT</sub>-V<sub>HS</sub>=4.3V @ I<sub>SOURCE</sub>=2A

<sup>2</sup> Incremental resistance V<sub>VCC</sub>-V<sub>LS</sub>=4.4V @ I<sub>SOURCE</sub>=2A

**Package Drawing P-DSO-14-3**



Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

**Layout Footprints**



e	A	L	B
1,27 mm	5,69 mm	1,31 mm	0,65 mm



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