

FSTD3306

2-Bit Low-Power Bus Switch with Level Shifting

Features

- Typical 3Ω switch resistance at 5.0V V_{CC} , $V_{IN} = 0V$
- Level shift facilitates 5V to 3.3V interfacing
- Minimal propagation delay through the switch
- Power down high impedance input/output
- Zero bounce in flow-through mode
- TTL compatible active LOW control inputs
- Control inputs are over-voltage tolerant

Description

The FSTD3306 is a 2-bit ultra high-speed CMOS FET bus switch with enhanced level-shifting circuitry and TTL-compatible active LOW control inputs. The low on resistance of the switch allows inputs to be connected to outputs with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 2-bit switch with independent bus-enable (\overline{BE}) controls. When \overline{BE} is LOW, the switch is ON and Port A is connected to Port B. When \overline{BE} is HIGH, the switch is OPEN and a high-impedance state exists between the two ports. Reduced voltage drive to the gate of the FET switch permits nominal level shifting of 5V to 3V through the switch. Control inputs tolerate voltages up to 5.5V independent of V_{CC} .

Ordering Information

Part Number	Top Mark	Package	Pb-Free	Operating Temperature Range	Packing Method
FSTD3306MTCX	FD3306	8-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Yes	-40 to +85°C	Tape & Reel
FSTD3306MTC	FD3306	8-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Yes	-40 to +85°C	Tube
FSTD3306L8X	TD	8-Lead MicroPak™	Yes	-40 to +85°C	5000 units on Reel

Logic Diagram

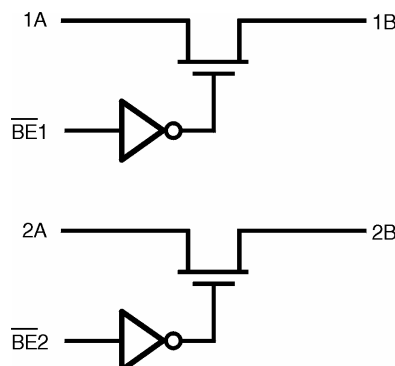


Figure 1. Logical Connections for the FSTD3306

Connections Diagram

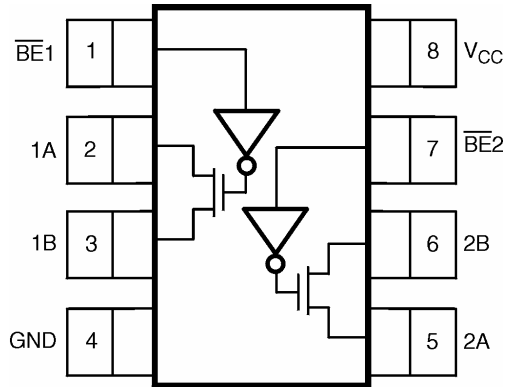


Figure 2. TSSOP Pin Outs (Top View)

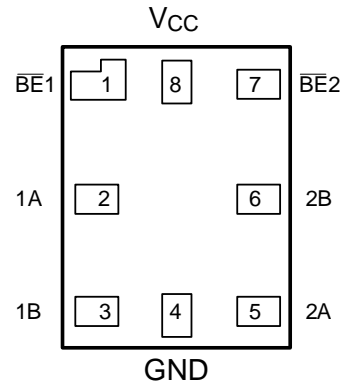


Figure 3. MicroPak Pin Outs (Top View)

Pin Definitions

Pin	Description
A	Bus A switch I/O
B	Bus B switch I/O
\overline{BE}	Bus enable input

Function Table

Bus Enable Input (\overline{BE})	Function
LOW Logic Level	B connected to A
HIGH Logic Level	Disconnected

Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
V _{CC}	Supply Voltage		- 0.5		+ 7.0	V
V _S	DC Switch Voltage		- 0.5		+ 7.0	V
V _{IN}	DC Output Voltage ⁽¹⁾		- 0.5		+ 7.0	V
I _{IK}	DC Input Diode Current	V _{IN} < 0V		- 50		mA
I _{OUT}	DC Output Sink Current			128		mA
I _{CC} /I _{GND}	DC V _{CC} or Ground Current			± 100		mA
T _{STG}	Storage Temperature Range		- 65		+150	°C
T _J	Junction Temperature	under Bias		+ 150		°C
T _L	Junction Lead Temperature	(Soldering, 10 Seconds)		+ 260		°C
P _D	Power Dissipation	at +85°C		250		mW

Notes:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions⁽²⁾

Symbol	Parameter	Condition	Min.	Typ.	Max	Unit
V _{CC}	Supply Voltage		4.5		5.5	V
V _{IN}	Control Input Voltage		0.0		5.5	V
V _{IN}	Switch Input Voltage		0.0		5.5	V
V _{OUT}	Switch Output Voltage		0.0		5.5	V
T _A	Operating Temperature		- 40		+ 85	°C
t _r , t _f	Input Rise and Fall Time	Control Input	0		5	ns/V
		Switch I/O	0		DC	ns/V
Θ _{JA}	Thermal Resistance			250		°C/W

Notes:

2. Unused logic inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Ambient temperature (T_A) is -40°C to $+85^{\circ}$ unless otherwise specified.

Symbol	Parameters	Conditions	V_{CC} (V)	Min.	Typ.	Max.	Unit
V_{IK}	Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$	4.5			-1.2	V
V_{IH}	HIGH-Level Input Voltage		4.5-5.5	2.0			V
V_{IL}	LOW-Level Input Voltage		4.5-5.5			0.8	V
V_{OH}	HIGH-Level Output Voltage	$V_{IN} = V_{CC}$	4.5-5.5		(3)		V
I_{IN}	Input Leakage Current	$0 \leq V_{IN} \leq 5.5\text{V}$	5.5			± 1.0	μA
I_{OFF}	Power OFF Leakage Current	$0 \leq A, B \leq V_{CC}$	5.5			± 1.0	μA
R_{ON}	Switch On Resistance ⁽⁴⁾	$V_{IN} = 0\text{V}, I_{IN} = 64\text{mA}$	4.5		3	7	Ω
		$V_{IN} = 0\text{V}, I_{IN} = 30\text{mA}$	4.5		3	7	Ω
		$V_{IN} = 2.4\text{V}, I_{IN} = 15\text{mA}$	4.5		15	50	Ω
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ $\overline{BE} 1 = \overline{BE} 2 = \text{GND}$	5.5		1.1	1.5	mA
		$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ $\overline{BE} 1 = \overline{BE} 2 = V_{CC}$	5.5			10	μA
ΔI_{CC}	Increase in I_{CC} per Input ⁽⁵⁾	$V_{IN} = 3.4\text{V}, I_O = 0$, one control input only, other $\overline{BE} = V_{CC}$	5.5		1	2.5	mA

Notes:

- For typical DC characteristics, see Figures 7-9.
- Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.
- Increase per TTL-driven input ($V_{IN} = 3.4\text{V}$, control input only). A and B pins do not contribute to I_{CC} .

AC Electrical Characteristics

Ambient temperature (T_A) is -40°C to $+85^{\circ}$ and $C_L = 50\text{pF}$, $R_U = R_D = 500\Omega$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	Min.	Typ.	Max.	Unit
t_{PHL}, t_{PLH}	Propagation Delay Bus-to-Bus ⁽⁶⁾	$V_I = \text{OPEN}$	4.5 - 5.5			0.25	ns
t_{PZL}, t_{PZH}	Output Enable Time	$V_I = 7\text{V}$ for t_{PZL} , $V_I = 0\text{V}$ for t_{PZH}	4.5 - 5.5	1.0	3.5	5.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	$V_I = 7\text{V}$ for t_{PLZ} , $V_I = 0\text{V}$ for t_{PHZ}	4.5 - 5.5	0.8	3.5	4.8	ns

Notes:

- This parameter is guaranteed. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance). The specified limit is calculated on this basis.

Capacitance

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CC} = 0\text{V}$	2.5	pF
$C_{I/O} (\text{OFF})$	Port OFF Capacitance	$V_{CC} = 5.0\text{V} = \overline{BE}$	6	pF
$C_{I/O} (\text{ON})$	Port ON Capacitance	$V_{CC} = 5.0\text{V}, \overline{BE} = 0\text{V}$	12	pF

AC Loading and Waveforms

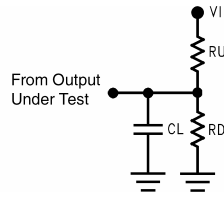


Figure 4. AC Test Circuit. Input driven by 50Ω source-terminated in 50Ω. C_L includes load and stray capacitance. Input PRR = 1.0 MHz; $T_W = 500\text{ns}$.

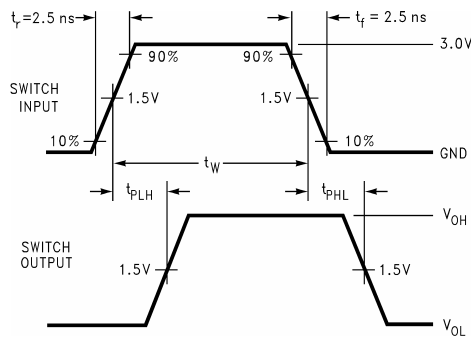


Figure 5. AC Waveform

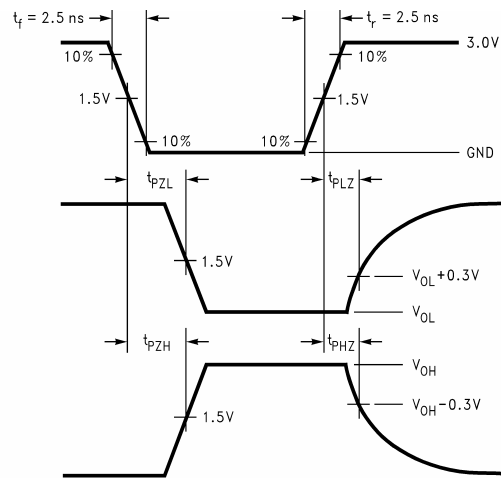


Figure 6. AC Waveform

DC Characteristics

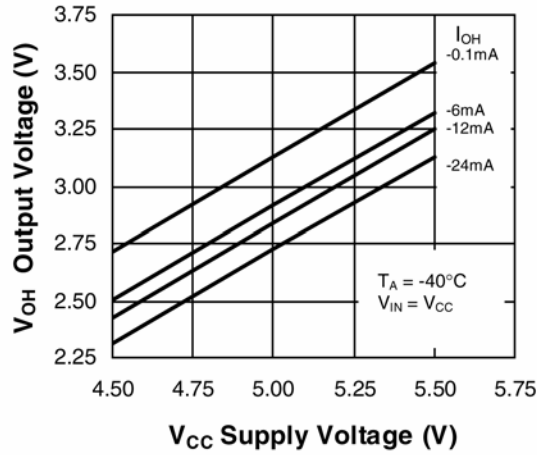


Figure 7. Typical High-Level Output Voltage vs. Supply Voltage ($T_A = -40^\circ\text{C}$, $V_{IN} = V_{CC}$)

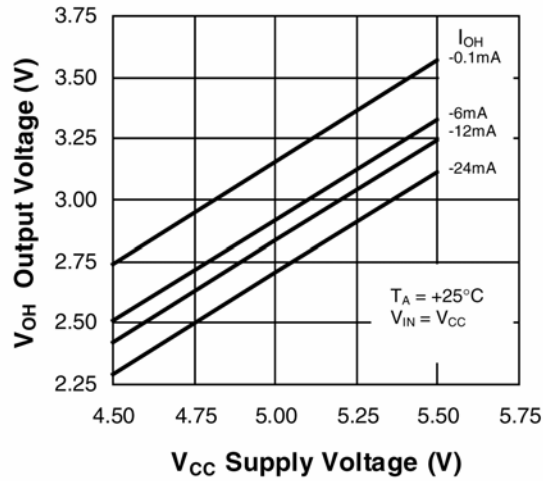


Figure 8. Typical High-Level Output Voltage vs. Supply Voltage ($T_A = 25^\circ\text{C}$, $V_{IN} = V_{CC}$)

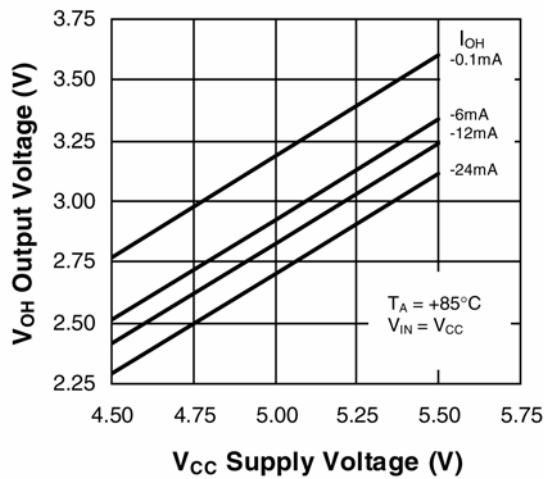


Figure 9. Typical High-Level Output Voltage vs. Supply Voltage ($T_A = 85^\circ\text{C}$, $V_{IN} = V_{CC}$)

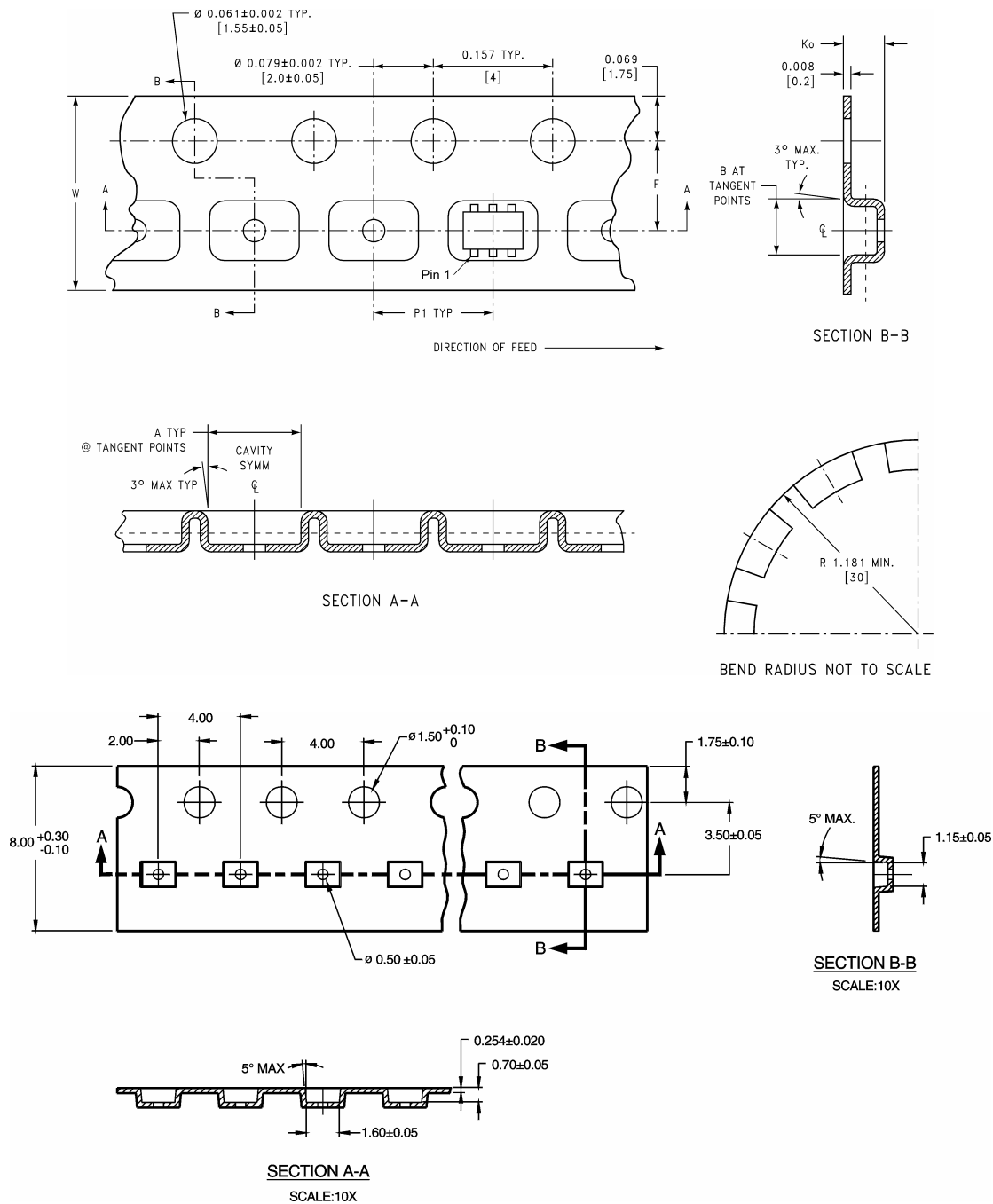
Tape and Reel Specifications

Tape Format MicroPak

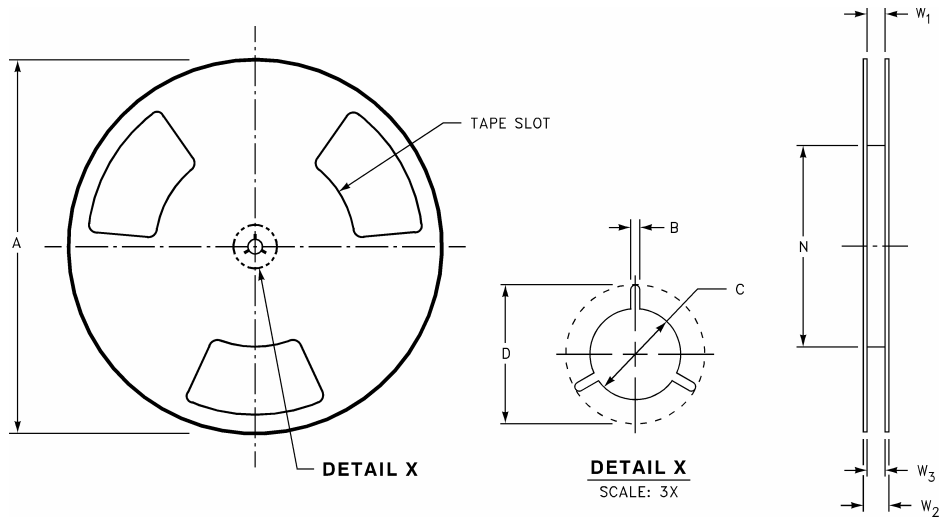
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



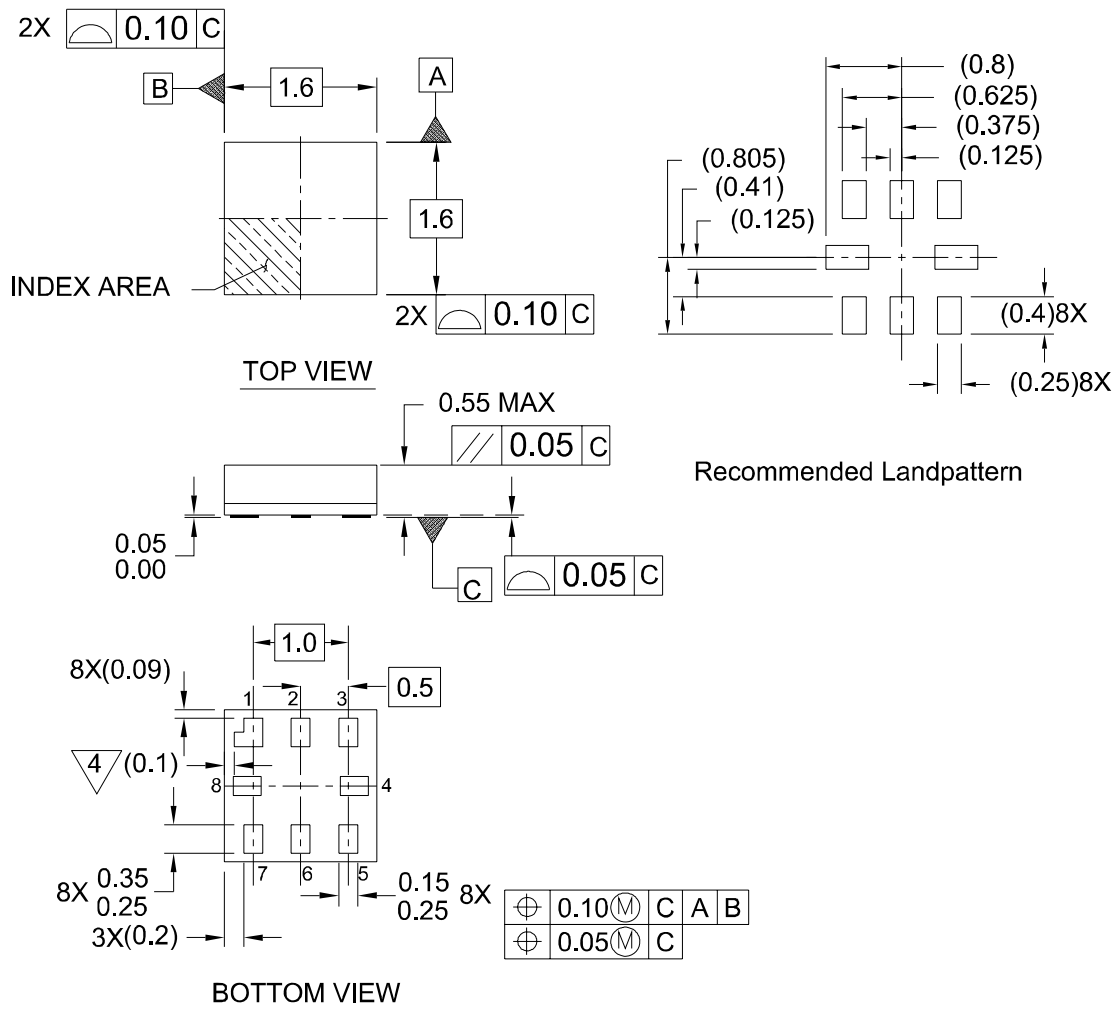
Reel Dimensions



Tape Size	A	B	C	D	N	W1	W2	W23
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	.0331 +0.059 / -0.000 (8.40 +1.50 / -0.00)	0.567 (14.40)	W1 +0.078 / -0.039 (W1 +2.00 / -1.00)

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

Figure 10. 8-Lead MicroPak, 1.6mm-wide Package

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

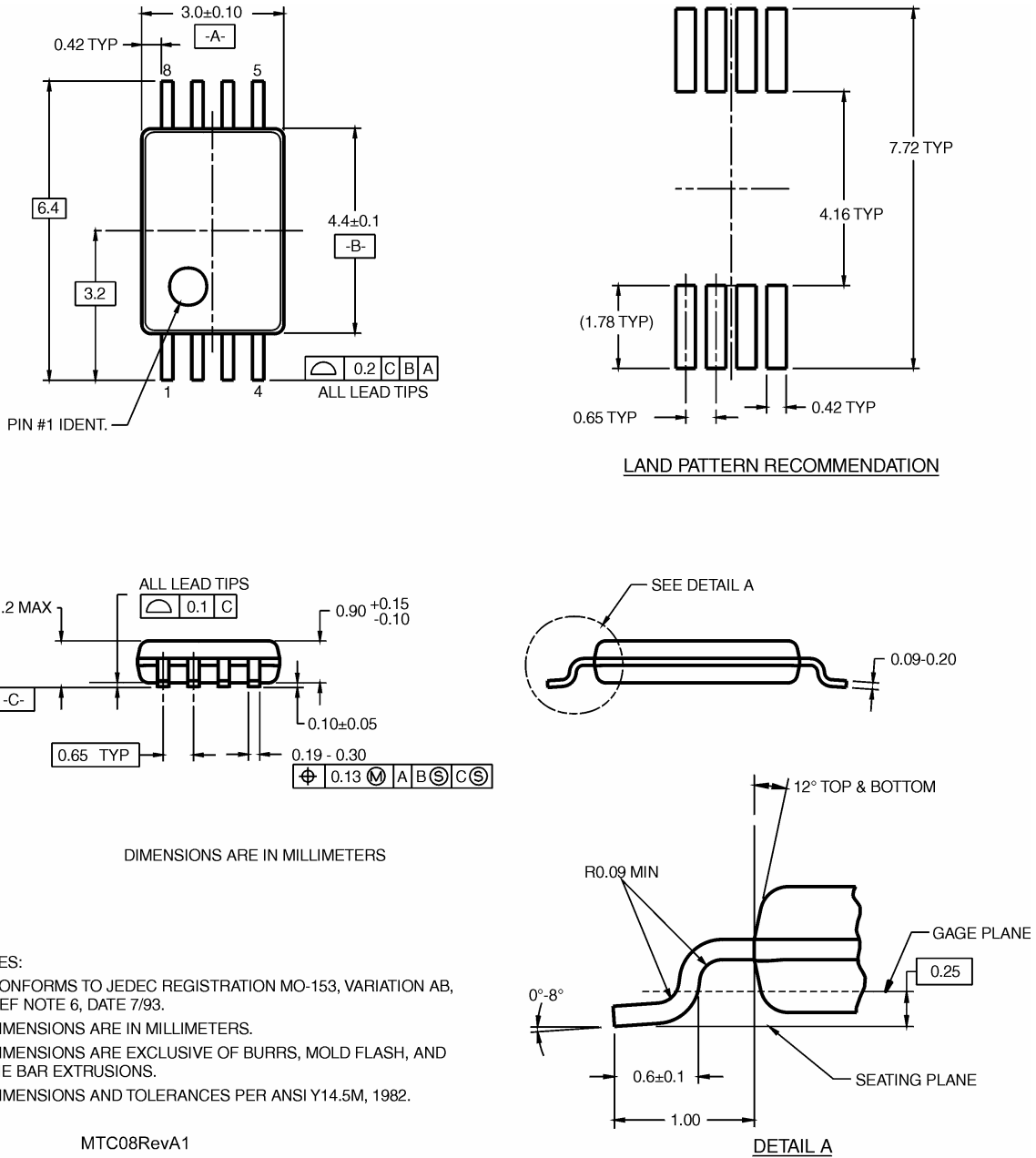


Figure 11. 8-Lead Thin Shrink Small Outline (TSSOP), JEDEC MO-153, 4.4mm-wide Package

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	GlobalOptoisolator™	OCXPro™	μSerDes™	TinyBuck™
ActiveArray™	GTO™	OPTOLOGIC®	SILENT SWITCHER®	TinyLogic®
Bottomless™	HiSeC™	OPTOPLANAR™	SMART START™	TINYOPTO™
Build it Now™	I ² C™	PACMAN™	SPM™	TinyPower™
CoolFET™	i-Lo™	POP™	Stealth™	TinyPWM™
CROSSVOLT™	ImpliedDisconnect™	Power247™	SuperFET™	TruTranslation™
DOME™	IntelliMAX™	PowerEdge™	SuperSOT™-3	UHC™
EcoSPARK™	ISOPLANAR™	PowerSaver™	SuperSOT™-6	UltraFET®
E ² CMOS™	LittleFET™	PowerTrench®	SuperSOT™-8	UniFET™
EnSigna™	MICROCOUPLER™	QFET®	SyncFET™	VCX™
FACT™	MicroFET™	QS™	TCM™	Wire™
FACT Quiet Series™	MicroPak™	QT Optoelectronics™	TinyBoost™	
FAST®	MICROWIRE™	Quiet Series™		
FASTr™	MSX™	RapidConfigure™	Across the board. Around the world.™	
FPS™	MSXPro™	RapidConnect™	Programmable Active Droop™	
FRFET™	OCX™	ScalarPump™	The Power Franchise®	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I20