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## MAX77752

## Multichannel Integrated Power Management IC

### General Description

The MAX77752 is a highly-integrated power management solution including three step-down converters, a low-dropout linear regulator, two external regulators enable outputs, two dedicated load switch controllers, and an inrush-current limiter which can be configured as a third load switch controller using OTP. The MAX77752 provides a combination of high-performance power management components, high-accuracy monitoring, and a customized top-level controller that results in an efficient, size optimized solution.

The 40-pin, 5mm x 5mm x 0.8mm, 0.4mm pitch TQFN package is ideal for space constrained applications.

Numerous factory programmable options allow the device to be tailored for many variations of the end application.

### Applications

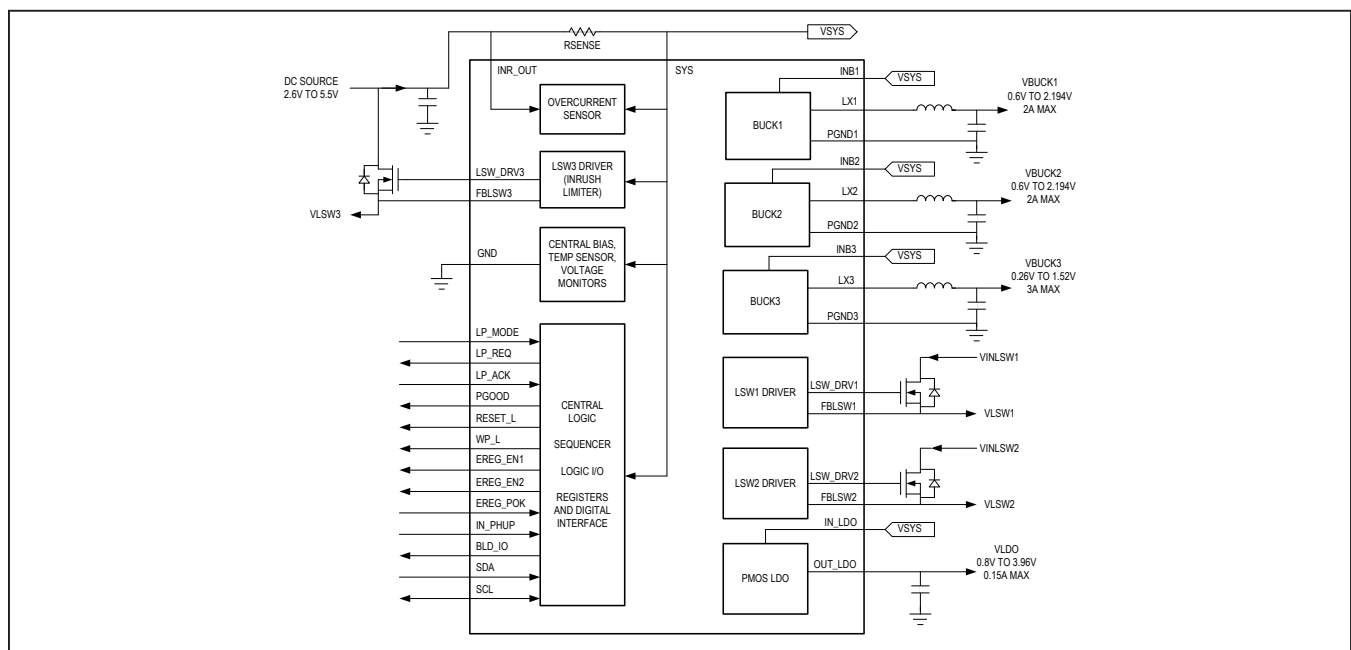
- Solid-State Drive Systems
- Handheld Devices
- Gaming Consoles
- Drones
- Automation Systems
- Cameras

### Benefits and Features

- Highly Integrated
  - Three Buck Regulators
    - Integrated High-Accuracy Brownout Comparators
  - One Low-Dropout Linear Regulator
    - Low-Input Voltage
  - Two Dedicated Load Switch Controllers
  - One Inrush-Current Limiter, Configurable to be Load Switch 3 Controller Using OTP
  - Two External Regulator Enable Outputs
  - Voltage Monitor for Backup Power Control
- Highly Flexible and Configurable
  - I<sup>2</sup>C-Compatible Interface
  - Factory OTP Options Available
  - Flexible Power Sequencer
  - Configurable Sleep-State Control
- Small Size
  - 40-Pin, 5mm x 5mm x 0.8mm, 0.4mm Pitch TQFN
  - 70mm<sup>2</sup> Total Solution Size

*Ordering Information* appears at end of data sheet.

### Simplified Block Diagram



## Absolute Maximum Ratings

### Top

IN_DRV to GND	-0.3V to +16.0V
IN_SNS to GND (Note 1)	-0.3V to +6.0V
INR_OUT to GND	-0.3V to +6.0V
SYS to GND	-0.3V to +6.0V
IN_PHUP to GND	-0.3V to +6.0V
RESET_L to GND	-0.3V to $V_{SYS}+0.3V$
LP_REQ to GND	-0.3V to $V_{SYS}+0.3V$
LP_ACK to GND	-0.3V to $V_{SYS}+0.3V$
LP_MODE to GND	-0.3V to $V_{SYS}+0.3V$
WP_L to GND (Note 2)	-0.3V to $V_{H\_INT}$
PGOOD to GND (Note 2)	-0.3V to $V_{H\_INT}$
EREG_EN1 to GND (Note 2)	-0.3V to $V_{H\_INT}$
EREG_EN2 to GND	-0.3V to 6.0V
EREG_POK to GND	-0.3V to $V_{SYS}+0.3V$
BLD_IO to GND (Note 2)	-0.3V to +6.0V
WP_L Sink Current	35mA
RESET_L Sink Current	35mA
PGOOD Sink Current	35mA
EREG_EN1 Sink Current	35mA
EREG_EN2 Sink Current	35mA
LP_REQ Sink Current	35mA
DGND to GND	-0.3V to +0.3V

### LDO

IN_LDO to GND	-0.3V to +6.0V
OUT_LDO to GND	-0.3V to $V_{IN\_LDO}+0.3V$

### Buck

INB1, INB2, INB3 to SYS	-0.3V to +0.3V
INB1 to PGND1	-0.3V to +6.0V
INB2 to PGND2	-0.3V to +6.0V
INB3 to PGND3	-0.3V to +6.0V
LX1 to PGND1 (Note 3)	-0.3V to $V_{INB1}+0.3V$
LX2 to PGND2 (Note 3)	-0.3V to $V_{INB2}+0.3V$
LX3 to PGND3 (Note 3)	-0.3V to $V_{INB3}+0.3V$
LX1, LX2 RMS Current per pin ( $T_J = +110^\circ C$ )	
(RMS current per pin ( $T_J = +110^\circ C$ ))	1.7A
LX3 RMS Current per pin ( $T_J = +110^\circ C$ )	
(RMS current per pin ( $T_J = +110^\circ C$ ))	3.0A
FBB1, FBB2, FBB3 to GND	-0.3V to $V_{SYS}+0.3V$
PGND1, PGND2, PGND3 to GND	-0.3V to +0.3V

### I<sup>2</sup>C

SDA, SCL to GND	-0.3V to $V_{IN\_VIO\_I2C}+0.3V$
SDA Sink Current	35mA

### Load Switch

LSW_DRV1 to GND	-0.3V to +16.0V
LSW_DRV2 to GND	-0.3V to +16.0V
FBLSW1 to GND	-0.3V to $V_{SYS}+0.3V$
FBLSW2 to GND	-0.3V to $V_{SYS}+0.3V$

### Continuous Power Dissipation (Multilayer Board)

$T_A = +70^\circ C$ , derate 35.70mW/ $^\circ C$	
above $+70^\circ C$	mW to 2857.1mW
Operating Temperature Range	$-40^\circ C$ to $+85^\circ C$
Junction Temperature	$+150^\circ C$
Storage Temperature Range	$-40^\circ C$ to $+150^\circ C$
Soldering Temperature (reflow)	$+260^\circ C$

**Note 1:** IN\_SNS voltage ramp rates greater than  $2.8V/\mu s$  trigger the internal ESD device and should be avoided. The ESD device recovers if exposed to an excessive ramp rate.

**Note 2:**  $V_{H\_INT}$  is the maximum voltage of  $V_{SYS}$  and  $V_{IN\_PHUP}$ .

**Note 3:** The specified voltage limitation is for steady state conditions. Dead times of a few nano seconds exist during the dynamic BUCK regulator transitions from inductor charging to inductor discharging and vice versa. These dead times allow internal clamping diodes to PGNDx and INBx to forward bias ( $V_f \sim 1V$ ). When the LXx waveform is observed on a high-bandwidth oscilloscope ( $\geq 100MHz$ ), the LXx transition edges are commonly seen with 1.5V spikes. These spikes are due to (1) the internal clamping diode forward voltage and (2) the high rate of current change through the current loop's inductance ( $V = L \times di/dt$ ). Designs must follow the recommended printed circuit board (PCB) layout in order to minimize this current loop's inductance.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### TQFN

<b>PACKAGE CODE</b>	<b>T4055+1C</b>
Outline Number	<a href="#">21-0140</a>
Land Pattern Number	<a href="#">90-0016</a>
<b>Thermal Resistance, Single-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	45°C/W
Junction to Case ( $\theta_{JC}$ )	2°C/W
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	28°C/W
Junction to Case ( $\theta_{JC}$ )	2°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics—Global Resources

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY CURRENT</b>						
OFF State Quiescent Current	$I_{QSYS\_OFF}$	$V_{SYSUVLO} < V_{SYS} < V_{SYS\_RESET}$ (rising), $OTP\_INT\_PU = 1$ , all regulators are disabled. This includes any central bias currents disabled (EREG_EN1 pulled to $V_{SYS}$ )		86	135	$\mu A$
DEVSLP State Quiescent Current	$I_{QSYS\_DEVSLP}$	$V_{SYS} = 3.3V$ , $V_{SYS} > V_{SYS\_RESET}$ , $OTP\_INT\_PU = 0$ , PMIC in DEVSLP State, Buck2, Buck3, LDO enabled in low-power mode. No load on all regulators. All other regulators disabled		70	125	$\mu A$
		$V_{SYS} = 5V$ , $V_{SYS} > V_{SYS\_RESET}$ , $OTP\_INT\_PU = 0$ , PMIC in DEVSLP state, Buck2, Buck3, LDO enabled in low-power mode. No load on all regulators. All other regulators disabled		90	155	
Buck Quiescent Supply Current	$I_{QSYS\_BUCK}$	$V_{SYS} = 5V$ , $V_{SYS} > V_{SYS\_RESET}$ , all bucks enabled in normal-power mode and skip mode		233	420	$\mu A$

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BIAS AND REFERENCE CURRENT GENERATOR</b>						
Operating Voltage Range	$V_{SYS}$		2.6		5.5	V
Quiescent Supply Current	$I_{QCBRG}$	$V_{SYS} > V_{SYSUVLO}$ (rising)		25		$\mu A$
Shutdown Supply Current		$V_{SYS} < V_{SYSUVLO}$ (falling)		0.1		$\mu A$
Bias Enable time	$t_{BIASOK}$			100		$\mu s$
<b>POR COMPARATOR (INTERNAL)</b>						
Quiescent Supply Current	$I_{QSYS\_POR}$			1		$\mu A$
POR Undervoltage-Lockout Threshold	$V_{POR}$	$V_{SYS}$ falling		1.33		V
POR Threshold Hysteresis	$V_{HYS\_POR}$	$V_{SYS}$ rising		160		mV
Response Time		100mV overdrive		300		$\mu s$
POR to UVLO Delay	$t_{PORUVLO}$	$V_{SYS}$ rising across POR (1V to 2V)		100		$\mu s$
		$V_{SYS}$ falling across POR		50		
<b>SYS UNDERVOLTAGE-LOCKOUT COMPARATOR</b>						
Quiescent Supply Current	$I_{QSYS\_UVLO}$			1		$\mu A$
SYS Undervoltage-Lockout Threshold	$V_{SYSUVLO}$	$V_{SYS}$ falling	2.00	2.10	2.25	V
SYS Undervoltage-Lockout Hysteresis	$V_{INUVLO\_HYS}$			400		mV
SYS Undervoltage-Lockout Response Time	$t_{SYSUVLO}$	100mV overdrive, falling edge		150		$\mu s$
<b>SYS RESET COMPARATOR</b>						
Quiescent Supply Current	$I_{QSYS\_RESET}$			3		$\mu A$
Reset Falling Threshold Range	$V_{SYS\_RESET}$	Programmed by SYSRST[3:0]	2650		4150	mV
Reset Threshold Step Size				100		mV
Reset Threshold Hysteresis Range	$V_{SYSRESET\_HYS}$	Programmed by SYSRSTHYS[1:0]	150		300	mV
Reset Threshold Hysteresis Step Size				50		mV
Reset Comparator Response Time	$t_{SYSRESET}$			5		$\mu s$
Reset Comparator Accuracy		SYSRSTTH[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF	-2.5		+2.5	%

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SYS BROWNOUT COMPARATOR</b>						
Brownout Falling Threshold Range	$V_{SYS\_BO}$	Programmed by SYSBOTH[3:0]	2800		4300	mV
Brownout Threshold Step Size				100		mV
Brownout Threshold Hysteresis Range	$V_{SYS\_BO\_HYS}$	Programmed by SYSBOHYS[1:0]	150		300	mV
Brownout Threshold Hysteresis Step Size				50		mV
Brownout Comparator Response Time	$t_{SYSBO}$	SYS_BO_PR[1:0] = 0b00 (fast), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s		1.04		$\mu$ s
		SYS_BO_PR[1:0] = 0b01 (med-fast), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s		1.14		
		SYS_BO_PR[1:0] = 0b10 (med-slow), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s		1.30		
		SYS_BO_PR[1:0] = 0b11 (slow), PMIC not in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s		1.68		
Brownout Comparator Response Time (DEVSLP)	$t_{SYSBO}$	PMIC in DEVSLP state, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s		3.53		$\mu$ s
Quiescent Supply Current	$I_{QSYS\_BO}$	SYS_BO_PR[1:0] = 0b00 (fast), PMIC not in DEVSLP state		13.4		$\mu$ A
		SYS_BO_PR[1:0] = 0b01 (med-fast), PMIC not in DEVSLP state		10.4		
		SYS_BO_PR[1:0] = 0b10 (med-slow), PMIC not in DEVSLP state		7.4		
		SYS_BO_PR[1:0] = 0b11 (slow), PMIC not in DEVSLP state		4.4		
Quiescent Supply Current (DEVSLP)	$I_{QSYS\_BO}$	PMIC in DEVSLP state		1.3		$\mu$ A
Brownout Comparator Accuracy		SYSBO[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF, PMIC is not in DEVSLP state	-2.5		+2.5	%
Brownout Comparator Accuracy (DEVSLP)		SYSBO[3:0] = 0x0, 0x1, 0x5, 0xA, 0xF, PMIC is in DEVSLP state	-2.5		+2.5	%
Brownout Timer Period	$t_{BO}$	T_BO_EN = 1		100		ms

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OSCILLATOR</b>						
Clock Frequency	CLK32K	$V_{SYS} = 5V$		31.5		kHz
Oscillator Tolerance		$V_{SYS} = 3.3V$	-10		+10	%
		$V_{SYS} = 5V$	-10		+10	
<b>WP_L OUTPUT (OPEN DRAIN)</b>						
WP_L Output-Voltage Low	$V_{OL}$	$I_{SINK} = 2mA$			0.4	V
WP_L Open Leakage Current		$V_{SYS} = V_{WP\_L} = 5.5V$ , $T_A = +25^\circ C$ , OTP_INT_PU[0] = 0b0		0.001	1	$\mu A$
		$V_{SYS} = V_{WP\_L} = 5.5V$ , $T_A = +85^\circ C$ , OTP_INT_PU[0] = 0b0		0.01		
WP_L Falling Edge Time		$C_{WP\_L} = 25pF$ , $V_{WP\_L} = 1.8V \geq 0$		25		ns
WP_L Output Deassert Delay Time	$t_{WPDLY}$	WP_L_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		0		$\mu s$
		WP_L_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		WP_L_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		WP_L_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
WP_L Output Assert Delay Time				0		$\mu s$
WP_L Pullup Resistance	$R_{PU\_WP\_L}$	Pulled up to $V_{IN\_VIO}$ , OTP_INT_PU[0] = 0b1	50	100	170	k $\Omega$
<b>RESET_L OUTPUT (OPEN DRAIN)</b>						
RESET_L Output-Voltage Low	$V_{OL}$	$I_{SINK} = 2mA$			0.4	V
RESET_L Open Leakage Current		$V_{SYS} = V_{RESET\_L} = 5.5V$ , $T_A = +25^\circ C$ , OTP_INT_PU[0] = 0b0		0.001	1	$\mu A$
		$V_{SYS} = V_{RESET\_L} = 5.5V$ , $T_A = +85^\circ C$ , OTP_INT_PU[0] = 0b0		0.01		
RESET_L Falling Edge Time		$C_{RESET\_L} = 25pF$ , $V_{RESET\_L}$ falling from $1.8V \geq 0$		25		ns

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET_L Output Deassert Delay Time	$t_{RSTDLY}$	RST_L_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		0		$\mu s$
		RST_L_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		RST_L_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		RST_L_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
RESET_L Output Assert Delay Time				0		$\mu s$
RESET_L Pullup Resistance	$R_{PU\_RESET\_L}$	Pulled up to $V_{IN\_VIO}$ , OTP_INT_PU[0] = 0b1	50	100	170	$k\Omega$
<b>PGOOD OUTPUT (OPEN DRAIN)</b>						
PGOOD Output-Voltage Low	$V_{OL}$	$I_{SINK} = 2mA$			0.4	V
PGOOD Open Leakage Current		$V_{SYS} = V_{PGOOD} = 5.5V$ , $T_A = +25^{\circ}C$ , OTP_INT_PU[0] = 0b0		0.001	1	$\mu A$
		$V_{SYS} = V_{PGOOD} = 5.5V$ , $T_A = +85^{\circ}C$ , OTP_INT_PU[0] = 0b0		0.01		
PGOOD Falling Edge Time		$C_{PGOOD} = 25pF$ , $V_{PGOOD} = 1.8V \geq 0$		25		ns
PGOOD Output Assert Delay Time	$t_{PGOODDLY}$	PG_DLY[1:0] = 0b00 (based on an internal 31.5kHz clock)		31.5		$\mu s$
		PG_DLY[1:0] = 0b01 (based on an internal 31.5kHz clock)		254		
		PG_DLY[1:0] = 0b10 (based on an internal 31.5kHz clock)		508		
		PG_DLY[1:0] = 0b11 (based on an internal 31.5kHz clock)		1016		
PGOOD Output Deassert Delay Time				0		$\mu s$
PGOOD Pullup Resistance	$R_{PU\_PGOOD}$	Pulled up to $V_{IN\_VIO}$ . OTP_INT_PU[0] = 0b1	50	100	170	$k\Omega$

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LP_MODE INPUT</b>						
LP_MODE I/O Pad Operating Voltage	$V_{SYS}$		2.6		5.5	V
LP_MODE Input-Low Voltage	$V_{IL}$				0.4	V
LP_MODE Input-High Voltage	$V_{IH}$		1.4			V
LP_MODE Input Hysteresis	$V_{HYS}$			50		mV
LP_MODE Input Leakage Current		$V_{SYS} = V_{IN\_VIO} = 5.5V$ , $V_{LP\_MODE} = 0V$ and $5.5V$ , $T_A = +25^{\circ}C$		0.001	1	$\mu A$
		$V_{SYS} = V_{IN\_VIO} = 5.5V$ , $V_{LP\_MODE} = 0V$ and $5.5V$ , $T_A = +85^{\circ}C$		0.01		
LP_MODE Debounce	$t_{LPMD\_DBNC}$	Debounce applies to rising and falling edge. Does not account for oscillator tolerance (Note 4)		95	127	$\mu s$
LP_MODE I/O Pad Undervoltage Lockout	$V_{SYSUVLO}$	$V_{SYS}$ falling		2.1		V
LP_MODE Mask Deassertion Timer	$t_{LPMD\_MSK}$		16	20	25	ms
<b>LP_ACK INPUT</b>						
I/O Pad Operating Voltage	$V_{SYS}$		2.6		5.5	V
Input Low Voltage	$V_{IL}$				0.4	V
Input High Voltage	$V_{IH}$		1.4			V
Input Hysteresis	$V_{HYS}$			50		mV
Input Leakage Current		$V_{SYS} = 5.5V$ , $V_{LP\_ACK} = 0V$ and $5.5V$ , $T_A = +25^{\circ}C$ , $OTP\_INT\_PU[0] = 0b0$		0.001	1	$\mu A$
		$V_{SYS} = 5.5V$ , $V_{LP\_ACK} = 0V$ and $5.5V$ , $T_A = +85^{\circ}C$ , $OTP\_INT\_PU[0] = 0b0$		0.01		
LP_ACK Pullup Resistance	$R_{PU\_LP\_ACK}$	Pulled up to $V_{IN\_VIO}$ , $OTP\_INT\_PU[0] = 0b1$	50	100	170	k $\Omega$



### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LP_REQ OUTPUT (OPEN DRAIN)</b>						
LP_REQ Output Voltage Low	$V_{OL}$	$I_{SINK} = 2mA$			0.4	V
LP_REQ Open Leakage Current		$V_{SYS} = V_{LP\_REQ} = 5.5V$ , $T_A = +25^\circ C$ , OTP_INT_PU[0] = 0b0		0.001	1	$\mu A$
		$V_{SYS} = V_{LP\_REQ} = 5.5V$ , $T_A = +85^\circ C$ , OTP_INT_PU[0] = 0b0		0.01		
LP_REQ Falling Edge Time		$C_{LP\_REQ} = 25pF$ , $V_{LP\_REQ} = 1.8V \geq 0$		25		ns
LP_REQ Delay	$t_{LPREQ\_LOW}$	LP_REQ_T_EN = 0, PMIC in master mode (OTP_SLP_MSTRSLV = 0), applies during DevSlp exit sequence		31.75		$\mu s$
		LP_REQ_T_EN = 1, PMIC in master mode (OTP_SLP_MSTRSLV = 0), applies during DevSlp exit sequence		20		ms
LP_REQ Pullup Resistance	$R_{PU\_LP\_REQ}$	Pulled up to $V_{IN\_VIO}$ , OTP_INT_PU[0] = 0b1	50	100	170	k $\Omega$
<b>EREG_ENx OUTPUT (OPEN DRAIN)</b>						
EREG_EN1 Output-Voltage Low	$V_{OL}$	$I_{SINK} = 2mA$			0.4	V
EREG_EN2 Output-Voltage Low	$V_{OL}$	$I_{SINK} = 10mA$			0.4	V
EREG_ENx Open Leakage Current		$V_{SYS} = V_{EREG\_ENx} = 5.5V$ , $T_A = +25^\circ C$ , OTP_INT_PU[0] = 0b0		0.001	1	$\mu A$
		$V_{SYS} = V_{EREG\_ENx} = 5.5V$ , $T_A = +85^\circ C$ , OTP_INT_PU[0] = 0b0		0.01		
EREG_ENx Falling Edge Time		$C_{EREG\_ENx} = 25pF$ , $V_{EREG\_ENx} = 1.8V \geq 0$		25		ns
EREG_EN1 Pullup Resistance	$R_{PU\_EREG\_ENx}$	Pulled up to $V_{H\_INT}$ , OTP_INT_PU[0] = 0b1	50	100	170	k $\Omega$
EREG_EN2 Pullup Resistance	$R_{PU\_EREG\_ENx}$	Pulled up to $V_{IN\_VIO}$ , OTP_INT_PU[0] = 0b1	50	100	170	k $\Omega$
<b>EREG_POK INPUT</b>						
I/O Pad Operating Voltage	$V_{SYS}$		2.6		5.5	V
Input Low Voltage	$V_{IL}$				0.4	V
Input High Voltage	$V_{IH}$		1.4			V
Input Hysteresis	$V_{HYS}$			50		mV

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		$V_{SYS} = 5.5V$ , $V_{EREG\_POK} = 0V$ and $5.5V$ , $T_A = +25^{\circ}C$ , $OTP\_INT\_PU[0] = 0b0$		0.001	1	$\mu A$
		$V_{SYS} = 5.5V$ , $V_{EREG\_POK} = 0V$ and $5.5V$ , $T_A = +85^{\circ}C$ , $OTP\_INT\_PU[0] = 0b0$		0.01		
EREG_POK Pullup Resistance	$R_{PU\_EREG\_POK}$	Pulled up to $V_{IN\_VIO}$ , $OTP\_INT\_PU[0] = 0b1$	50	100	170	$k\Omega$
<b>THERMAL MONITORS</b>						
Quiescent Supply Current	$I_{QTM}$			1.5		$\mu A$
Shutdown Supply Current				0.1		$\mu A$
Thermal Overload	$T_{JOVLD}$	$T_J$ rising, $15^{\circ}C$ hysteresis		165		$^{\circ}C$
Response Time		$5^{\circ}C$ overdrive		10		$\mu s$
<b>FLEXIBLE POWER SEQUENCER</b>						
Power-Up Sequence Enable Delay	$t_{FPSDON}$	Measured from internal $FPSxEN = 1$ to start of sequence (based on a 31.5kHz clock)		63.492		$\mu s$
Power-Down Sequence Enable Delay	$t_{FPSDOFF}$	Measured from internal $FPSxEN = 0$ to start of sequence (based on a 31.5kHz clock)		95.240		$\mu s$
Flexible Power Sequencer Event Period	$t_{FPS\_PU}$ , $t_{FPS\_PD}$	$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b000$		31		$\mu s$
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b001$		63		
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b010$		127		
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b011$		253		
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b100$		508		
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b101$		984		
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b110$		1936		
		$MSTRxUPF[2:0] =$ $MSTRxDNF[2:0] = 0b111$		3904		

### Electrical Characteristics—Global Resources (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IO} = 1.8V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Sequence Delay	$t_{PD\_DLY}$	PD_DLY[1:0] = 0b00		0		ms
		PD_DLY[1:0] = 0b01		1.0		
		PD_DLY[1:0] = 0b10		1.5		
		PD_DLY[1:0] = 0b11		2.0		
<b>BLD_IO</b>						
Maximum Bleed Time	$t_{BLEED\_MAX}$			20	22	ms
Minimum Bleed Time	$t_{BLEED\_MIN}$			31.5		$\mu s$
Bleed Threshold		BLD_IO falling		90	100	mV
Bleed Resistance	$R_{BLEED}$	BLD_IO = 0.3V		20	27	$\Omega$
BLD_IO Input Leakage Current		$V_{SYS} = 5.5V$ , $V_{BLD\_IO} = 0V$ and $5.5V$ , $T_A = +85^{\circ}C$		0.01		$\mu A$
		$V_{SYS} = 5.5V$ , $V_{BLD\_IO} = 0V$ and $5.5V$ , $T_A = +25^{\circ}C$		0.001	1	
<b>ON/OFF CONTROLLER</b>						
Hiccup Counter Limit	HICCUP_CNT_LIM			7		counts
<b>IN_PHUP</b>						
Operating Voltage Range	$V_{IN\_PHUP}$		2.4		5.5	V
IN_PHUP Supply Current	$I_{IN\_PHUP}$	$V_{SYS} = V_{IN\_PHUP} = 5.5V$ , $T_A = +25^{\circ}C$		5.0		$\mu A$

**Note 4:** The LP\_MODE debounce period has a variation due to the variability associated with quantizing an asynchronous input signal. Additionally, while measuring the period from a valid LP\_MODE edge to a subsequent event, such as LP\_REQ assertion, there is one more clock cycle (CLK32K) of delay observed in a real system.

## Electrical Characteristics—Inrush Control

( $V_{IN\_SNS} = 5.0V$ , limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>POWER SUPPLY</b>							
Supply Voltage Range	$V_{IN}$		2.1		5.5	V	
IN Undervoltage-Lockout Threshold	$V_{INUVLO}$	$V_{IN}$ rising		2.3	2.55	V	
IN Undervoltage-Lockout Hysteresis	$V_{INUVLO\_HYS}$			200		mV	
IN Undervoltage-Lockout Response Time	$t_{INUVLO}$	$V_{IN}$ rising ( $V_{IN} = V_{INUVLO} + 100mV$ )		39		$\mu s$	
IN Overvoltage-Lockout Threshold	$V_{INOVLO}$	$V_{IN}$ rising	5.70	5.87	6.10	V	
IN Overvoltage-Lockout Hysteresis	$V_{INOVLO\_HYS}$			80		mV	
IN Overvoltage-Lockout Response Time	$t_{INOVLO}$	$V_{IN}$ rising ( $V_{IN} = V_{INOVLO} + 50mV$ )		8		$\mu s$	
Leakage	$I_{LKG\_VIN\_DRV}$	$V_{IN} = 5.5V$ , $V_{IN\_DRV} = 0V$ and $11V$ , $T_A = +25^\circ C$		0.001	1	$\mu A$	
		$V_{IN} = 5.5V$ , $V_{IN\_DRV} = 0V$ and $11V$ , $T_A = +85^\circ C$		0.01			
Supply Current (Soft-Start)	$I_{Q\_IN\_SS}$	$V_{IN\_DRV} - VINR\_OUT < V_{IN\_SNS}$ (soft-start state), $OTP\_GDRV\_FREQ = 0b111$ (800kHz), $V_{IN\_SNS} = 3.3V$		85		$\mu A$	
		$V_{IN\_DRV} - VINR\_OUT < V_{IN\_SNS}$ (soft-start state), $OTP\_GDRV\_FREQ = 0b111$ (800kHz), $V_{IN\_SNS} = 5V$		138			
Supply Current (Steady-State)	$I_{IN}$	$V_{IN\_DRV} - VINR\_OUT = V_{IN\_SNS}$ (steady state), $t_{SS\_DONE}$ expired, $f_{GDRV} = 12.5kHz$ , $V_{IN\_SNS} = 3.3V$		26		$\mu A$	
		$V_{IN\_DRV} - VINR\_OUT = V_{IN\_SNS}$ (steady state), $t_{SS\_DONE}$ expired, $f_{GDRV} = 12.5kHz$ , $V_{IN\_SNS} = 5V$		37			
<b>NMOS SWITCH DRIVER</b>							
Gate Drive ON Voltage	$V_{IN\_DRV\_ON}$	$V_{IN} = 5V$	Voltage with respect to ground when external MOSFET is being driven to it's fully ON state	8.5		11	V
Gate Drive Current	$I_{GDRV\_INRUSH}$	$V_{IN} = 3.3V$ , 1X gate drive frequency setting		1.8	3.0	4.2	$\mu A$
4x Gate Drive Oscillator Frequency	$f_{GDRV\_4X}$	$OTP\_INR\_FREQ[2:0] = 0b111$ , $V_{IN} = 3.3V$ , $V_{IN} = 5V$		720			kHz

### Electrical Characteristics—Inrush Control (continued)

( $V_{IN\_SNS} = 5.0V$ , limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2x Gate Drive Oscillator Frequency	$f_{GDRV\_2X}$	OTP_INR_FREQ[2:0] = 0b110, $V_{IN} = 3.3V, V_{IN} = 5V$		360		kHz
1x Gate Drive Oscillator Frequency	$f_{GDRV\_1X}$	OTP_INR_FREQ[2:0] = 0b101 (nominal gate drive strength), $V_{IN} = 3.3V, V_{IN} = 5V$	120	180	240	kHz
0.5x Gate Drive Oscillator Frequency	$f_{GDRV\_0.5X}$	OTP_INR_FREQ[2:0] = 0b100, $V_{IN} = 3.3V, V_{IN} = 5V$		90		kHz
0.25x Gate Drive Oscillator Frequency	$f_{GDRV\_0.25X}$	OTP_INR_FREQ[2:0] = 0b011, $V_{IN} = 3.3V, V_{IN} = 5V$		45		kHz
0.125x Gate Drive Oscillator Frequency	$f_{GDRV\_0.125X}$	OTP_INR_FREQ[2:0] = 0b010, $V_{IN} = 3.3V, V_{IN} = 5V$	15	23	32	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{GDRV\_0.0625X}$	OTP_INR_FREQ[2:0] = 0b001, $V_{IN} = 3.3V, V_{IN} = 5V$		11.25		kHz
0.03125x Gate Drive Oscillator Frequency	$f_{GDRV\_0.03125X}$	OTP_INR_FREQ[2:0] = 0b000, $V_{IN} = 3.3V, V_{IN} = 5V$		5.625		kHz
Gate Drive Discharge Resistance	$R_{GDRV\_DIS}$	Resistance from INR_DRV to INR_OUT, $V_{INR\_DRV-INR\_OUT} = 4V$		74		$\Omega$
		Resistance from INR_DRV to INR_OUT, $V_{INR\_DRV-INR\_OUT} = 3.3V$		100		
<b>TIMING</b>						
Start-Up Delay	$t_{EN\_INRUSH}$	Time from $V_{IN}$ rising above $V_{INUVLO}$ to the internal charge pump being enabled. Duration is based on the gate drive oscillator frequency ( $f_{GDRV}$ ) selected by OTP_INR_FREQ[2:0]		128		cycles of $f_{GDRV}$
Soft-Start Done Time	$t_{SS\_1}$	Duration from MOSFET drive circuit being enabled (subsequent to startup delay) to the point when the IN_SS_DONE (internal signal) is asserted allowing a power-up sequence to occur. Based on default gate drive frequency ( $f_{GDRV}$ ) selected by OTP_INR_FREQ[2:0]		512		cycles of $f_{GDRV}$
Gate Drive Idle Time	$t_{SS\_DONE}$	Duration from MOSFET drive circuit being enabled (subsequent to the startup delay) to the point when the gate drive oscillator frequency folds back to the 12.5kHz setting (idle gate drive). Based on default gate drive frequency ( $f_{GDRV}$ ) selected by OTP_INR_FREQ[2:0]		1024		cycles of $f_{GDRV}$

### Electrical Characteristics—Current Sense Amplifier

( $V_{SYS} = 3.3V$ ,  $C_{LOAD} = 10pF$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT OVERCURRENT</b>						
Input Overcurrent Threshold		2.25A setting, $V_{SYS} = 3.3V$	-6.5		+6.5	%
CSA Debounce Timer		OTP_CSA_DBNC = 0		100		$\mu s$
		OTP_CSA_DBNC = 1		50		
Overcurrent-Sense Comparator Threshold 1	$V_{OC\_THR}$	Overcurrent limit, CSTH_OPT[1:0] = 0b00		30		mV
Overcurrent-Sense Comparator Threshold 2	$V_{OC\_THR}$	Overcurrent limit, CSTH_OPT[1:0] = 0b01		35		mV
Overcurrent-Sense Comparator Threshold 3	$V_{OC\_THR}$	Overcurrent-limit, CSTH_OPT[1:0] = 0b10		40		mV
Overcurrent-Sense Comparator Threshold 4	$V_{OC\_THR}$	Overcurrent limit, CSTH_OPT[1:0] = 0b11		45		mV

### Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY VOLTAGE AND CURRENT</b>						
Input Voltage Range	$V_{INBx}$		2.6		5.5	V
Shutdown Supply Current	$I_{QSHDN\_BUCKx}$	(Note 5)		0.1		$\mu A$
Supply Quiescent Current	$I_{Q\_SKIP\_NM\_BUCKx}$	No switching, no load, (Note 6), $V_{SYS} = 3.3V$		19	30	$\mu A$
		No switching, no load, (Note 6), $V_{SYS} = 5V$		19	30	
	$I_{Q\_FPWM\_BUCKx}$	FPWM mode (switching at fixed frequency), no load, $V_{SYS} = 3.3V$		10		mA
		FPWM mode (switching at fixed frequency), no load, $V_{SYS} = 5V$		10		
	$I_{Q\_SKIP\_LPM\_BUCKx}$	Low-power mode (no switching), no load, (Note 6), $V_{SYS} = 3.3V$		5	9	$\mu A$
		Low-power mode (no switching), no load, (Note 6), $V_{SYS} = 5V$		5	9	

### Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OUTPUT VOLTAGE</b>						
Output Voltage Range	$V_{OUT\_BUCKx}$	Programmable in 6.25mV steps with BUCK1VOUT[7:0] and BUCK2VOUT[7:0]	0.600		2.194	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_BUCKx}$	FPWM mode, normal mode, no load, $V_{OUT\_BUCK1} = 1.800V$	-2		+2	%
	$V_{OUT\_ACC\_LPM\_BUCKx}$	Low-power mode, no load, $V_{OUT\_BUCK1} = 1.800V$	-4		+4	
	$V_{OUT\_ACC\_NM\_BUCKx}$	FPWM mode, normal mode, no load, $V_{OUT\_BUCK2} = 1.200V$	-2		+2	
	$V_{OUT\_ACC\_LPM\_BUCKx}$	Low-power mode, no load, $V_{OUT\_BUCK2} = 1.200V$	-4		+4	
<b>OUTPUT CURRENT</b>						
Maximum Output Current	$I_{OUT\_MAX\_NM\_BUCKx}$	RMS, normal mode, $L = 1\mu H$	2000			mA
	$I_{OUT\_MAX\_LPM\_BUCKx}$	RMS, low-power mode, $L = 1\mu H$		10		
PMOS Peak Current Limit	$I_{LIMP}$	$V_{SYS} = 3.6V$	2300	2875	4200	mA
		$V_{SYS} = 5V$	2300	2875	4200	
NMOS Valley Current Limit	$I_{LIMV}$	$V_{SYS} = 3.6V$		2125		mA
		$V_{SYS} = 5V$		2125		
NMOS Negative Current Limit	$I_{LIMN}$	$V_{SYS} = 3.6V$		800		mA
		$V_{SYS} = 5V$		800		
<b>PERFORMANCE PARAMETERS</b>						
Line Regulation		$V_{SYS} = V_{INBx} = 2.6V$ to $5.5V$		0.2		%/V
Load Regulation		Load = 0 to 1A, FPWM mode		0.125		%/A
Load Transient Response		FPWM mode, $V_{OUT\_BUCKx} =$ default, $L = 1\mu H$ , $C_{OUT} = 12\mu F$ effective $\Delta I_{OUT} = 0.2A-2A$ , $\Delta t = 3\mu s$		88		mV
		Skip mode, $V_{OUT\_BUCKx} =$ default, $L = 1\mu H$ , $C_{OUT} = 12\mu F$ effective $\Delta I_{OUT} = 10mA$ to $0.7A$ , $\Delta t = 3\mu s$ ,		90		
Switching Frequency	$f_{SW}$	$V_{SYS} = 3.3V$	1.8	2	2.2	MHz
Dead Time	$t_{DEAD}$	$V_{SYS} = 3.3V$		2.0		ns
Switching Frequency	$f_{SW}$	$V_{SYS} = 5V$	1.8	2	2.2	MHz

### Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dead Time	$t_{DEAD}$	$V_{SYS} = 5V$		2.0		ns
Soft-Start Slew Rate		Fixed for buck 1		6.5		mV/ $\mu$ s
		Fixed for buck 2		17		
Output Voltage Ramp-Up Slew Rate		Fixed for buckx (Notes 5, 8, 9), $C_{OUT} = 22\mu F$		40		mV/ $\mu$ s
Output Voltage Ramp-Down Slew Rate		Fixed for buck 1, 2 (Notes 5, 8), $C_{OUT} = 22\mu F$ , BUCKxFPWMEN = 1 (x = 1, 2), no load		18		mV/ $\mu$ s
PMOS ON Resistance	$R_{ON\_PCH}$	$V_{SYS} = V_{INBUCKx} = 3.6V$ , $I_{OUT} = 150mA$		100	150	m $\Omega$
		$V_{SYS} = V_{INBUCKx} = 5V$ , $I_{OUT} = 150mA$		100	150	
NMOS ON Resistance	$R_{ON\_NCH}$	$V_{SYS} = V_{INBUCKx} = 3.6V$ , $I_{OUT} = 150mA$		60	100	m $\Omega$
		$V_{SYS} = V_{INBUCKx} = 5V$ , $I_{OUT} = 150mA$		60	100	
NMOS Zero-Crossing Threshold	$I_{ZX}$	Threshold to determine transition from PWM to SKIP mode		20		mA
Output Voltage Ripple in Skip Mode		$V_{OUT\_BUCKx} = 1.0V$ , $L = 1\mu H$ , $C_{OUT} = 12\mu F$ effective, no load (Note 5)		40		mV $_{P-P}$
Output Voltage Ripple in PWM Mode		$V_{OUT\_BUCKx} = 1.0V$ , $L = 1\mu H$ , $C_{OUT} = 12\mu F$ effective, $I_{LOAD} = 0.5 \times I_{OUT\_MAX\_BUCKx}$ (Note 5)		5		mV $_{P-P}$
LX Leakage	$I_{L\_LX\_25C}$	$V_{LX} = 5.5V$ or $0V$ , $T_A = +25^{\circ}C$		0.1	1	$\mu A$
	$I_{L\_LX\_85C}$	$V_{LX} = 5.5V$ or $0V$ , $T_A = +85^{\circ}C$ (Note 5)		1		
Output Active Discharge Resistance	$R_{DISCHG\_BUCKx}$	Resistance from FBBx to PGNDx, output disabled, (Note 7)		100		$\Omega$
Nominal Output Inductance	$L_{NOM}$			1.0		$\mu H$
Minimum Effective Output Capacitance	$C_{OUT\_EFF\_MIN}$	$0mA < I_{OUT} < 2000mA$	18			$\mu F$
Light Load Efficiency	$Eff_{LIGHT}$	Low-power mode, $I_{OUT} = 0.5mA$ , $V_{OUT\_BUCKx} = 1.0V$ , $L = 1\mu H$ , $DCR_L = 50m\Omega$ , $C_{OUT} = 22\mu F$ (Note 5)		75		%



### Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Typical Load Efficiency	$Eff_{IOUT\_TYP}$	$I_{OUT} = 0.25 \times I_{OUT\_MAX\_BUCKx}$ , $V_{OUT\_BUCKx} = 1.0V$ , $L = 1\mu H$ , $DCR_L = 50m\Omega$ , $C_{OUT} = 22\mu F$ (Note 5)		85		%
Maximum Load Efficiency	$EFF_{IOUT\_MAX}$	$I_{OUT} = I_{OUT\_MAX\_BUCKx}$ , $V_{OUT} = 1.0V$ , $L = 1\mu H$ , $DCR_L = 50m\Omega$ , $C_{OUT} = 22\mu F$ (Note 5)		70		%
Turn-On Delay Time	$t_{ON\_DLY\_BUCKx}$	EN signal to LX switching with bias ON		30		$\mu s$
Maximum Duty Cycle		$V_{OUT\_BUCKx} / V_{IN\_BUCKx}$ expressed as %		90		%
<b>BROWNOUT COMPARATOR</b>						
Output Brownout Threshold	$V_{BO\_BUCKx}$	Normal-power mode, falling threshold, $BUCKx\_BO\_THR[1:0] = 0b00$		75		%
		Normal-power mode, falling threshold, $BUCKx\_BO\_THR[1:0] = 0b01$		80		
		Normal-power mode, falling threshold, $BUCKx\_BO\_THR[1:0] = 0b10$		85		
		Normal-power mode, falling threshold, $BUCKx\_BO\_THR[1:0] = 0b11$		90.7		
Output Brownout Accuracy		Normal-power mode. $V_{OUT\_BUCKx} = 1.0V$ ( $V_{OUT\_BUCKx}[7:0] = 0 \times 40$ )	-4.0		+4.0	%
Output Brownout Threshold (Low-Power Mode)	$V_{BO\_BUCKx}$	Falling threshold, low-power mode		86.0		%
Output Brownout Accuracy		Low-power mode. $V_{OUT\_BUCKx} = 1.0V$ ( $V_{OUT\_BUCKx}[7:0] = 0 \times 40$ )	-4		+4	%
Output Brownout Hysteresis Range	$V_{BO\_HYS\_BUCKx}$	2-bit control over I <sup>2</sup> C. Max rising threshold limited to 96%	5		20	%
Brownout Voltage Hysteresis Programming Step Size		Programmable with $BUCKx\_BO\_HYS[1:0]$		5		%
Output Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_BUCKx\_LPM}$			5		%

### Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Brownout Response Time	$t_{BO\_BUCKx}$	BUCKx_BO_PR[1:0] = 0b00 (fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.04		$\mu$ s
		BUCKx_BO_PR[1:0] = 0b01 (med-fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.14		
		BUCKx_BO_PR[1:0] = 0b10 (med-slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.30		
		BUCKx_BO_PR[1:0] = 0b11 (slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.68		
		Buck in low-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		3.18		
Output Brownout Supply Current	$I_{QNM\_BO\_BUCKx}$	Normal-power mode, BUCKx_BO_PR[1:0] = 0b00 (fast)		13.4		$\mu$ A
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b01 (med-fast)		10.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b10 (med-slow)		7.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b11 (slow)		4.4		
	$I_{QLPM\_BO\_BUCKx}$	Low-power mode		1.3		

### Electrical Characteristics—Buck Regulators (BUCK1/2 - 2A Output) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OV COMPARATOR</b>						
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCKx_OV_THR = 1, referenced to output voltage setting		116.6		%
Output OV Hysteresis		BUCKx_OV_THR = 1		9.1		%
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCKx_OV_THR = 0, referenced to output voltage setting		108.3		%
Output OV Hysteresis		BUCKx_OV_THR = 0		2.8		%
Output OV Trip Level (Low-Power Mode)	$V_{OUTBUCKx\_OV}$	Rising edge, low-power mode		108.3		%
Output OV hysteresis (Low-Power Mode)		Low-power mode		2.8		%
Output Over-Voltage Response Time	$t_{OV\_BUCKx}$	Normal-power mode, 100mV over-drive with rising slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ rising to PGOOD pin falling (Note 5)		1.68		$\mu$ s
Output Over-Voltage Supply current	$I_{Q\_OV\_BUCKx}$	Normal-power mode		4.4		$\mu$ A
Output Over-Voltage Response Time (Low-Power Mode)	$t_{OV\_BUCKx}$	Low-power mode, 100mV over-drive with rising slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ rising to PGOOD pin falling (Note 5)		3.18		$\mu$ s
Output Over-Voltage Supply Current (Low-Power Mode)	$I_{Q\_OV\_BUCKx}$	Low-power mode		1.3		$\mu$ A

**Note 5:** Design guidance only and is not production tested.

**Note 6:** Individual buck  $I_q$  is not production tested. It is covered by a combined test by turning on all bucks.

**Note 7:** There is an n-channel MOSFET in series with the output active-discharge resistance. This NMOS requires  $V_{SYS} > 1.2V$  to be enhanced.

**Note 8:** The ramp down slew rate when the output voltage is decreased through  $I^2C$  is a function of the negative current limit and the output capacitance. With no load, forced PWM mode and 22 $\mu$ F output capacitor, the ramp-down slew rate is  $dv/dt = i / C = 0.4A / 22\mu F = 18mV/\mu s$ .

**Note 9:** DVS and soft-start ramp rates can be expected to vary by up to 30%.

### Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output)

( $V_{SYS} = 5.0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SUPPLY VOLTAGE AND CURRENT</b>						
Input Voltage Range	$V_{INBUCK3}$		2.6		5.5	V
Shutdown Supply Current	$I_{QSHDN\_BUCK3}$	(Note 10)		0.1		$\mu A$
Supply Quiescent Current	$I_{Q\_SKIP\_NM\_BUCK3}$	No switching, no load (Note 10)		26	40	$\mu A$
	$I_{Q\_FPWM\_BUCK3}$	FPWM mode, no load (Note 10)		10		mA
	$I_{Q\_SKIP\_LPM\_BUCK3}$	Low-power mode (no switching), no load (Note 10)		10	19	$\mu A$
<b>OUTPUT VOLTAGE</b>						
Output Voltage Range	$V_{OUT\_BUCK3}$	I <sup>2</sup> C programmable in 10mV Steps (BUCK3VOUT[6:0] = 0x01 to 0x7F)	0.26		1.52	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_BUCK3}$	FPWM mode, normal mode, no load, $T_A = +25^{\circ}C$ , $V_{OUT\_BUCK3} = 1.0V$	-2		+2	%
	$V_{OUT\_ACC\_LPM\_BUCK3}$	Low-power mode, no load, $T_A = +25^{\circ}C$ , $V_{OUT\_BUCK3} = 1.000V$	-4		+4	
<b>PERFORMANCE PARAMETERS</b>						
Switching Frequency	$f_{SW}$	$V_{SYS} = 3.3V$	1.8	2	2.2	MHz
		$V_{SYS} = 5V$	1.8	2	2.2	
Line Regulation		$V_{INBUCK3} = 2.6V$ to $5.5V$ , $V_{OUT\_BUCK3} = 1.0V$		0.2		%/V
Load Regulation		$V_{OUT\_BUCK3} = 1.0V$ , (Note 10), load = 0 to 1A, FPWM mode		0.125		%/A
Load Transient Response (Droop)		Skip mode, $V_{OUT} =$ default, $L = 1\mu H$ , $C_{OUT} = 28\mu F$ effective $\Delta I_{OUT} = 20mA$ to $500mA$ , $\Delta t = 0.8\mu s$ (Note 10)		45		mV
		Skip mode, $V_{OUT} =$ default, $L = 1\mu H$ , $C_{OUT} = 28\mu F$ effective $\Delta I_{OUT} = 20mA$ to $3A$ , $\Delta t = 4.8\mu s$ (Note 10)		70		
Soft-Start Slew Rate		BUCK3SSRAMP = 0		2.5		mV/ $\mu s$
		BUCK3SSRAMP = 1		10		
Output Voltage Ramp-Up/Down Slew Rate (DVS)				10		mV/ $\mu s$

### Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

( $V_{SYS} = 5.0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMOS ON Resistance	$R_{ON\_PCH}$	$V_{SYS} = V_{INBUCK3} = 5V$ , $I_{OUT} = 150mA$		60	90	m $\Omega$
		$V_{SYS} = V_{INBUCK3} = 3.6V$ , $I_{OUT} = 150mA$		60	90	
NMOS ON Resistance	$R_{ON\_NCH}$	$V_{SYS} = V_{INBUCK3} = 5V$ , $I_{OUT} = 150mA$		35	60	m $\Omega$
		$V_{SYS} = V_{INBUCK3} = 3.6V$ , $I_{OUT} = 150mA$		35	60	
NMOS Zero-Crossing Threshold	$I_{ZX\_SKIP}$	SKIP mode		20		mA
	$I_{ZX\_PWM}$	PWM mode		20		
Output Voltage Ripple In Skip Mode		$V_{OUT\_BUCK3} = 1.0V$ , $L = 1\mu H$ , $C_{OUT} = 28\mu F$ effective, no load (Note 10)		15		mV
Output Voltage Ripple In PWM Mode		$V_{OUT\_BUCK3} = 1.0V$ , $L = 1\mu H$ , $C_{OUT} = 28\mu F$ effective, $I_{LOAD} = 0.5 \times I_{OUT\_MAX\_BUCK3}$ (Note 10)		5		mV
LX Leakage	$I_{L\_LX\_25C}$	$V_{LXBUCK1} = 5.5V$ or $0V$ , $T_A = +25^{\circ}C$		0.1	1	$\mu A$
	$I_{L\_LX\_85C}$	$V_{LXBUCK1} = 5.5V$ or $0V$ , $T_A = +85^{\circ}C$ (Note 10)		1		
Output Active Discharge Resistance	$R_{DISCHG\_BUCK3}$	Resistance from FBB3 to PGND3, output disabled		100		$\Omega$
Nominal Output Inductance	$L_{NOM}$			1.0		$\mu H$
Minimum Effective Output Capacitance	$C_{OUT\_EFF\_MIN}$	$0mA < I_{OUT} < 3000mA$		28		$\mu F$
Turn-On Delay Time	$t_{ON\_DLY\_BUCK1}$	EN signal to LX switching with bias ON		200		$\mu s$
Light Load Efficiency	$Eff_{LIGHT}$	Low-power mode, $I_{OUT} = 0.5mA$ , $V_{OUT\_BUCKx} = 1.0V$ , $L = 1\mu H$ , $DCR_L = 50m\Omega$ , $C_{OUT} = 3 \times 22\mu F$ (Note 10)		75		%
Typical Load Efficiency	$Eff_{I_{OUT\_TYP}}$	$I_{OUT} = 0.25 \times I_{OUT\_MAX\_BUCKx}$ , $V_{OUT\_BUCKx} = 1.0V$ , $L = 1\mu H$ , $DCR_L = 50m\Omega$ , $C_{OUT} = 3 \times 22\mu F$ (Note 10)		88		%
Maximum Load Efficiency	$Eff_{I_{OUT\_MAX}}$	$I_{OUT} = I_{OUT\_MAX\_BUCKx}$ , $V_{OUT} = 1.0V$ , $L = 1\mu H$ , $DCR_L = 50m\Omega$ , $C_{OUT} = 3 \times 22\mu F$ (Note 10)		77		%

### Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

( $V_{SYS} = 5.0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OUTPUT CURRENT</b>						
Maximum Output Current	$I_{OUT\_MAX\_NM\_BUCK3}$	RMS, normal mode	3000			mA
	$I_{OUT\_MAX\_LPM\_BUCK3}$	RMS, low-power mode		10		
PMOS Peak Current Limit	$I_{LIMP}$	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{SYS} = 3.6V$	3825	4250	4675	mA
NMOS Valley Current Limit	$I_{LIMV}$			3750		mA
NMOS (Negative) Current Limit	$I_{LIMN}$			2000		mA
<b>BROWNOUT COMPARATOR</b>						
Output Brownout Threshold	$V_{BO\_BUCK3}$	Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b00		77		%
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b01		81		
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b10		85.7		
		Normal-power mode, falling threshold, BUCK3_BO_THR[1:0] = 0b11		91		
Output Brownout Accuracy		Normal-power mode. $V_{OUT\_BUCK3} = 1.0V$ ( $V_{OUT\_BUCK3}[7:0] = 0x4B$ )	-4.5		+4.5	%
Output Brownout Threshold (Low-Power Mode)	$V_{BO\_BUCKx}$	Falling threshold, low-power mode		86.0		%
Output Brownout Accuracy		Low-power mode, $V_{OUT\_BUCK3} = 1.0V$ ( $V_{OUT\_BUCK3}[7:0] = 0x4B$ )	-4		+4	%
Output Brownout Hysteresis Range	$V_{BO\_HYS\_BUCKx}$	2-Bit control over I <sup>2</sup> C. Max rising threshold limited to 96%	5		20	%
Brownout Voltage Hysteresis Programming Step Size		Programmable with BUCKx_BO_HYS[1:0]		5		%
Output Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_BUCKx\_LPM}$			5		%

### Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

( $V_{SYS} = 5.0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Brownout Response Time	$t_{BO\_BUCKx}$	BUCKx_BO_PR[1:0] = 0b00 (fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.04		$\mu$ s
		BUCKx_BO_PR[1:0] = 0b01 (med-fast), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.14		
		BUCKx_BO_PR[1:0] = 0b10 (med-slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.30		
		BUCKx_BO_PR[1:0] = 0b11 (slow), buck in normal-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		1.68		
		Buck in Low-power mode, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ falling to PGOOD pin falling		3.18		
Output Brownout Supply Current	$I_{QNM\_BO\_BUCKx}$	Normal-power mode, BUCKx_BO_PR[1:0] = 0b00 (fast)		13.4		$\mu$ A
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b01 (med-fast)		10.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b10 (med-slow)		7.4		
		Normal-power mode, BUCKx_BO_PR[1:0] = 0b11 (slow)		4.4		
	$I_{QLPM\_BO\_BUCKx}$	Low-power mode		1.3		

### Electrical Characteristics—Buck Regulators (BUCK3 - 3A Output) (continued)

( $V_{SYS} = 5.0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OV COMPARATOR</b>						
Output OV Trip Level	$V_{OUTBUCK3\_OV}$	Rising edge, BUCK3_OV_THR = 1		117.1		%
Output OV hysteresis		BUCK3_OV_THR = 1		8.6		%
Output OV Trip Level	$V_{OUTBUCKx\_OV}$	Rising edge, BUCK3_OV_THR = 0		108.5		%
Output OV Hysteresis		BUCK3_OV_THR = 0		3.9		%
Output OV Trip Level (Low-Power Mode)	$V_{OUTBUCK3\_OV}$	Rising edge, low-power mode		108.3		%
Output OV Hysteresis (Low-Power Mode)		Low-power mode		3.9		%
Output Over-Voltage Response Time	$t_{OV\_BUCK3}$	Buck in normal-power mode, 100mV over-drive with rising slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCK3}$ rising to PGOOD pin falling (Note 10)		1.68		$\mu$ s
Output Over-Voltage Supply current	$I_{Q\_OV\_BUCKx}$	Buck in normal-power mode		4.4		$\mu$ A
Output Over-Voltage Response Time (Low-Power Mode)	$t_{OV\_BUCKx}$	Buck in low-power mode, 100mV over-drive with rising slew rate of 150mV/ $\mu$ s. Time from $V_{OUT\_BUCKx}$ rising to PGOOD pin falling (Note 10)		3.18		$\mu$ s
Output Over-Voltage Supply current (Low-Power Mode)	$I_{Q\_OV\_BUCK3}$	Buck in low-power mode		1.3		$\mu$ A

**Note 10:** Design guidance only and is not production tested.



## Electrical Characteristics—Load Switch Driver (LSW1/2)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. x is used to represent multiple instances of similar resources, for this section  $x = 1, 2$  unless specified for e.g., LSWx represents LSW1, LSW2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Current	$I_{SYS\_LSW\_SS}$	$V_{INLSWx} = V_{SYS} = 5V$ , LSWxDRV_FREQ=0b111 (800kHz), $C_{OUTLSWx} = 20\mu F$		68		$\mu A$
Supply Voltage Range	$V_{SYS}$		2.6		5.5	V
Supply Current	$I_{SYS\_LSW\_SS}$	$V_{INLSWx} = V_{SYS} = 3.3V$ , LSWxDRV_FREQ = 0b111 (1.6MHz), $C_{OUTLSWx} = 20\mu F$		43		$\mu A$
		$V_{INLSWx} = V_{SYS} = 5V$ , LSWxDRV_FREQ = 0b101 (400kHz), $C_{OUTLSWx} = 20\mu F$		20		
Leakage	$I_{LKG\_LSWx\_DRV}$	$V_{SYS} = 5.5V$ , $V_{LSWx\_DRV} = 0V$ and $11V$ , $T_A = +25^{\circ}C$		0.001	1	$\mu A$
		$V_{SYS} = 5.5V$ , $V_{LSWx\_DRV} = 0V$ and $11V$ , $T_A = +85^{\circ}C$		0.01		
<b>NMOS SWITCH DRIVER</b>						
Gate Drive Voltage	$V_{LSWx\_DRV}$	$V_{SYS} = 5V$	8.5		11	V
Gate Drive Current	$I_{LSWx\_DRV}$	$V_{SYS} = 3.3V$ , 1X gate drive frequency setting (LSWx_DRV_FREQ[2:0] = 0b101), $C_{OUTLSWx} = 20\mu F$	1.85	3.7	5.55	$\mu A$
4x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_4X}$	LSWxDRV_FREQ[2:0] = 0b111, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		1600		kHz
2x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_2X}$	LSWx_DRV_FREQ[2:0] = 0b110, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		800		kHz
1x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_1X}$	LSWx_DRV_FREQ[2:0] = 0b101 (nominal gate drive strength), $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$	200	400	600	kHz
0.5x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.5X}$	LSWx_DRV_FREQ[2:0] = 0b100, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		200		kHz
0.25x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.25X}$	LSWx_DRV_FREQ[2:0] = 0b011, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		100		kHz
0.125x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.125X}$	LSWx_DRV_FREQ[2:0] = 0b010, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$	25	50	75	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.0625X}$	LSWx_DRV_FREQ[2:0] = 0b001, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		25		kHz

### Electrical Characteristics—Load Switch Driver (LSW1/2) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. x is used to represent multiple instances of similar resources, for this section  $x = 1, 2$  unless specified for e.g., LSWx represents LSW1, LSW2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
0.03125x Gate Drive Oscillator Frequency	$f_{LSWx\_DRV\_0.03125X}$	LSWx_DRV_FREQ[2:0] = 0b000, $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		12.50		kHz
Output Active Discharge Resistance	$R_{DISCHG\_LSW}$		50	100	150	$\Omega$
Gate Drive Discharge Resistance	$R_{LSW\_GDRV\_DIS}$	Resistance from LSWx_DRV to FBLSWx, $V_{LSWx\_DRV-FBLSWx} = 4V$		74		$\Omega$
		Resistance from LSWx_DRV to FBLSWx, $V_{LSWx\_DRV-FBLSWx} = 3.3V$		100		
<b>TIMING</b>						
Soft-Start Done Time	$t_{SS\_DONE\_LSW}$	Duration from MOSFET drive circuit being enabled to the internal soft-start done signal being asserted. Based on default gate drive frequency ( $f_{LSWx\_DRV\_FREQ}$ ) selected by LSWx_DRV_FREQ[2:0] to program the default gate drive frequency		256		cycles of $f_{LSWx\_DRV\_FREQ}$
<b>POWER-OK COMPARATOR</b>						
Output Power-OK Threshold	$V_{LSWx\_OUT\_POK\_INT}$	Rising edge, input to the load switch is either one of the three internal buck regulator outputs or $V_{SYS}$ as selected by LSWx_INP_EXT	0.85 x $V_{IN\_LSWx}$	0.90 x $V_{IN\_LSWx}$	0.95 x $V_{IN\_LSWx}$	V
Output Power-OK Hysteresis				3		%
Power-OK Response Time		$V_{SYS} = 3.3V$ , $V_{INLSWx} = 1.8V$ , LSWx is enabled, 100mV under-drive with falling slew rate of 150mV/ $\mu$ s		1.20		$\mu$ s
Power-OK Comparator Active Current	$I_{Q\_POK\_LSWx}$	$V_{SYS} = 3.3V$ , $V_{INLSWx} = 1.8V$ , LSWx is enabled		1.1		$\mu$ A

### Electrical Characteristics—Load Switch Driver (LSW3)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. This section is applicable when  $OTP\_INRUSH\_DISABLE = 1$  and  $LSW\_OTP\_SEL = 1$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Voltage Range	$V_{SYS}$		2.6		5.5	V
Supply Current	$I_{SYS\_LSW\_SS}$	$V_{INLSW3} = V_{SYS} = 3.3V$ , $OTP\_INR\_FREQ[2:0] = 0b111$ (720kHz), $C_{OUTLSW3} = 20\mu F$		40		$\mu A$
		$V_{INLSW3} = V_{SYS} = 5V$ , $OTP\_INR\_FREQ[2:0] = 0b111$ (720kHz), $C_{OUTLSW3} = 20\mu F$		67		
Leakage	$I_{LKG\_LSW3\_DRV}$	$V_{SYS} = 5.5V$ , $V_{INR\_DRV} = 0V$ and $11V$ , $T_A = +25^{\circ}C$		0.001	1	$\mu A$
		$V_{SYS} = 5.5V$ , $V_{INR\_DRV} = 0V$ and $11V$ , $T_A = +85^{\circ}C$		0.01		
<b>NMOS SWITCH DRIVER</b>						
Gate Drive Voltage	$V_{LSW3\_DRV}$	$V_{SYS} = 5V$	8.5		11	V
Gate Drive Current	$I_{LSW3\_DRV}$	$V_{SYS} = 3.3V$ , 1X gate drive frequency setting ( $OTP\_INR\_FREQ[2:0] = 0b101$ ), $C_{OUTLSW3} = 20\mu F$	1.8	3	4.2	$\mu A$
4x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_4X}$	$OTP\_INR\_FREQ[2:0] = 0b111$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		720		kHz
2x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_2X}$	$OTP\_INR\_FREQ[2:0] = 0b110$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		360		kHz
1x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_1X}$	$OTP\_INR\_FREQ[2:0] = 0b101$ (nominal gate drive strength), $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$	120	180	240	kHz
0.5x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.5X}$	$OTP\_INR\_FREQ[2:0] = 0b100$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		90		kHz
0.25x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.25X}$	$OTP\_INR\_FREQ[2:0] = 0b011$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		45		kHz
0.125x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.125X}$	$OTP\_INR\_FREQ[2:0] = 0b010$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$	15	23	32	kHz
0.0625x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.0625X}$	$OTP\_INR\_FREQ[2:0] = 0b001$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		11.25		kHz

### Electrical Characteristics—Load Switch Driver (LSW3) (continued)

( $V_{SYS} = 3.6V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested. This section is applicable when  $OTP\_INRUSH\_DISABLE = 1$  and  $LSW\_OTP\_SEL = 1$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
0.03125x Gate Drive Oscillator Frequency	$f_{LSW3\_DRV\_0.03125X}$	$OTP\_INR\_FREQ[2:0] = 0b000$ , $V_{SYS} = 3.3V$ , $V_{SYS} = 5V$		5.625		kHz
Gate Drive Discharge Resistance	$R_{LSW\_GDRV\_DIS}$	Resistance from LSW3_DRV to FBLSW3, $V_{LSW3\_DRV-FBLSW3} = 4V$		74		$\Omega$
		Resistance from LSWx_DRV to FBLSWx, $V_{LSWx\_DRV-FBLSWx} = 3.3V$		100		
<b>TIMING</b>						
Soft-Start Done Time	$t_{SS\_DONE\_LSW}$	Duration from MOSFET drive circuit being enabled to the internal soft-start done signal being asserted. Based on default gate drive frequency ( $f_{LSW3\_DRV\_FREQ}$ ) selected by ( $OTP\_INR\_FREQ[2:0]$ ), to program the default gate drive frequency		512		cycles of $f_{LSW3\_DRV\_FREQ}$
<b>POWER-OK COMPARATOR</b>						
Output Power-OK Threshold	$V_{LSW3\_OUT\_POK\_INT}$	Rising edge, input to the load switch is either one of the four internal buck regulator outputs or $V_{SYS}$ as selected by LSW3_INP_EXT	0.85 x $V_{IN\_LSW3}$	0.90 x $V_{IN\_LSW3}$	0.95 x $V_{IN\_LSW3}$	V
Output Power-OK Hysteresis				3		%
Power-OK Response Time		$V_{SYS} = 3.3V$ , $V_{INLSWx} = 1.8V$ , LSWx is enabled, 100mV under-drive with falling slew rate of 150mV/ $\mu s$		1.20		$\mu s$
Power-OK Comparator Active Current	$I_{Q\_POK\_LSWx}$	$V_{SYS} = 3.3V$ , $V_{INLSWx} = 1.8V$ , LSWx is enabled		1.1		$\mu A$

## Electrical Characteristics—Linear Regulator

( $V_{SYS} = 3.6V$ ,  $V_{IN\_LDO} = 3.6V$ ,  $V_{OUT\_LDO} = 1.8V$ ,  $C_{IN\_LDO} = 1\mu F$ ,  $C_{OUT\_LDO} = 2.2\mu F$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GENERAL CHARACTERISTICS</b>						
Input Voltage Range	$V_{IN\_LDO}$	Guaranteed by Output Voltage Accuracy tests (Notes 11, 12)	1.7		$V_{SYS}$	V
LDO Shutdown IN_LDO Current	$I_{IN\_LDO}$	Current measured into IN_LDO, LDO output disabled, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ . Production tested in combination with other blocks as shown in the <i>OFF State Quiescent Current</i> parameter of the <i>Electrical Characteristics—Linear Regulator</i> table		<0.1	1	$\mu A$
LDO Shutdown SYS Current	$I_{SYS}$	Current measured into IN_LDO, LDO output disabled, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ . Production tested in combination with other blocks as shown in the global resources " <i>OFF State Quiescent Current</i> " parameter		<0.1		$\mu A$
LDO Normal Mode Quiescent Supply IN_LDO Current (Not in Dropout)	$I_{IN\_LDO}$	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ , $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ . Production tested in a combination with all other blocks as shown in the global resources " <i>ON State Quiescent Current</i> " parameter		16	20	$\mu A$
LDO Normal Mode Quiescent Supply SYS Current (Not in Dropout)	$I_{SYS}$	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ , $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ . Production tested in combination with other blocks as shown in the global resources " <i>ON State Quiescent Current</i> " parameter		5	7	$\mu A$
LDO Normal Mode Quiescent Supply IN_LDO Current (In Dropout)	$I_{IN\_LDO}$	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 2.0V$ , $V_{OUT\_LDO\_TARGET} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ (Note 13)		20		$\mu A$
LDO Normal Mode Quiescent Supply SYS Current (In Dropout)	$I_{SYS}$	Normal mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 2.0V$ , $V_{OUT\_LDO\_TARGET} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ (Note 13)		5		$\mu A$

### Electrical Characteristics—Linear Regulator (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IN\_LDO} = 3.6V$ ,  $V_{OUT\_LDO} = 1.8V$ ,  $C_{IN\_LDO} = 1\mu F$ ,  $C_{OUT\_LDO} = 2.2\mu F$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO Low-Power Mode Quiescent Supply IN_LDO Current (Not in Dropout)	$I_{IN\_LDO}$	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ , $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ . Production tested in combination with other blocks as shown in the global resources "DEVSLP State Quiescent Current" parameter		2	3	$\mu A$
LDO Low-Power Mode Quiescent Supply SYS Current (Not in Dropout)	$I_{SYS}$	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ , $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ .		2	3	$\mu A$
LDO Low-Power Mode Quiescent Supply IN_LDO Current (In Dropout)	$I_{IN\_LDO}$	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 2.0V$ , $V_{OUT\_LDO\_TARGET} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ (Note 13)		1.5		$\mu A$
LDO Low-Power Mode Quiescent Supply SYS Current (In Dropout)	$I_{SYS}$	Low-power mode of operation, current measured into IN_LDO, LDO output enabled and in regulation, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 2.0V$ , $V_{OUT\_LDO\_TARGET} = 2.5V$ , $I_{OUT\_LDO} = 0mA$ (Note 13)		2.5		$\mu A$
Maximum Output Current	$I_{OUT\_LDO}$	Normal-power mode (Note 14)	150			mA
		Low-power mode (Note 14)	5			
Output Current Limit		Normal-power mode, $V_{OUT\_LDO}$ set for 3.2V and loaded down to 90% of set output voltage (Note 15)	165	300		mA
		Low-power mode, $V_{OUT\_LDO}$ set for 3.2V and loaded down to 90% of set output voltage		40		
Output Capacitance for Stability	$C_{LDO\_OUT}$	ESR must be less than 200m $\Omega$ , ESL is less than 20nH	1.1	2.2	20	$\mu F$
<b>OUTPUT VOLTAGE RANGE</b>						
Minimum Programmable Output Voltage		TV_LDO[6:0] = 0b0000000		0.8		V
Maximum Programmable Output Voltage		TV_LDO[6:0] = 0b1111111		3.975		V
Output DAC Bits				7		Bits
Output DAC LSB Size				25		mV

### Electrical Characteristics—Linear Regulator (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IN\_LDO} = 3.6V$ ,  $V_{OUT\_LDO} = 1.8V$ ,  $C_{IN\_LDO} = 1\mu F$ ,  $C_{OUT\_LDO} = 2.2\mu F$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC CHARACTERISTICS</b>						
Output Voltage Accuracy		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 1.7V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 150mA$ , normal-power mode	-2		+2	%
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 1.7V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 5mA$ , low-power mode	-6.5		+6.5	
		$V_{SYS} = 2.8V$ , $V_{IN\_LDO} = 2.8V$ , $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 150mA$ , normal-power mode	-2		+2	
		$V_{SYS} = 2.8V$ , $V_{IN\_LDO} = 2.8V$ , $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 5mA$ , low-power mode	-6.5		+6.5	
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 5.5V$ , $V_{OUT\_LDO} = 3.975V$ , $I_{OUT\_LDO} = 0.1mA$ , normal-power mode	-2		+2	
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 5.5V$ , $V_{OUT\_LDO} = 3.975V$ , $I_{OUT\_LDO} = 0.1mA$ , low-power mode	-6.5		+6.5	
Line Regulation		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 1.7V$ to $5.5V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 0.1mA$ , normal-power mode		0.05		%/ $V$
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 1.7V$ to $5.5V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 0.1mA$ , low-power mode		0.05		
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 4.4V$ to $5.5V$ , $V_{OUT\_LDO} = 3.975V$ , $I_{OUT\_LDO} = 0.1mA$ , normal-power mode		0.05		
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 4.4V$ to $5.5V$ , $V_{OUT\_LDO} = 3.975V$ , $I_{OUT\_LDO} = 0.1mA$ , low-power mode		0.05		
Load Regulation		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 1.7V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 0.1mA$ to $150mA$ , normal-power mode		0.5		%
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 1.7V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 0.1mA$ to $5mA$ , low-power mode		0.5		
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 3.975V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 0.1mA$ to $150mA$ , normal-power mode		0.5		
		$V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 3.975V$ , $V_{OUT\_LDO} = 0.8V$ , $I_{OUT\_LDO} = 0.1mA$ to $5mA$ , low-power mode		0.5		

### Electrical Characteristics—Linear Regulator (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IN\_LDO} = 3.6V$ ,  $V_{OUT\_LDO} = 1.8V$ ,  $C_{IN\_LDO} = 1\mu F$ ,  $C_{OUT\_LDO} = 2.2\mu F$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise		Normal-power mode, $f = 10\text{Hz}$ to $100\text{kHz}$ , $I_{LDO\_OUT} = 15\text{mA}$ , $V_{SYS} = 2.7V$ , $V_{IN\_LDO} = 1.7V$ , $V_{LDO} = 0.8V$		100		$\mu V_{RMS}$
		Normal-power mode, $f = 10\text{Hz}$ to $100\text{kHz}$ , $I_{LDO\_OUT} = 15\text{mA}$ , $V_{SYS} = 2.7V$ , $V_{IN\_LDO} = 1.7V$ , $V_{LDO} = 1.0V$		150		
		Normal-power mode, $f = 10\text{Hz}$ to $100\text{kHz}$ , $I_{LDO\_OUT} = 15\text{mA}$ , $V_{SYS} = 2.7V$ , $V_{IN\_LDO} = 2.7V$ , $V_{LDO} = 2.0V$		200		
		Normal-power mode, $f = 10\text{Hz}$ to $100\text{kHz}$ , $I_{LDO\_OUT} = 15\text{mA}$ , $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 3.6V$ , $V_{LDO} = 3.0V$		300		
		Normal-power mode, $f = 10\text{Hz}$ to $100\text{kHz}$ , $I_{LDO\_OUT} = 15\text{mA}$ , $V_{SYS} = 5.5V$ , $V_{IN\_LDO} = 5.5V$ , $V_{LDO} = 3.975V$		400		
<b>DYNAMIC CHARACTERISTICS</b>						
Power-Supply Rejection Ratio	PSRR	Normal-power mode, $V_{SYS} = 3.6V$ , $V_{IN\_LDO} = 2.8V + 20\text{mV}_{pp}$ , $f = 10\text{Hz}$ to $10\text{kHz}$ , $V_{OUT\_LDO} = 1.8V$ , $I_{OUT\_LDO} = 15\text{mA}$		60		dB
Line Transient		Normal-power mode, $V_{OUT\_LDO} = 1.2V$ , $I_{OUT\_LDO} = 1\text{mA}$ , $V_{SYS} = V_{IN\_LDO} = 3.6V$ to $3.2V$ to $3.6V$ with $5\mu s$ transition times		5		mV
		Normal-power mode, $V_{OUT\_LDO} = 1.2V$ , $I_{OUT\_LDO} = 1\text{mA}$ , $V_{SYS} = 3.6V$ , $V_{IN\_LDO} =$ $3.6V$ to $3.2V$ to $3.6V$ with $5\mu s$ transition times		5		
Load Transient		Normal-power mode, $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 1\text{mA}$ to $75\text{mA}$ to $1\text{mA}$ with $1\mu s$ transition times, $C_{OUT\_LDO} = 2.2\mu F$		$\pm 5$		%
		Normal-power mode, $V_{OUT\_LDO} = 2.5V$ , $I_{OUT\_LDO} = 1\text{mA}$ to $75\text{mA}$ to $1\text{mA}$ with $1\mu s$ transition times, $C_{OUT\_LDO} = 10\mu F$		$\pm 3$		
Output Over-Shoot During Startup				50		mV
<b>TIMING CHARACTERISTICS</b>						
Maximum Turn-On Delay		From the LDO receiving an enable signal to when the output voltage starts to rise		20		$\mu s$
Maximum Soft-Start Time		$V_{OUT\_LDO}$ from 10% to 90% of 2.5V final value		40		$\mu s$



## Electrical Characteristics—Linear Regulator (continued)

( $V_{SYS} = 3.6V$ ,  $V_{IN\_LDO} = 3.6V$ ,  $V_{OUT\_LDO} = 1.8V$ ,  $C_{IN\_LDO} = 1\mu F$ ,  $C_{OUT\_LDO} = 2.2\mu F$ , limits are 100% production tested at  $T_A = +25^\circ C$ , limits over the operating temperature range ( $T_A = -40^\circ C$  to  $+85^\circ C$ ) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER STAGE CHARACTERISTICS</b>						
Dropout Voltage	$V_{LDO\_DO}$	Normal-power mode, $V_{SYS} = 3.6V$ , 3.3V programmed output voltage, $V_{IN\_LDO} = 3.1V$ , $I_{OUT\_LDO} = 150mA$ (Note 13)		100	200	mV
		Normal-power mode, $V_{SYS} = 3.6V$ , 1.8V programmed output voltage, $V_{IN\_LDO} = 1.7V$ , $I_{OUT\_LDO} = 150mA$ (Note 13)		100		
Disabled Output Impedance	$R_{AD\_LDO}$	Regulator disabled, active-discharge enabled ( $ADE\_LDO = 1$ ) (Note 16)	50	100	150	$\Omega$
Disabled Output Leakage Current		Regulator disabled, active-discharge disabled ( $ADE\_LDO = 0$ ), $V_{SYS} = V_{IN\_LDO} = 5.5V$ , $V_{OUT\_LDO} = 5.5V$ and $0V$ , $T_A = +25^\circ C$ (Note 17)	-1.0	$\pm 0.1$	+1.0	$\mu A$
<b>POWER-OK COMPARATOR</b>						
Output Power-OK Trim Level		Rising edge, $V_{OUT\_LDO} = 2.0V$	82.5	87.5	92.5	%
Output Power-OK Hysteresis		$V_{OUT\_LDO} = 2.0V$		3		%

**Note 11:** When the input voltage is within the specified range, the LDO tries to regulate the output voltage. However, the regulator may be in dropout. For example, if the output voltage is fixed at 1.85V and a 1.7V input is provided, the output is 1.7V minus the dropout voltage ( $V_{LDO} = V_{IN\_LDO} - V_{LDO\_DO}$ ). To achieve the specified output voltage, the input voltage must be the output voltage plus the dropout voltage ( $V_{IN\_LDO} \geq V_{LDO} + V_{LDO\_DO\_MAX}$ ).

**Note 12:**  $V_{IN\_LDO}$  must be lower than or equal to  $V_{SYS}$ . The  $V_{SYS}$  maximum operating voltage range is 5.5V. For example, if  $V_{SYS}$  is 4.2V, then the maximum voltage for  $V_{IN\_LDO}$  is 4.2V. Similarly, if  $V_{SYS}$  is 5.5V, then the maximum voltage for  $V_{IN\_LDO}$  is 5.5V.

**Note 13:** The dropout voltage is the difference between the input voltage and the output voltage, when the input voltage is inside the specified "input voltage" range but below the "output voltage" set point. For example, if the output voltage set point is 1.85V, the input voltage is 1.7V, and the actual output voltage is 1.65V, then the dropout voltage is 50mV ( $V_{LDO\_DO} = V_{IN\_LDO} - V_{OUT\_LDO}$ ).

**Note 14:** The "Maximum Output Current" is guaranteed by the "Output Voltage Accuracy" tests.

**Note 15:** Current limit is provided for thermal concerns as a system fail safe feature, minor (50mA) oscillations of current when the LDO is at current limit are normal. Over process corner current limit is not expected to exceed 560mA.

**Note 16:** There is an n-channel MOSFET in series with the output active discharge resistance. This NMOS requires  $V_{SYS} > 1.2V$  to be enhanced.

**Note 17:** Guaranteed by design and characterization but not directly production tested. The ability to disconnect the active discharge resistance is functionally checked in a production test.

## Electrical Characteristics—I<sup>2</sup>C Interface

(T<sub>A</sub> = -40°C to +85°C (unless otherwise specified), V<sub>IO</sub> = 1.8V, V = 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
VIO Voltage Range	V <sub>IN_VIO_I2C</sub>		1.7		3.6	V
<b>SDA AND SCL I/O STAGE</b>						
SCL, SDA Input HIGH Voltage	V <sub>IH</sub>	V <sub>IN_VIO_I2C</sub> = 1.7V to 3.6V	0.7 x V <sub>IN_VIO_I2C</sub>			V
SCL, SDA Input LOW Voltage	V <sub>IL</sub>	V <sub>IN_VIO_I2C</sub> = 1.7V to 3.6V			0.3 x V <sub>IN_VIO_I2C</sub>	
SCL, SDA Input Hysteresis	V <sub>HYS</sub>		0.1 x V <sub>IN_VIO_I2C</sub>			V
SCL, SDA Input Leakage Current	I <sub>I</sub>	V <sub>IN_VIO_I2C</sub> = 3.6V, V <sub>SCL</sub> = V <sub>SDA</sub> = 0V and 3.6V	-10		+10	μA
SDA Output LOW Voltage	V <sub>OL</sub>	IOL = 20mA			0.4	V
SCL, SDA Pin Capacitance	C <sub>I</sub>		10			pF
Output Fall Time from V <sub>IH</sub> to V <sub>IL</sub>	t <sub>OF</sub>	(Note 18)			120	ns
Internal Pullup	R <sub>PU_SDA</sub> , R <sub>PU_SCL</sub>	OTP_INT_PU[0] = 0b0	Open			kΩ
		Pulled up to V <sub>IN_VIO_I2C</sub> , OTP_INT_PU[0] = 0b1	2.5	5.0	7.5	
<b>WATCHDOG TIMER</b>						
Watchdog Timer Period	t <sub>WD</sub>		35			ms
<b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (Note 18)</b>						
Clock Frequency	f <sub>SCL</sub>		0		1000	kHz
Bus Free Time between STOP and START Condition	t <sub>BUF</sub>		0.5			μs
Hold Time (REPEATED) START Condition	t <sub>HD;STA</sub>		0.26			μs
SCL LOW Period	t <sub>LOW</sub>		0.5			μs
SCL HIGH Period	t <sub>HIGH</sub>		0.26			μs
Setup Time REPEATED START Condition	t <sub>SU_STA</sub>		0.26			μs

### Electrical Characteristics—I<sup>2</sup>C Interface (continued)

(T<sub>A</sub> = -40°C to +85°C (unless otherwise specified), V<sub>IO</sub> = 1.8V, V = 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA Hold Time	t <sub>HD_DAT</sub>	Receive mode	0			μs
DATA Setup Time	t <sub>SU_DAT</sub>		50			ns
Setup Time for STOP Condition	t <sub>SU_STO</sub>		0.26			μs
Data Valid Time	t <sub>VD_DAT</sub>	Transmit mode			0.45	μs
Data Valid Acknowledge Time	t <sub>VD_ACK</sub>				0.45	μs
Bus Capacitance	C <sub>B</sub>				550	pF
Pulse Width of Suppressed Spikes	t <sub>SP</sub>		50			ns
<b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C<sub>B</sub> = 100pF) (Note 18)</b>						
Clock Frequency	f <sub>SCL</sub>				3.4	MHz
Hold Time (REPEATED) START Condition	t <sub>HD_STA</sub>		160			ns
Setup Time REPEATED START Condition	t <sub>SU_STA</sub>		160			ns
SCL LOW Period	t <sub>LOW</sub>		160			ns
SCL HIGH Period	t <sub>HIGH</sub>		60			ns
DATA Hold Time	t <sub>HD_DAT</sub>		0			ns
DATA Setup Time	t <sub>SU_DAT</sub>		10			ns
SCL Rise Time	t <sub>rCL</sub>	T <sub>A</sub> = +25°C (Note 18)	10		40	ns
Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit	t <sub>rCL1</sub>	T <sub>A</sub> = +25°C (Note 18)	10		80	ns
SCL Fall Time	t <sub>fCL</sub>	T <sub>A</sub> = +25°C (Note 18)	10		40	ns
SDA Rise Time	t <sub>rDA</sub>	T <sub>A</sub> = +25°C (Note 18)	10		80	ns
SDA Fall Time	t <sub>fDA</sub>	T <sub>A</sub> = +25°C (Note 18)			80	ns
Setup Time for STOP Condition	t <sub>SU_STO</sub>		160			ns
Bus Capacitance	C <sub>B</sub>				100	pF
Pulse Width of Suppressed Spikes	t <sub>SP</sub>			10		ns

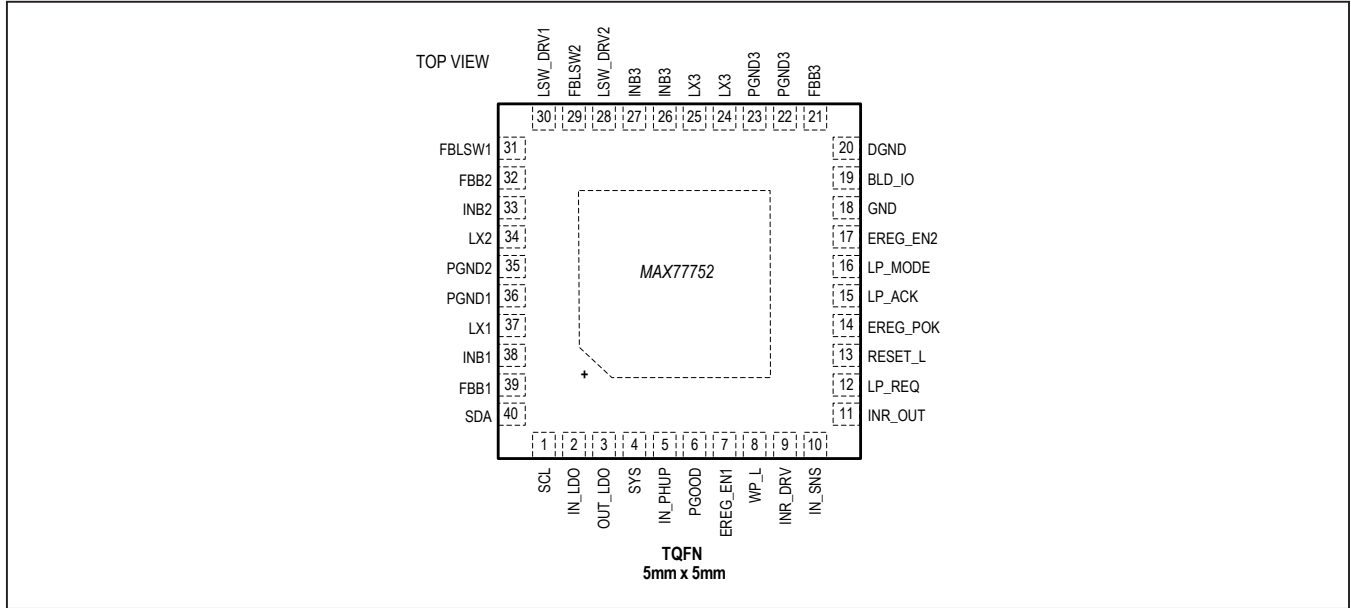
### Electrical Characteristics—I<sup>2</sup>C Interface (continued)

(T<sub>A</sub> = -40°C to +85°C (unless otherwise specified), V<sub>IO</sub> = 1.8V, V = 3.6V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>I<sup>2</sup>C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, C<sub>B</sub> = 400pF) (Note 18)</b>						
Clock Frequency	f <sub>SCL</sub>				1.7	MHz
Hold Time (REPEATED) START Condition	t <sub>HD_STA</sub>		160			ns
Setup Time REPEATED START Condition	t <sub>SU_STA</sub>		160			ns
SCL LOW Period	t <sub>LOW</sub>		320			ns
SCL HIGH Period	t <sub>HIGH</sub>		120			ns
DATA Hold Time	t <sub>HD_DAT</sub>		0			ns
DATA Setup Time	t <sub>SU_DAT</sub>		10			ns
SCL Rise Time	t <sub>rCL</sub>	T <sub>A</sub> = +25°C (Note 18)	20		80	ns
Rise Time of SCL Signal after REPEATED START Condition and after Acknowledge bit	t <sub>rCL1</sub>	T <sub>A</sub> = +25°C (Note 18)	20		160	ns
SCL Fall Time	t <sub>fCL</sub>	T <sub>A</sub> = +25°C (Note 18)	20		80	ns
SDA Rise Time	t <sub>rDA</sub>	T <sub>A</sub> = +25°C (Note 18)	20		160	ns
SDA Fall Time	t <sub>fDA</sub>	T <sub>A</sub> = +25°C (Note 18)			160	ns
Setup Time for STOP Condition	t <sub>SU_STO</sub>		160			ns
Bus Capacitance	C <sub>B</sub>				400	pF
Pulse Width of Suppressed Spikes	t <sub>SP</sub>			10		ns

**Note 18:** Minimum typical and maximum values are guaranteed by design. Not production tested.

Pin Configuration



Pin Description

PIN	NAME	FUNCTION	TYPE
<b>TOP</b>			
9	INR_DRV	External Inrush FET Gate Drive. Inrush MOSFET Gate Driver. When using the inrush control feature, connect INR_DRV to the gate of an external NMOS. If the inrush feature is not required, this pin can also be configured as LSW3_DRV using LSW_OTP_SEL = 1. If either use cases do not apply, leave INR_DRV unconnected or connect to ground ONLY after ensuring that the inrush controller is disabled by the appropriate OTP option.	Analog Output
10	IN_SNS	Input Voltage Sense (Preswitch). Input Voltage Sense. When using the inrush control feature, connect IN_SNS to the drain of an external n-channel MOSFET. When the inrush control feature is not needed, connect IN_SNS to V <sub>SYS</sub> .	Power Input
11	INR_OUT	Inrush Control Output Sense. This pin must be connected to the source of the inrush control MOSFET. If the inrush controller is not required, this pin can also be configured as FBLSW3 by setting LSW_OTP_SEL = 1. If either use cases do not apply, then this pin must be connected to the SYS node.	Power Input
4	SYS	System Power Input. SYS is the voltage sense input for the inrush controller, system voltage monitors, and other analog circuits. Connect SYS to the same power source as that meant for the voltage regulators in the PMIC. When using the inrush control feature, connect SYS to the source of an external n-channel MOSFET whose drain is connected to the main power input. When the inrush control feature is not needed, connect SYS to IN_SNS. Regardless of the inrush controller configuration, SYS must connect to the buck regulator power inputs (INB1, INB2, INB3).	Power Input

## Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
18	GND	Ground. GND carries ground current for "quiet" control circuits. GND also carries the current for the OTP programming circuit when the programming sequence is executed.	Ground
8	WP_L	Write Protect (Open Drain, Active Low) to memory. Connect this pin to the appropriate pin on the memory. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal V <sub>IN_VIO</sub> node.	Digital Output
15	LP_ACK	Low-Power Mode Acknowledge from controller. Connect LP_ACK to the appropriate pin on the controller. LP_ACK acknowledges the LP_REQ output signal in master mode (OTP_SLP_MSTRSLV = 0) by asserting high, which initiates the transition to DevSlp state. LP_ACK initiates the transition to DevSlp state independently in slave mode (OTP_SLP_MSTRSLV = 1) by asserting high. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal V <sub>IN_VIO</sub> node.	Digital Input
13	RESET_L	Reset Output (Open Drain, Active Low) to controller. Connect to the reset input of the controller. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Output
6	PGOOD	Power Good Output (Open Drain, Active High). PGOOD indicates the status of all regulators controlled by the PMIC (internal and external) and asserts LOW if any regulator's individual Power-OK (POK) signal is deasserted. Additionally, it also asserts low if the system voltage (V <sub>SYS</sub> ) falls below the brownout threshold. Connect PGOOD to the appropriate pin on the controller. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Output
7	EREG_EN1	External Regulator #1 Enable Output. EREG_EN1 is an open-drain output with optional internal pullup resistor. EREG_EN1 is typically used to drive the enable pin of an external regulator.	Digital Output
17	EREG_EN2	External Regulator #2 Enable Output. EREG_EN2 is an open-drain output with optional internal pullup resistor. EREG_EN2 is typically used to drive the enable pin of an external regulator.	Digital Output
14	EREG_POK	External Regulator Power-OK Input. EREG_POK is a digital input. In the typical application, EREG_POK is derived from the POK outputs of the external regulators that are enabled/disabled by EREG_EN1 and EREG_EN2.	Digital Input
16	LP_MODE	Low-Power Mode Input to PMIC from Connector in Master Mode (OTP_SLP_MSTRSLV = 0). When in slave mode (OTP_SLP_MSTRSLV = 1), it is recommended to connect LP_MODE to ground or to a power supply such that it is logic high. Open-Drain Output. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Input
12	LP_REQ	Open-Drain (Active High) Output. Low-power mode request to controller in master mode in alternate mode (OTP_SLP_MSTRSLV = 0). Open-Drain Output. An optional 100kΩ internal pullup resistor is available which is pulled up to an internal node.	Digital Output

## Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
20	DGND	Digital Ground. DGND carries ground current for digital circuits such as the I <sup>2</sup> C.	Ground
19	BLD_IO	BLD_IO Pin is a Dedicated Open-Drain Input/Output Pin. In an application, this active-low input discharges the supply rail during a powerup cycle. This pin also senses the voltage on the pin it is connected to, and the function is to discharge a rail lower than 100mV. Connect this pin to GND when this feature is not required in the system.	Analog I/O
5	IN_PHUP	IN_PHUP is a Dedicated Analog Input Pin. This pin is connected to the output of the power holdup IC. In case of a power-fail event, the voltage on this pin drives the internal logic block to sustain the holdup function by maintaining the logic levels of the appropriate pins.	Power Input
<b>LDO</b>			
2	IN_LDO	Input Power for LDO (150mA). Bypass with a 2.2 $\mu$ F ceramic capacitor to GND with the following parasitic constraints (including capacitor and PCB parasitics) of ESR<100m $\Omega$ and ESL<30nH. If the LDO is not used, it is recommended to connect IN_LDO to OUT_LDO and connect them to ground.	Power Input
3	OUT_LDO	150mA PMOS LDO Output. Bypass with a 2.2 $\mu$ F capacitor to GND. If the LDO is not used, it is recommended to either ground OUT_LDO or leave it unconnected.	Power output
<b>BUCK</b>			
38	INB1	BUCK1 Power Input. INB1 is the shared drain connection of BUCK1's main power FET. Connect both INB1 pins together and to the power input to the system. INB1 is a critical discontinuous current node that requires careful PCB layout.	Power Input
37	LX1	BUCK1 Switching Node. Connect the required inductor between LX and the output capacitor. Both LX1 pins must be connected together. LX1 is a critical node that requires careful PCB layout.	Power I/O
36	PGND1	BUCK1 Power Ground are Internally Combined. PGND1 is the source connection of BUCK1's synchronous rectifier. PGND1 is a critical discontinuous current node that requires careful PCB layout.	Ground
39	FBB1	BUCK1 Output Voltage Feedback Node. Connect FBB1 to the local output capacitor at the buck output. In addition to setting the output-voltage regulation threshold, FBB1 can also be programmed to discharge the output capacitor when the converter is shutdown. FBB1 is a critical analog input that requires careful PCB layout.	Analog Input
33	INB2	BUCK2 Power Input. INB2 is the shared drain connection of BUCK2's main power FET. Connect both INB2 pins together and to the power input to the system. INB2 is a critical discontinuous current node that requires careful PCB layout.	Power Input

## Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
34	LX2	BUCK2 Switching Node. Connect the required inductor between LX and the output capacitor. LX2 is a critical node that requires careful PCB layout.	Power I/O
35	PGND2	BUCK2 Power Ground are Internally Combined. PGND2 is the source connection of BUCK2's synchronous rectifier. PGND2 is a critical discontinuous current node that requires careful PCB layout.	Ground
32	FBB2	BUCK2 Output Voltage Feedback Node. Connect FBB2 to the local output capacitor at the buck output. In addition to setting the output-voltage regulation threshold, FBB2 can also be programmed to discharge the output capacitor when the converter is shutdown. FBB2 is a critical analog input that requires careful PCB layout.	Analog Input
26,27	INB3	BUCK3 Power Input. INB3 is the drain connection of BUCK3's main power FET. Connect to the power input to the system. INB3 is a critical discontinuous current node that requires careful PCB layout.	Power Input
24,25	LX3	BUCK3 Switching Node. Connect the required inductor between LX and the output capacitor. LX3 is a critical node that requires careful PCB layout.	Power I/O
21	FBB3	BUCK3 Output Voltage Feedback Node. Connect FBB3 to the local output capacitor at the Buck output. In addition to setting the output voltage regulation threshold, FBB3 may also be programmed to discharges the output capacitor when the converter is shutdown. FBB3 is a critical analog input that requires careful PCB layout.	Analog Input
22, 23	PGND3	BUCK3 Power Ground. PGND2 is the shared source connection of BUCK3's synchronous rectifier. Connect both PGND3 pins together. PGND3 is a critical discontinuous current node that requires careful PCB layout.	Ground
<b>I<sup>2</sup>C</b>			
40	SDA	Serial Interface Data Bidirectional Open Drain. An optional 5kΩ internal pullup resistor is available which is pulled up to an internal V <sub>IN_VIO_I2C</sub> node. If the part is in Off state due to HICCUP_CNT_EXPIRE = 1, the I <sup>2</sup> C power switches from V <sub>FBB1</sub> to V <sub>IN_PHUP</sub> . Otherwise, the pin is in Hi-Z state during Off condition.	Digital I/O
1	SCL	Serial Interface Port 0 Clock Input. Open-Drain Output. An optional 5kΩ internal pullup resistor is available which is pulled up to an internal V <sub>IN_VIO_I2C</sub> node. If the part is in Off state due to HICCUP_CNT_EXPIRE = 1, the I <sup>2</sup> C power switches from V <sub>FBB1</sub> to V <sub>IN_PHUP</sub> . Otherwise, the pin is in Hi-Z state during Off condition.	Digital Input



## Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
<b>LOAD SWITCH</b>			
30	LSW_DRV1	Gate Drive for Load Switch 1. Connect to the gate of an external n-channel MOSFET used as the load switch. If the load switch is not used, LSW_DRV1 must be left unconnected.	Analog Output
28	LSW_DRV2	Gate Drive for LSW2. Connect to the gate of an external n-channel MOSFET used as the load switch. If the load switch is not used, LSW_DRV2 must be left unconnected.	Analog Output
31	FBLSW1	Feedback Input for Load-Switch Controller 1. FBLSW1 is an analog input to the load-switch controller which is used to control soft-start of the load switch and is the input to the output voltage monitor. Connect FBLSW1 to the output (source-side of n-channel MOSFET) of the load switch. If the load switch is not used, FBLSW1 can be left unconnected or tied to ground.	Analog Input
29	FBLSW2	Feedback Input for Load-Switch Controller 2. FBLSW2 is an analog input to the load-switch controller which is used to control soft-start of the load switch and is the input to the output voltage monitor. Connect FBLSW2 to the output (source-side of n-channel MOSFET) of the load switch. If the load switch is not used, FBLSW2 can be left unconnected or tied to ground.	Analog Input

## Detailed Description— Software Recommendations

Advice for optimizing software is provided throughout this data sheet within the context of the hardware descriptions. This section is dedicated to software recommendations and provides system level software guidance in order to optimally utilize the features of this device.

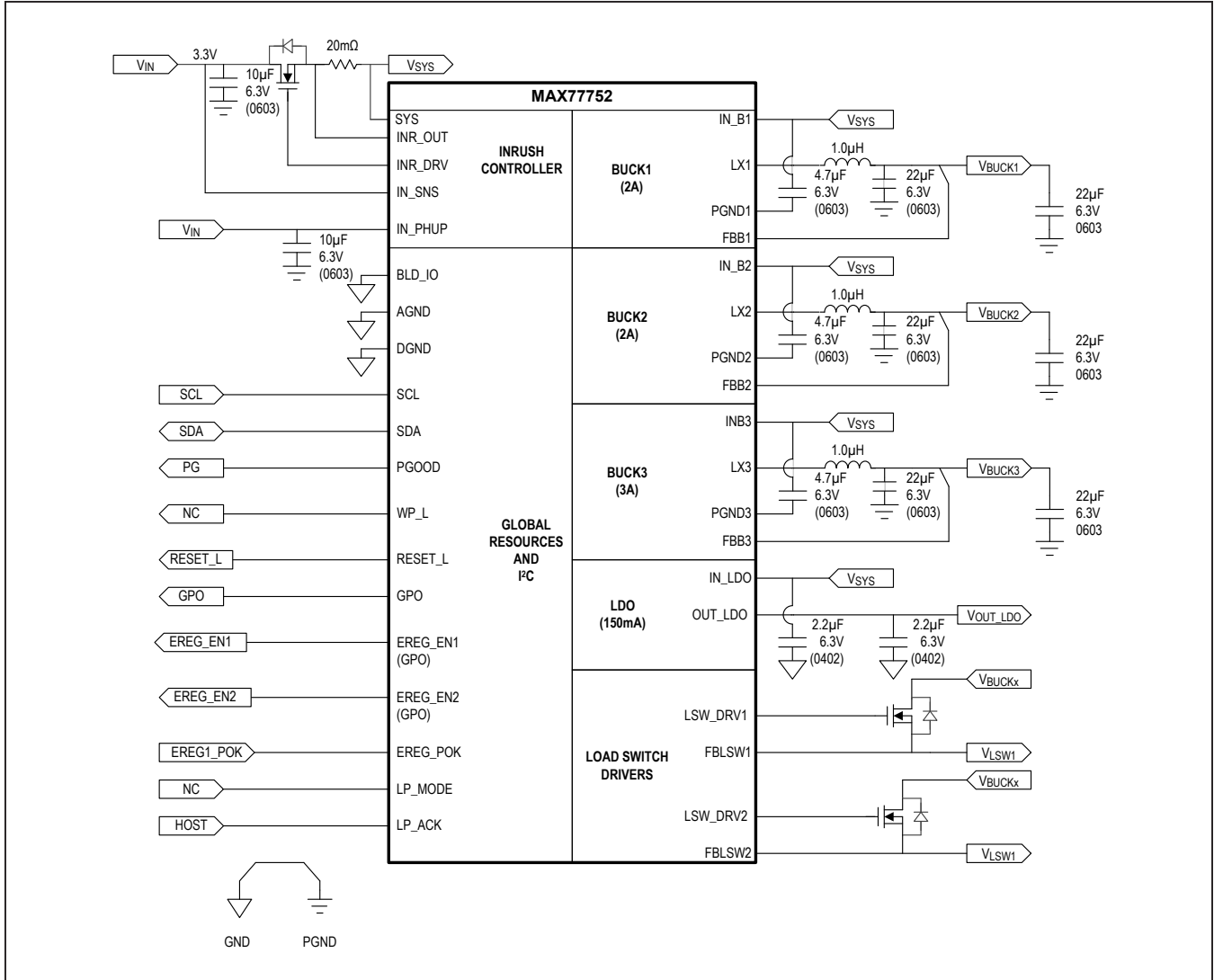
### OFF to ON Software Initialization

The system processor typically runs a set of initialization code each time a transition from the OFF to the ON state occurs, the reset output is deasserted (RESET\_L = 1), and the PGOOD is asserted (PGOOD = 1).

The following are recommended software steps within this initialization code:

- 1) Read the interrupt bits:
  - 1) Interrupt bits set at this point in time can indicate an issue that previously caused a shutdown.
- 2) Check the values of CID0, CID1, CID2, CID3, and CID4. Consider reporting these values if the product has some form of serial number checking utility. If the SBT bits do not read an appropriate value, then flag the product as bad and do not ship it. Only values of 0b011 and 0b101 should be shipped as production units. If the DRV bits do not match with what was intended for the given product, then flag that product as bad and do not ship it. This device has many OTP options and the DRV bits are set differently for each set of options. If parts got mixed up in the warehouse (i.e., A version confused for C version), then this step helps catch that mistake.
- 3) Set/Clear the mask bits as deemed appropriate for the target platform.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING	CID4
MAX77752AETL+	-40°C to +85°C	40 TQFN	MAX77752AETL+	0x07
MAX77752BETL+	-40°C to +85°C	40 TQFN	MAX77752BETL+	0x0D
MAX77752CETL+	-40°C to +85°C	40 TQFN	MAX77752CETL+	0x14
MAX77752DETL+	-40°C to +85°C	40 TQFN	MAX77752DETL+	0x15

+Denotes a lead(Pb)-free/RoHS-compliant package.

For a copy of the register map and for further questions, contact [techsupport@maximintegrated.com](mailto:techsupport@maximintegrated.com).

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	1/18	Added conditions statement to the <i>Electrical Characteristics—Current Sense Amplifier</i> table	14
2	1/18	Removed SSD and NAND from <i>Pin Description</i> table, added new part variant to <i>Ordering Information</i> table	38, 42
3	7/18	Updated <i>Ordering Information</i> table	42

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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