



# STP40NS15

N-CHANNEL 150V - 0.042Ω - 40A TO-220

MESH OVERLAY™ MOSFET

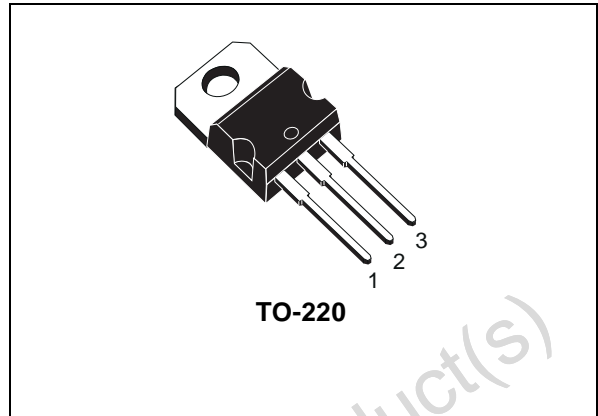
PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP40NS15	150 V	<0.052Ω	40A

- TYPICAL R<sub>DS(on)</sub> = 0.042Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

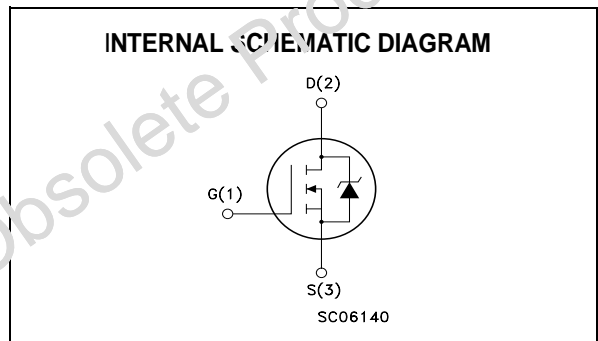
### DESCRIPTION

This powermos MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.



### APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- PRIMARY SWITCH IN ISOLATED DC-DC CONVERTERS



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	150	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	150	V
V <sub>GS</sub>	Gate-source Voltage	±20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	40	A
I <sub>C</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	25	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	160	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	140	W
	Derating Factor	0.933	W/°C
dv/dt	Peak Diode Recovery voltage slope	9	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(●)Pulse width limited by safe operating area

## STP40NS15

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.07	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.5	°C/W
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	40	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	500	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	150			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 40 A		0.044	0.052	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , V <sub>GS</sub> = 10V	40			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 20A		20		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2400		pF
C <sub>oss</sub>	Output Capacitance			380		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			160		pF

## ELECTRICAL CHARACTERISTICS (CONTINUED)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 75V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		25		ns
$t_r$	Rise Time			45		ns
$Q_g$	Total Gate Charge	$V_{DD} = 120V, I_D = 40A,$ $V_{GS} = 10V$		100	110	nC
$Q_{gs}$	Gate-Source Charge			17		nC
$Q_{gd}$	Gate-Drain Charge			47		nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 75V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		85		ns
$T_f$	Fall Time					
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{clamp} = 120V, I_D = 20A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		47		ns
$t_f$	Fall Time			35		ns
$t_c$	Cross-over Time			70		ns

## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				40	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				160	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 40A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$ (see test circuit, Figure 5)		270		ns
$Q_{rr}$	Reverse Recovery Charge			200		nC
$I_{RRM}$	Reverse Recovery Current			1.5		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

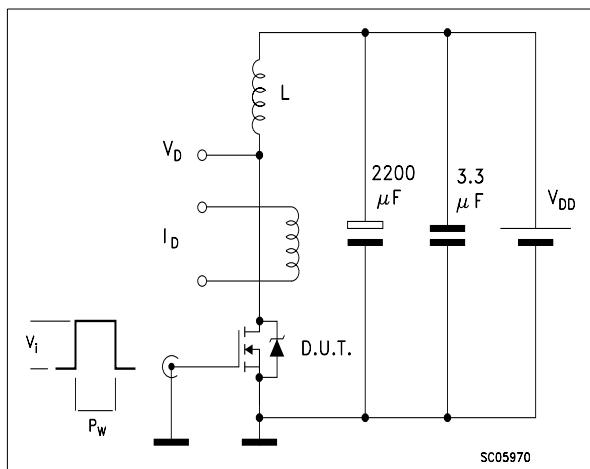


Fig. 2: Unclamped Inductive Waveform

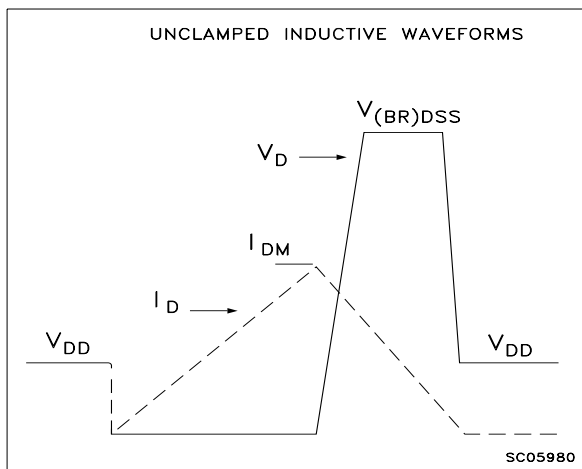


Fig. 3: Switching Times Test Circuit For Resistive Load

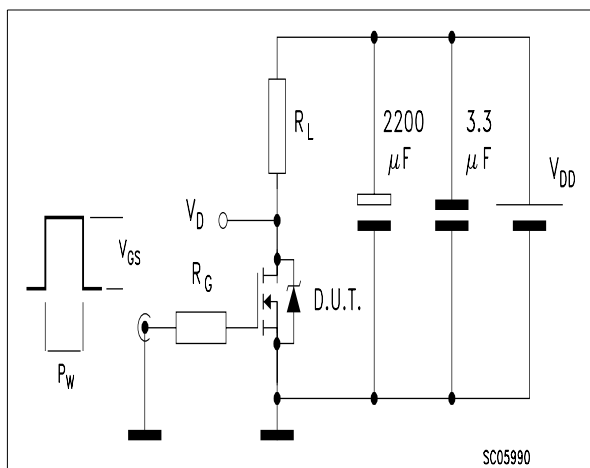


Fig. 4: Gate Charge test Circuit

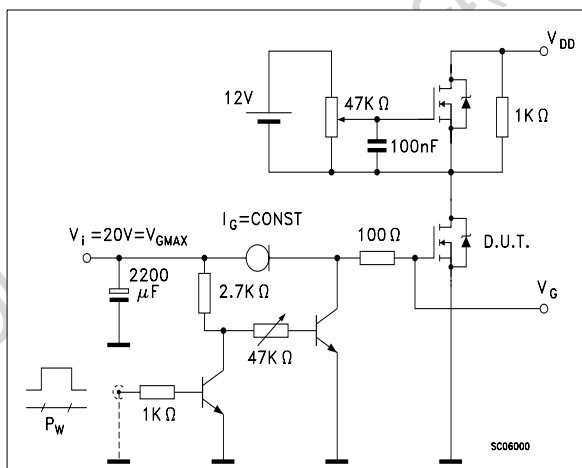
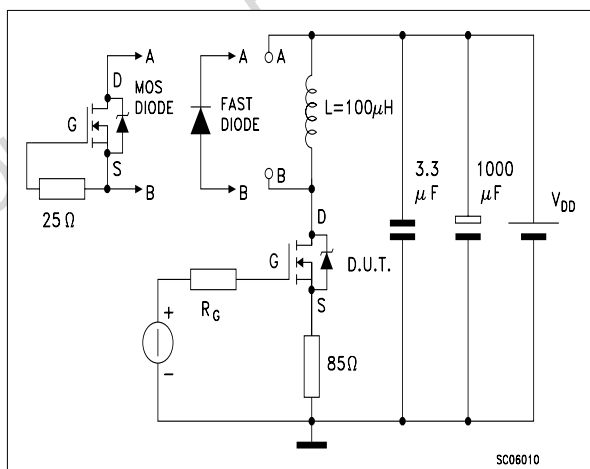
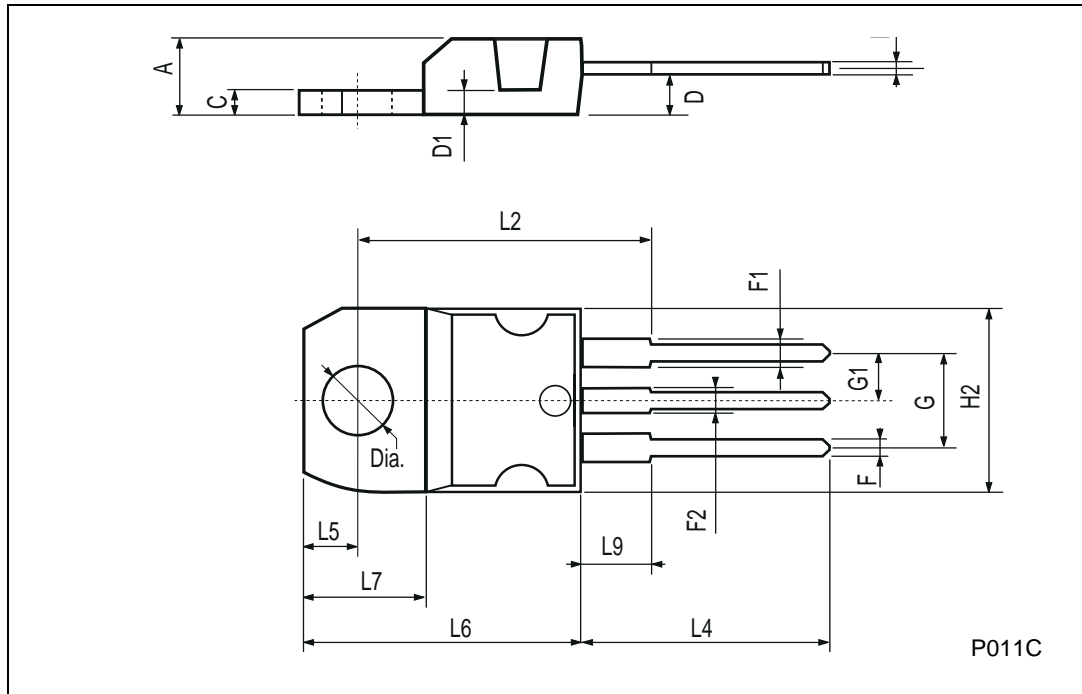


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -  
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>