

# NTB45N06, NTB45N06

## MOSFET – N-Channel, D<sup>2</sup>PAK 45 A, 60 V, 26 mΩ

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Higher Current Rating
- Lower  $R_{DS(on)}$
- Lower  $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter  $V_{SD}$  Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge
- AEC-Q101 Qualified and PPAP Capable – NTB45N06
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 10\text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	Vdc
– Continuous	$V_{GS}$	$\pm 30$	
– Non-Repetitive ( $t_p \leq 10\text{ ms}$ )			
Drain Current	$I_D$	45	Adc
– Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	30	
– Continuous @ $T_A = 100^\circ\text{C}$	$I_{DM}$	150	Apk
– Single Pulse ( $t_p \leq 10\text{ }\mu\text{s}$ )			
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	125	W
Derate above $25^\circ\text{C}$		0.83	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)		3.2	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		2.4	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50\text{ Vdc}$ , $V_{GS} = 10\text{ Vdc}$ , $R_G = 25\text{ }\Omega$ , $I_{L(pk)} = 40\text{ A}$ , $L = 0.3\text{ mH}$ , $V_{DS} = 60\text{ Vdc}$ )	$E_{AS}$	240	mJ
Thermal Resistance			$^\circ\text{C}/\text{W}$
– Junction-to-Case	$R_{\theta JC}$	1.2	
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	46.8	
– Junction-to-Ambient (Note 2)	$R_{\theta JA}$	63.2	
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1 in pad size, (Cu Area 1.127 in<sup>2</sup>).

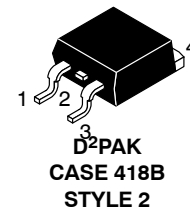
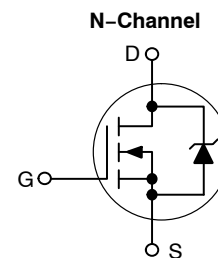


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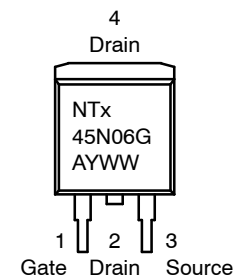
<http://onsemi.com>

45 AMPERES, 60 VOLTS

$R_{DS(on)} = 26\text{ m}\Omega$



### MARKING DIAGRAMS & PIN ASSIGNMENTS



NTx45N06 = Device Code  
 x = B or P  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

## **NTB45N06, NTB45N06**

2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

# NTB45N06, NTBV45N06

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 -	70 57	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0 -	2.8 7.2	4.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 22.5 Adc)	R <sub>DS(on)</sub>	-	21	26	mΩ
Static Drain-to-Source On-Voltage (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 45 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 22.5 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	- -	0.93 0.93	1.4 -	Vdc
Forward Transconductance (Note 3) (V <sub>DS</sub> = 8.0 Vdc, I <sub>D</sub> = 12 Adc)	g <sub>FS</sub>	-	16.6	-	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ISS</sub>	-	1224	1725	pF
Output Capacitance		C <sub>OSS</sub>	-	345	485	
Transfer Capacitance		C <sub>RSS</sub>	-	76	160	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 45 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 3)	t <sub>d(on)</sub>	-	10	25	ns
Rise Time		t <sub>r</sub>	-	101	200	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	33	70	
Fall Time		t <sub>f</sub>	-	106	220	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 45 Adc, V <sub>GS</sub> = 10 Vdc) (Note 3)	Q <sub>T</sub>	-	33	46	nC
		Q <sub>1</sub>	-	6.4	-	
		Q <sub>2</sub>	-	15	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I <sub>S</sub> = 45 Adc, V <sub>GS</sub> = 0 Vdc) (Note 3) (I <sub>S</sub> = 45 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	- -	1.08 0.93	1.2 -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 45 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	53.1	-	ns
		t <sub>a</sub>	-	36	-	
		t <sub>b</sub>	-	16.9	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.087	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

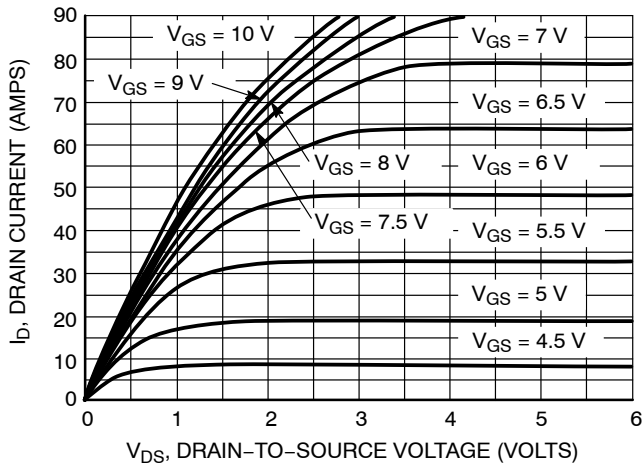
4. Switching characteristics are independent of operating junction temperatures.

### ORDERING INFORMATION

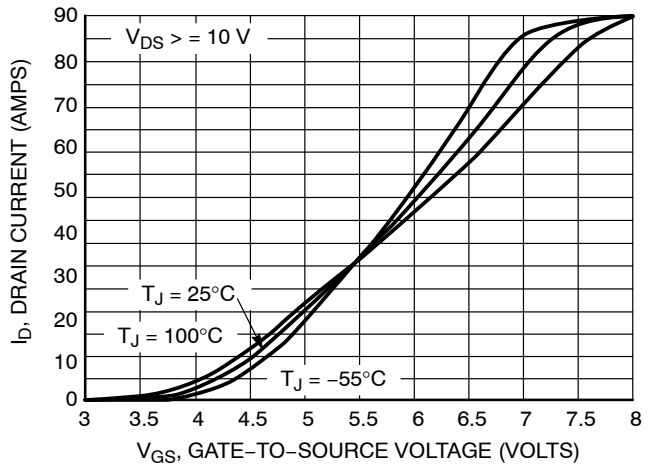
Device	Package	Shipping†
NTB45N06T4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel
NTBV45N06T4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

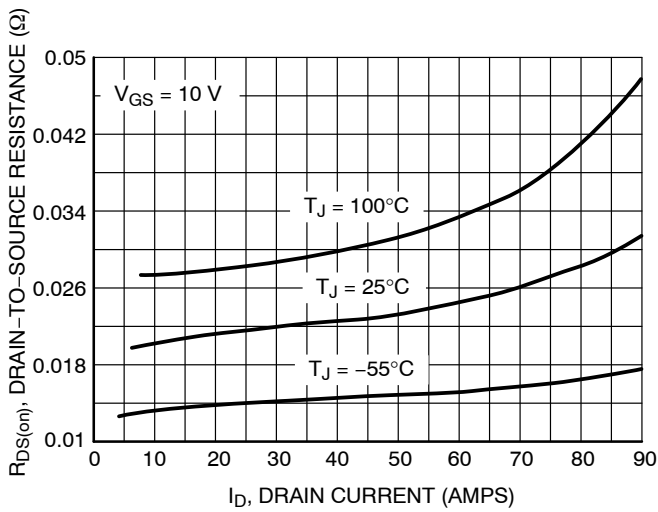
# NTB45N06, NTBV45N06



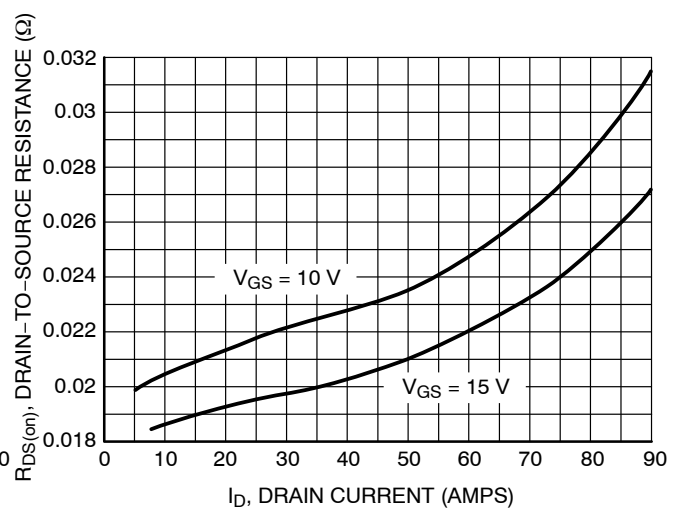
**Figure 1. On-Region Characteristics**



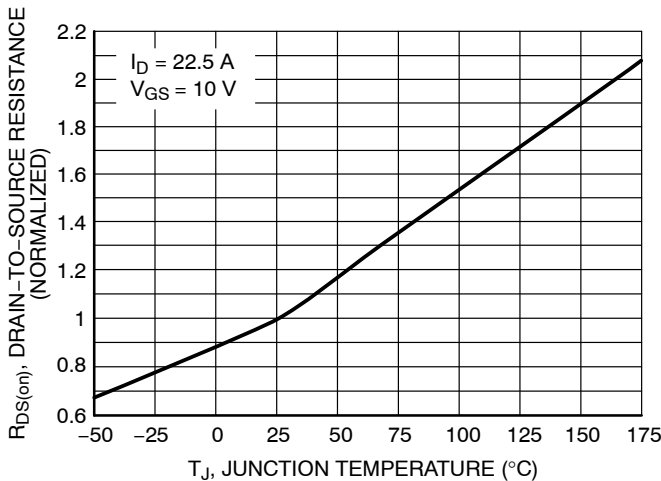
**Figure 2. Transfer Characteristics**



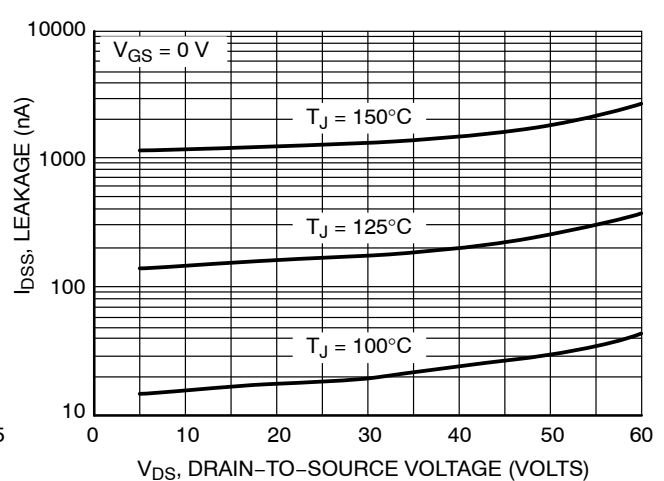
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**

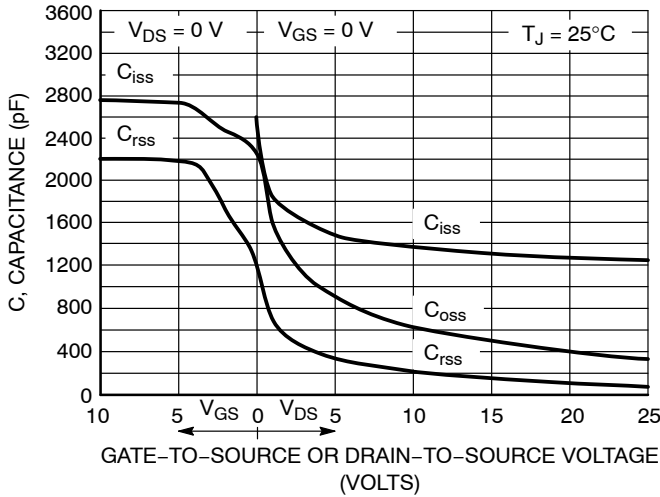


**Figure 5. On-Resistance Variation with Temperature**

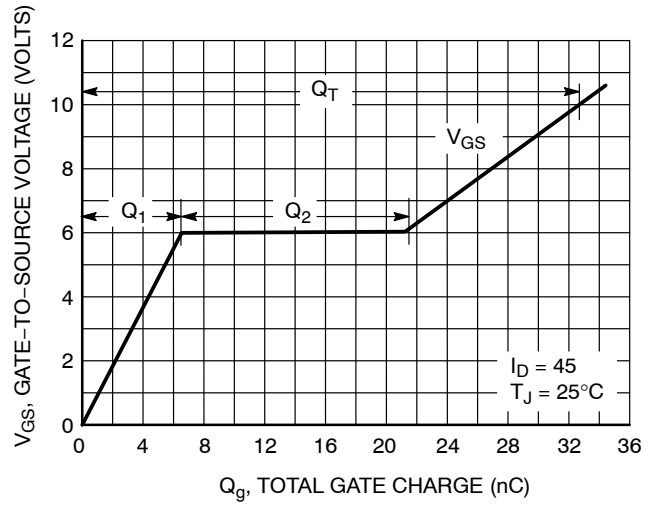


**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

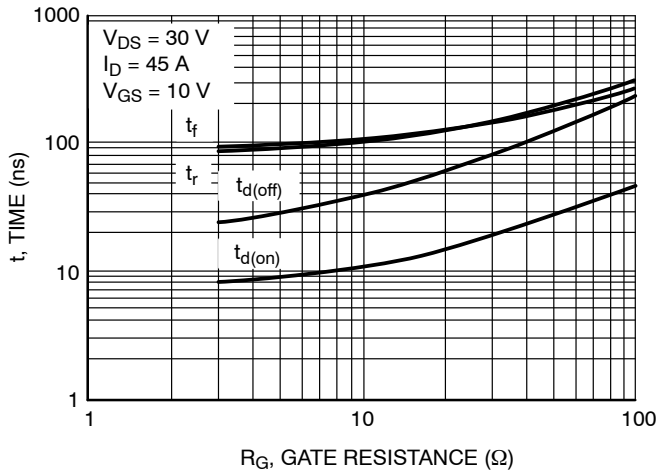
# NTB45N06, NTBV45N06



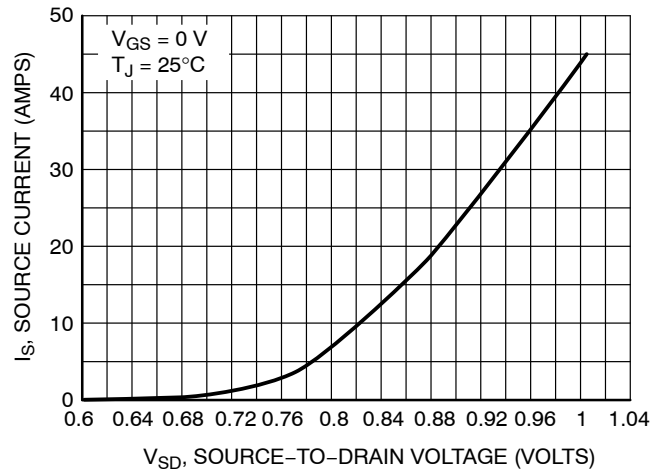
**Figure 7. Capacitance Variation**



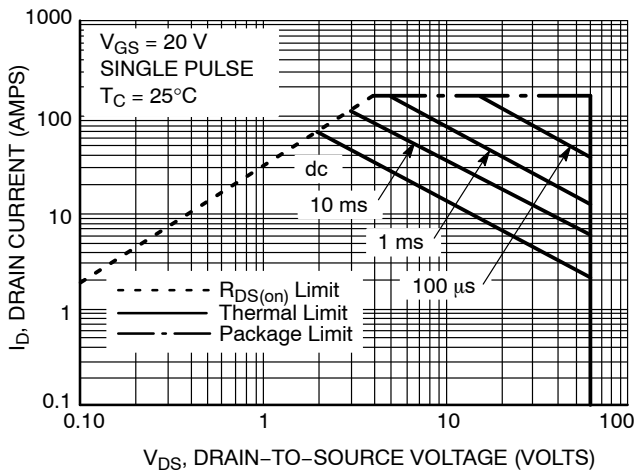
**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



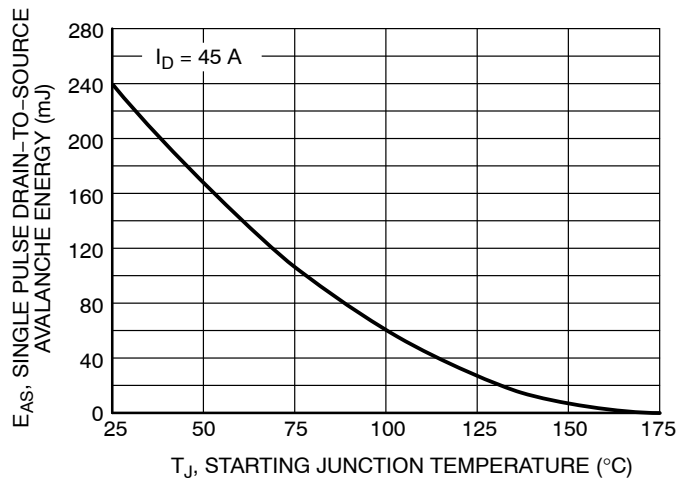
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

# NTB45N06, NTBV45N06

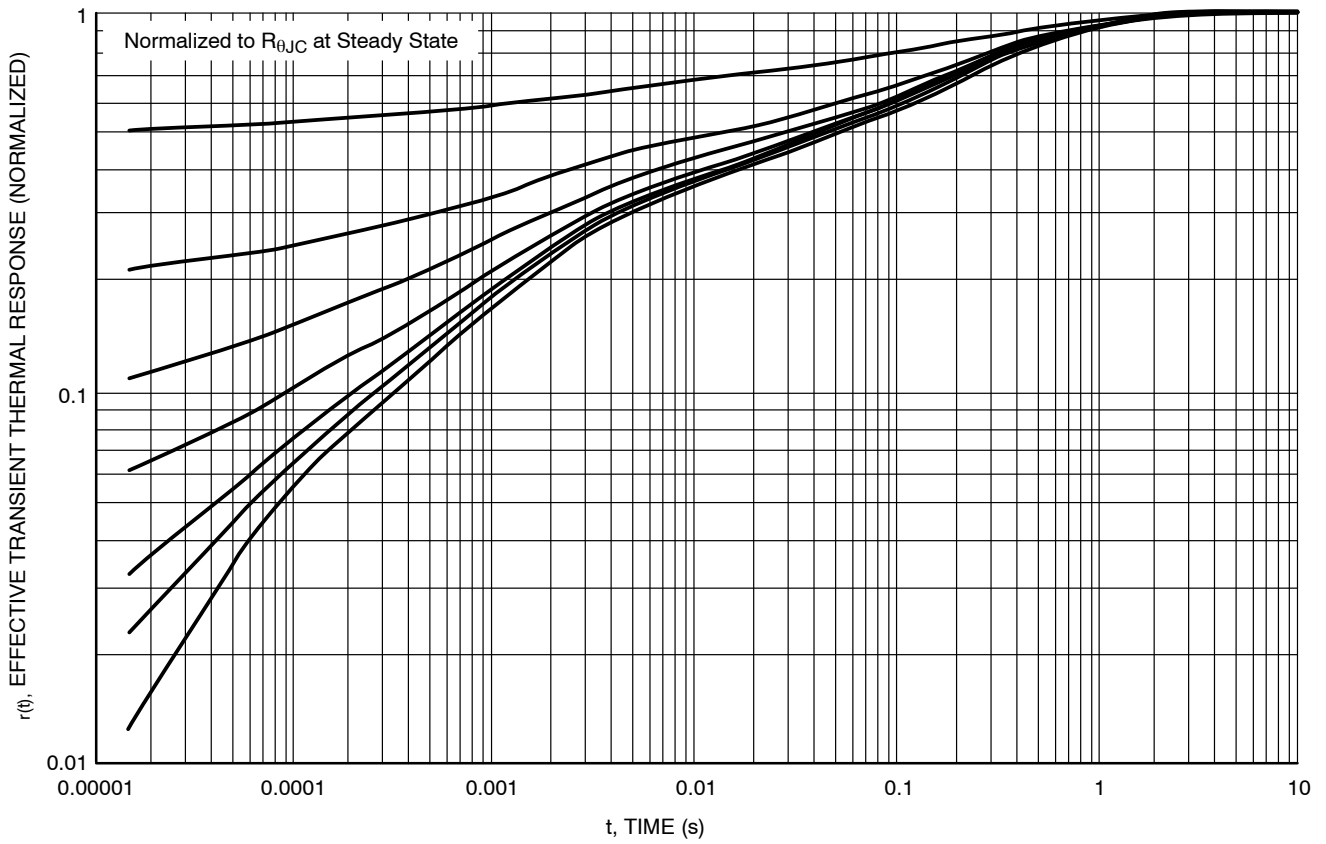


Figure 13. Thermal Response

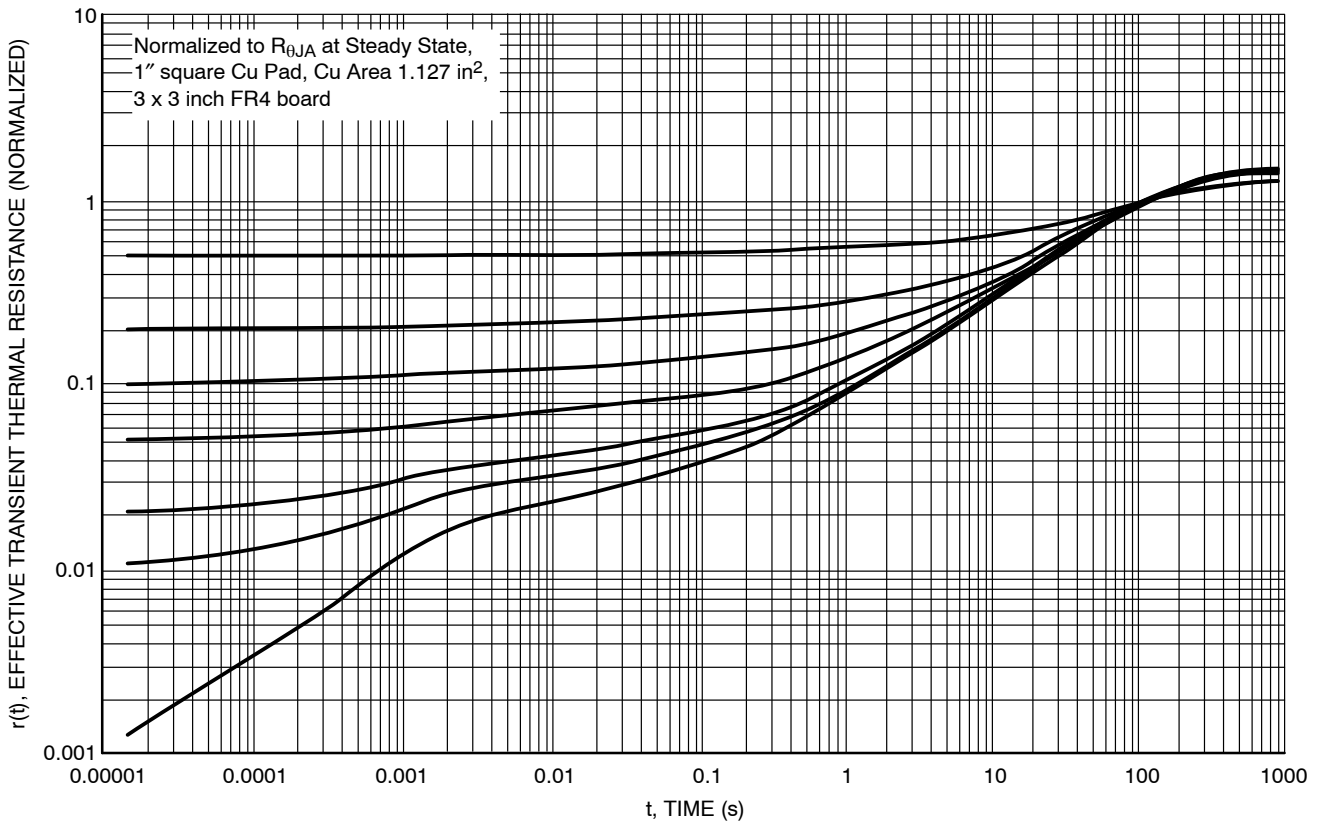
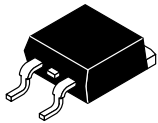


Figure 14. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

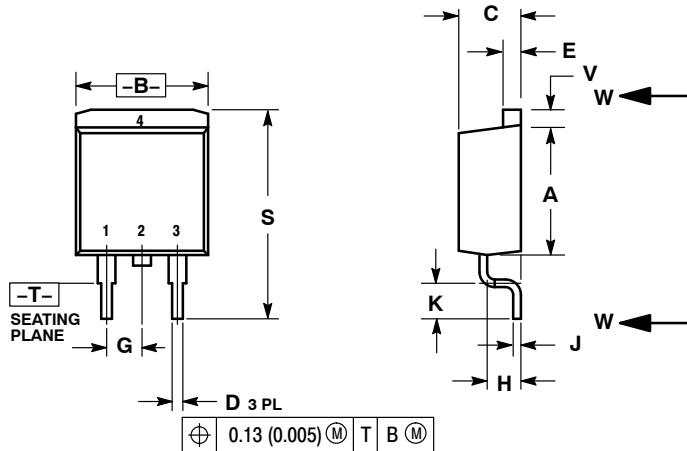
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

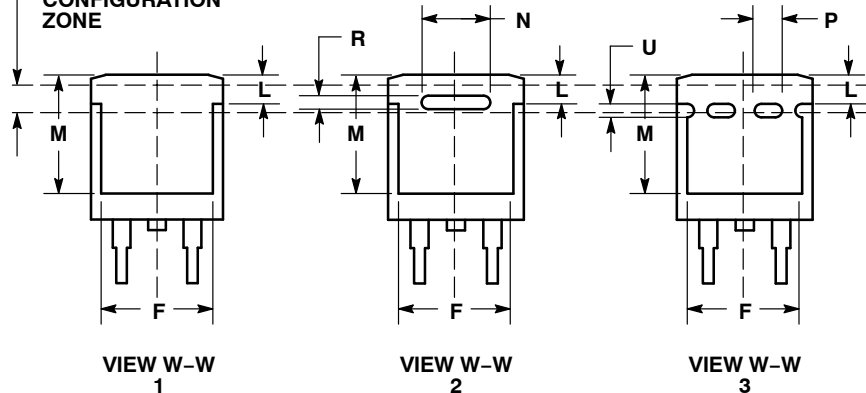


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

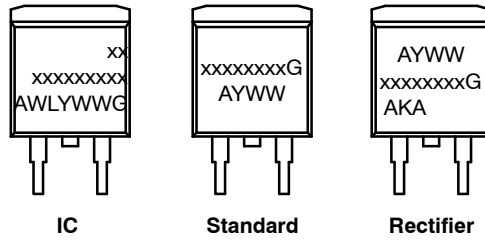
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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