Document Number: MD7IC2251N
Rev. 0, 5/2012

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

MD7IC2251NR1
MD7IC2251GNR1

2110–2170 MHz, 12 W AVG., 28 V
SINGLE W-CDMA
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

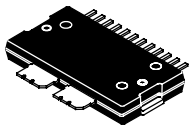
The MD7IC2251N wideband integrated circuit is designed with on-chip matching that makes it usable from 2110–2170 MHz. This multi-stage structure is rated for 26 to 32 volt operation and covers all typical cellular base station modulation formats.

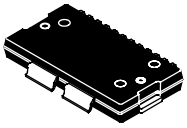
- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Volts, $I_{DQ1(A+B)}$ = 80 mA, I_{DQ2A} = 260 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 12 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	28.8	38.2	7.1	-34.6
2140 MHz	29.0	37.9	7.1	-36.2
2170 MHz	29.2	37.4	6.9	-36.1

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 63 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 3 dB Compression Point ≃ 58 Watts (1)

TO-270 WB-14
PLASTIC
MD7IC2251NR1





TO-270 WB-14 GULL
PLASTIC
MD7IC2251GNR1

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Production Tested in a Symmetrical Doherty Configuration
- Characterized with Large-Signal Load-Pull Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (2)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

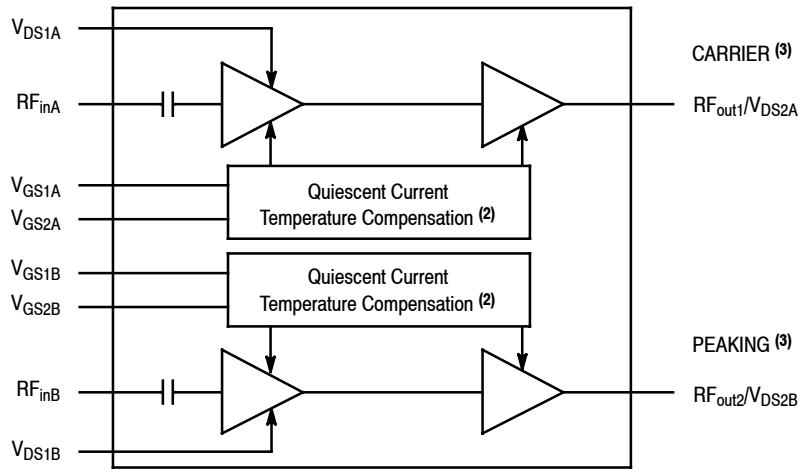
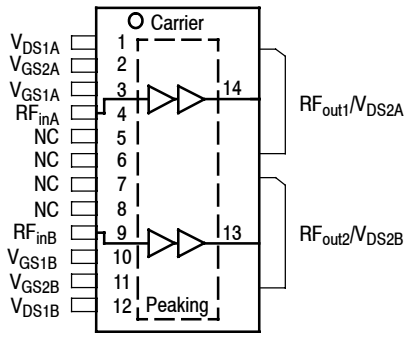


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.
3. Peaking and Carrier orientation is determined by the test fixture design.

freescale

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	28	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Final Doherty Application			
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 78°C, P_{out} = 12 W CW			
Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA		4.8	
Stage 2, 28 Vdc, I_{DQ2A} = 260 mA, V_{GS2B} = 1.4 Vdc		1.5	
Case Temperature 89°C, P_{out} = 50 W CW			
Stage 1, 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA		3.7	
Stage 2, 28 Vdc, I_{DQ2A} = 260 mA, V_{GS2B} = 1.4 Vdc		1.0	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	II

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 - Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 - On Characteristics (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 23 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	6.0	7.0	8.0	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 - Off Characteristics (1)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 1.5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 - On Characteristics (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	1.2	2.0	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2A} = 260 mAdc)	$V_{GSA(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2A} = 260 mAdc, Measured in Functional Test)	$V_{GGA(Q)}$	5.5	6.3	7.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.1	0.24	1.2	Vdc

Functional Tests (2,3,4) (In Freescale Doherty Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, I_{DQ2A} = 260 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 12 W Avg., f = 2140 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Power Gain	G_{ps}	27.6	28.2	32.0	dB
Power Added Efficiency	PAE	33.5	36.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.2	6.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.2	-31.5	dBc

Typical Broadband Performance (In Freescale Doherty Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, I_{DQ2A} = 260 mA, V_{GS2B} = 1.4 Vdc, P_{out} = 12 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	PAE (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	28.8	38.2	7.1	-34.6
2140 MHz	29.0	37.9	7.1	-36.2
2170 MHz	29.2	37.4	6.9	-36.1

1. Each side of device measured separately.
2. Part internally matched both on input and output.
3. Measurement made with device in a Symmetrical Doherty configuration.
4. Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (1) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, I_{DQ2A} = 260 mA, V_{GS2B} = 1.4 Vdc, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	40	—	W
P_{out} @ 3 dB Compression Point (2)	P3dB	—	58	—	W
IMD Symmetry @ 18 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	25	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	65	—	MHz
Quiescent Current Accuracy over Temperature with 4.7 kΩ Gate Feed Resistors (-30 to 85°C) (3) Stage 1 Stage 2	ΔI_{QT}	— —	1.5 5.0	— —	%
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 12 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.028	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.028	—	dB/°C

1. Measurement made with device in a Symmetrical Doherty configuration.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
3. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

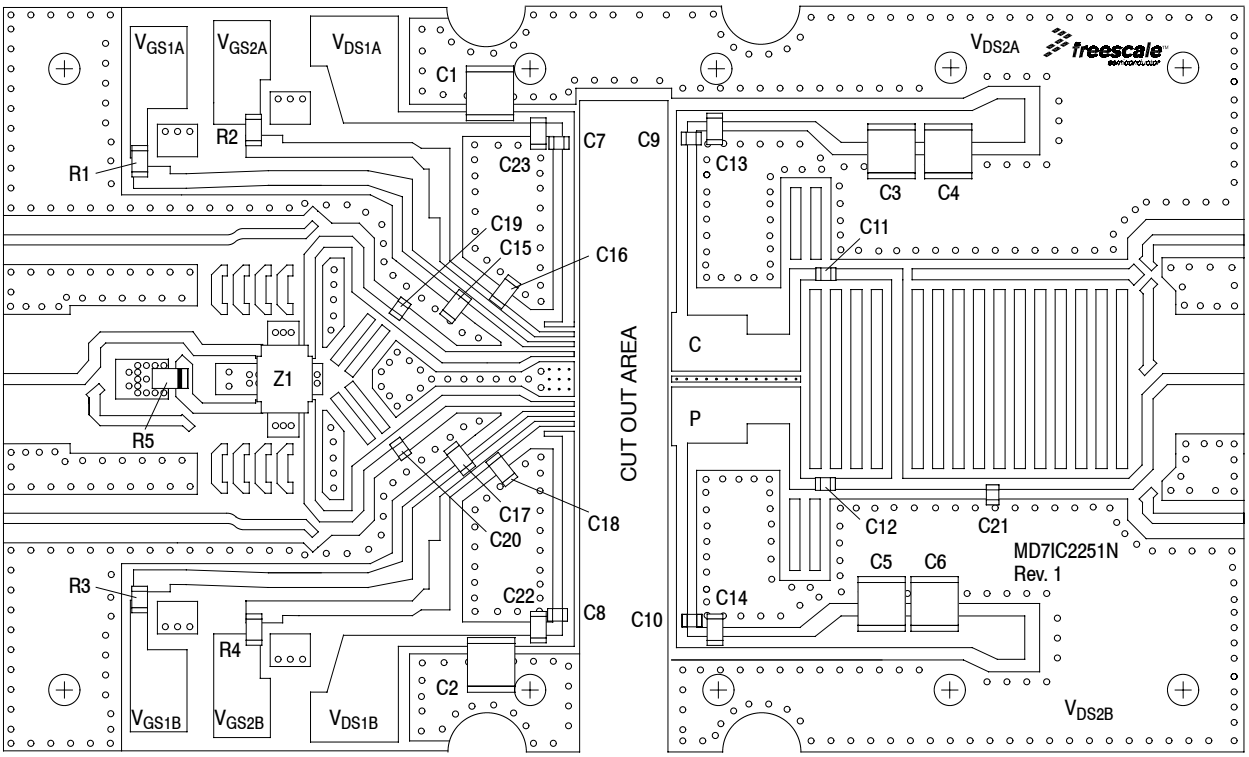


Figure 3. MD7IC2251NR1(GNR1) Production Test Circuit Component Layout

Table 6. MD7IC2251NR1(GNR1) Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C7, C8	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C9, C10	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C11, C12	39 pF Chip Capacitors	ATC600F390JT250XT	ATC
C13, C14, C15, C16, C17, C18	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C19, C20	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C21	0.9 pF Chip Capacitor	ATC600F0R9BT250XT	ATC
C22, C23	1.0 μF Chip Capacitors	GRM31CR71H105KA12L	Murata
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
R5	50 Ω, 10 W, Termination	RFP-06012A15Z50	Anaren
Z1	2100–2200 MHz, 90°, 3 dB Chip Hybrid Coupler	GSC355-HYB2150	Soshin
PCB	0.020″, ε_r = 3.5	RF-35A2	Taconic

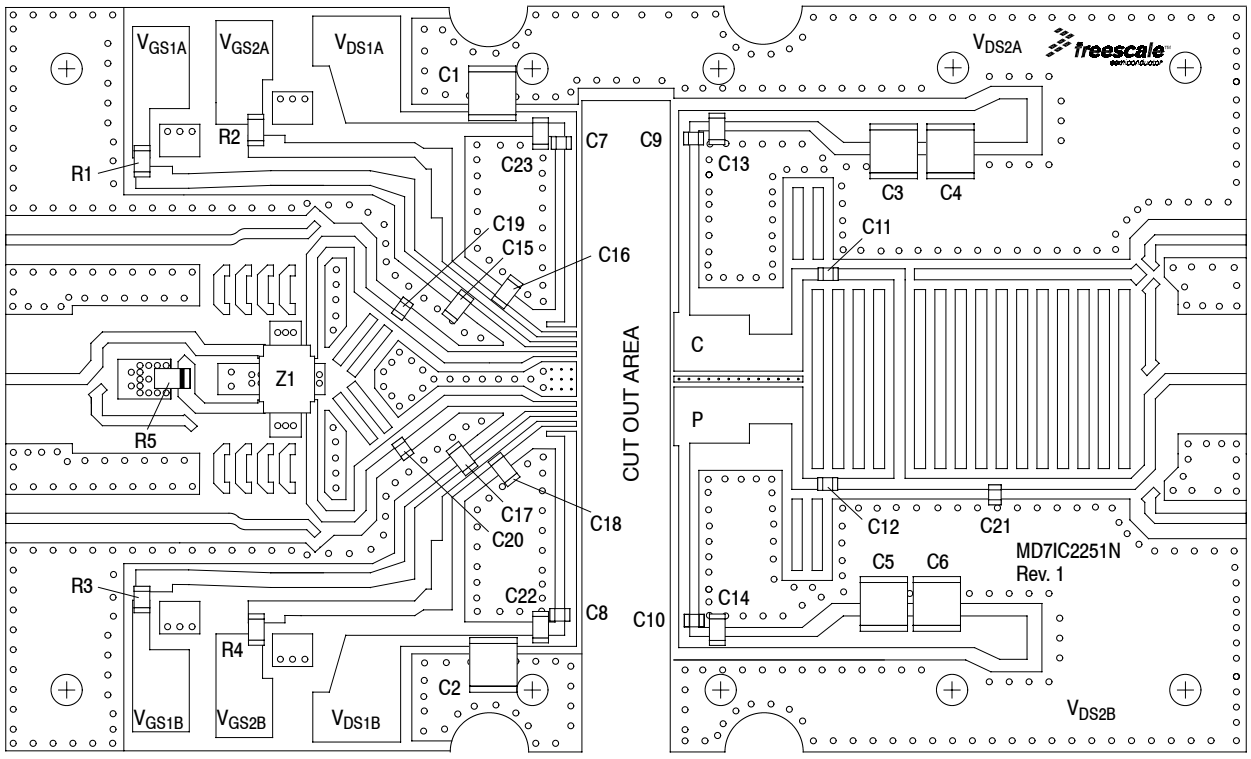


Figure 4. MD7IC2251NR1(GNR1) Characterization Test Circuit Component Layout

Table 7. MD7IC2251NR1(GNR1) Characterization Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	10 μF Chip Capacitors	GRM55DR61H106KA88L	Murata
C7, C8	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C9, C10	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C11, C12	39 pF Chip Capacitors	ATC600F390JT250XT	ATC
C13, C14, C15, C16, C17, C18	4.7 μF Chip Capacitors	GRM31CR71H475KA12L	Murata
C19, C20	0.5 pF Chip Capacitors	ATC600F0R5BT250XT	ATC
C21	0.9 pF Chip Capacitor	ATC600F0R9BT250XT	ATC
C22, C23	1.0 μF Chip Capacitors	GRM31CR71H105KA12L	Murata
R1, R2, R3, R4	4.7 kΩ, 1/4 W Chip Resistors	CRCW12064K70FKEA	Vishay
R5	50 Ω, 10 W, Termination	RFP-06012A15Z50	Anaren
Z1	2100–2200 MHz, 90°, 3 dB Chip Hybrid Coupler	GSC355-HYB2150	Soshin
PCB	0.020″, ε_r = 3.5	RF-35A2	Taconic

TYPICAL CHARACTERISTICS

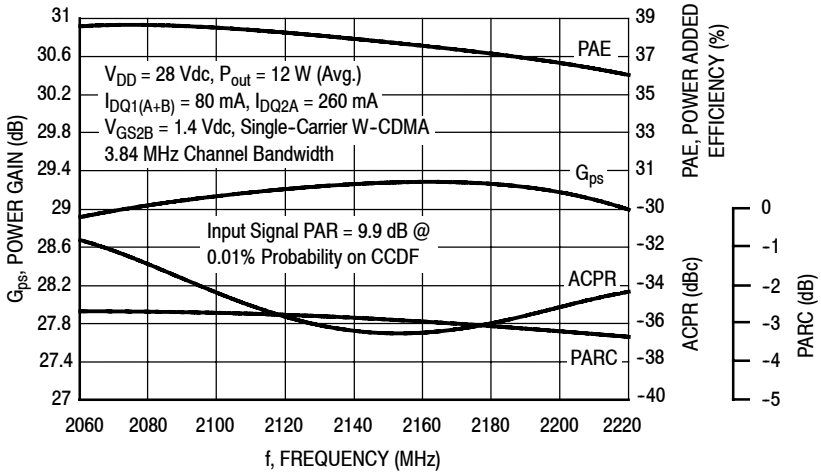


Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 12 Watts Avg.

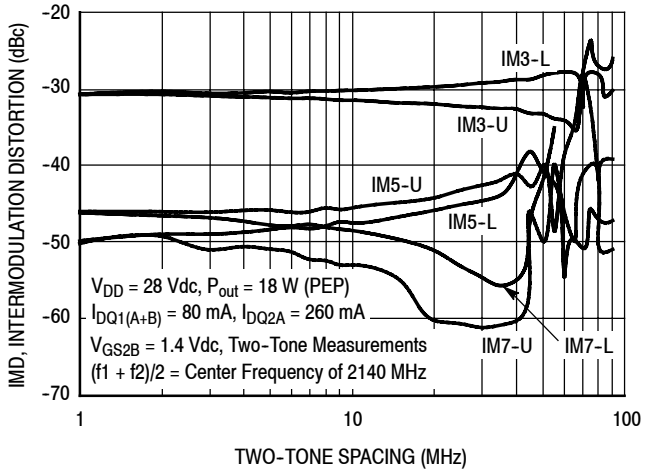


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

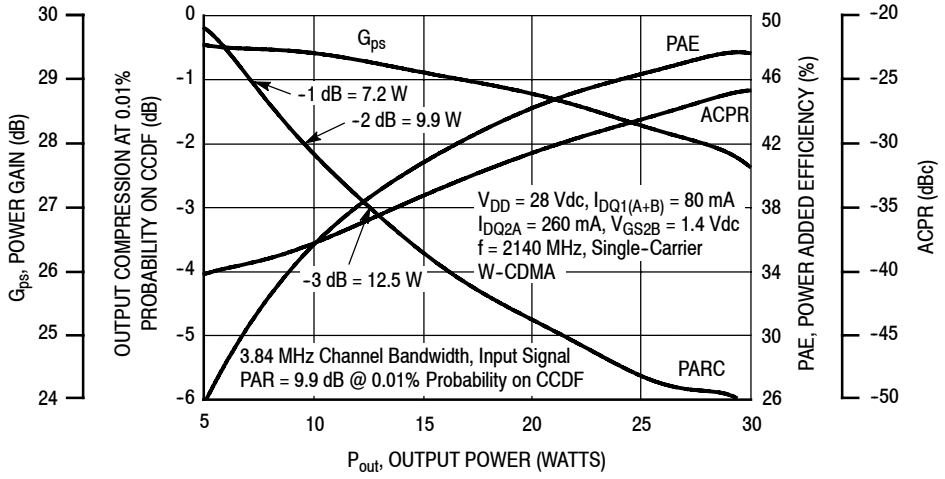


Figure 7. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

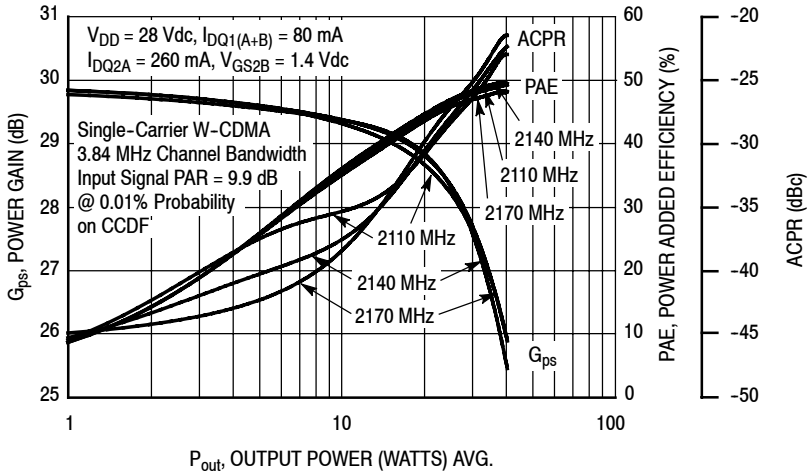


Figure 8. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power

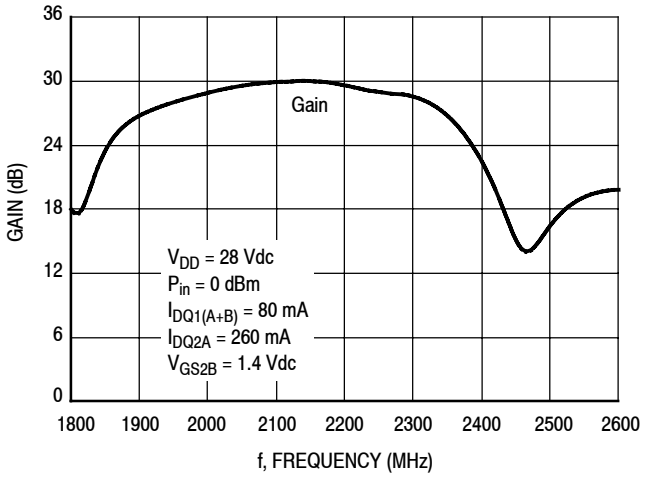


Figure 9. Broadband Frequency Response

W-CDMA TEST SIGNAL

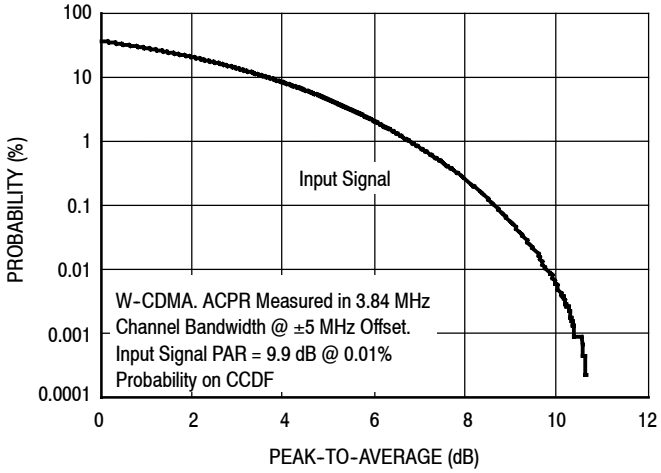


Figure 10. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

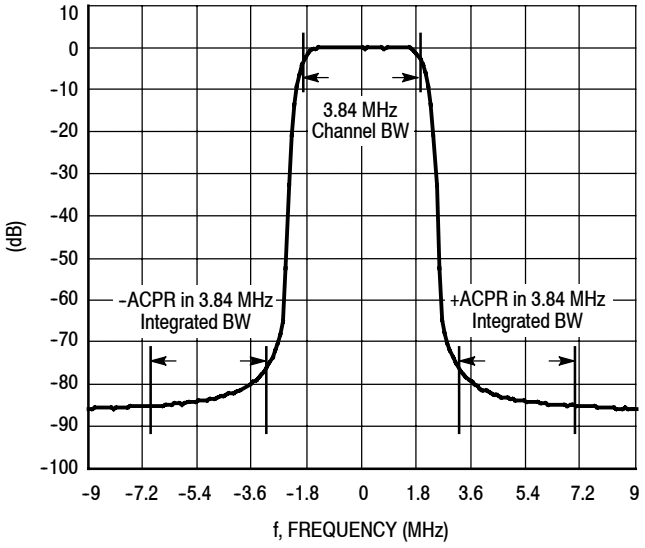


Figure 11. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, I_{DQ2A} = 260 mA, CW

f (MHz)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Output Power					
			P1dB			P3dB		
			(dBm)	(W)	PAE (%)	(dBm)	(W)	PAE (%)
2110	68.0 – j42.0	7.20 – j14.0	45.8	38	52.2	46.4	44	53.1
2140	60.6 – j37.0	7.40 – j14.4	45.7	37	51.9	46.4	44	52.7
2170	54.0 – j31.0	7.30 – j14.7	45.7	37	51.6	46.4	44	52.2

(1) Load impedance for optimum P1dB power.

Z_{in} = Impedance as measured from input contact to ground.
Z_{load} = Impedance as measured from drain contact to ground.

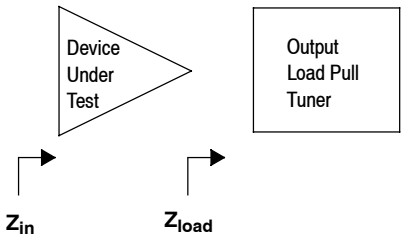


Figure 12. Carrier Side Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, $I_{DQ1(A+B)}$ = 80 mA, I_{DQ2A} = 260 mA, CW

f (MHz)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Power Added Efficiency					
			P1dB			P3dB		
			(dBm)	(W)	PAE (%)	(dBm)	(W)	PAE (%)
2110	60.0 – j53.0	9.10 – j8.80	44.4	28	58.1	45.0	32.0	57.6
2140	54.0 – j46.0	8.20 – j9.10	44.4	28	57.6	44.9	31.0	57.0
2170	48.0 – j39.0	7.90 – j9.60	44.4	28	57.4	45.0	32.0	56.7

(1) Load impedance for optimum P1dB efficiency.

Z_{in} = Impedance as measured from input contact to ground.
Z_{load} = Impedance as measured from drain contact to ground.

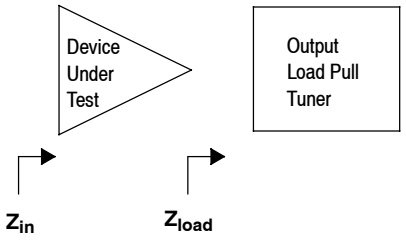
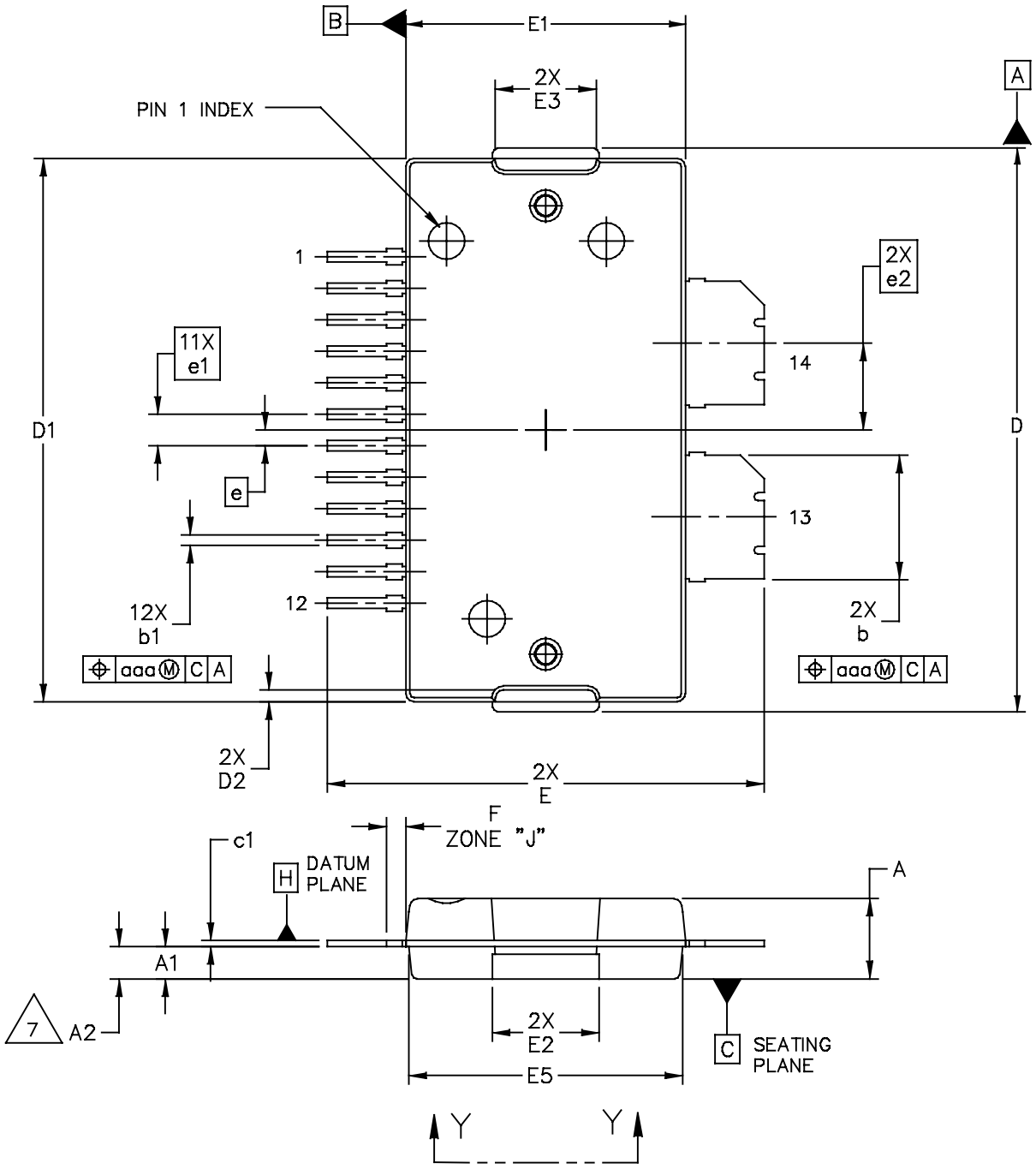


Figure 13. Carrier Side Load Pull Performance — Maximum Power Added Efficiency Tuning

PACKAGE DIMENSIONS



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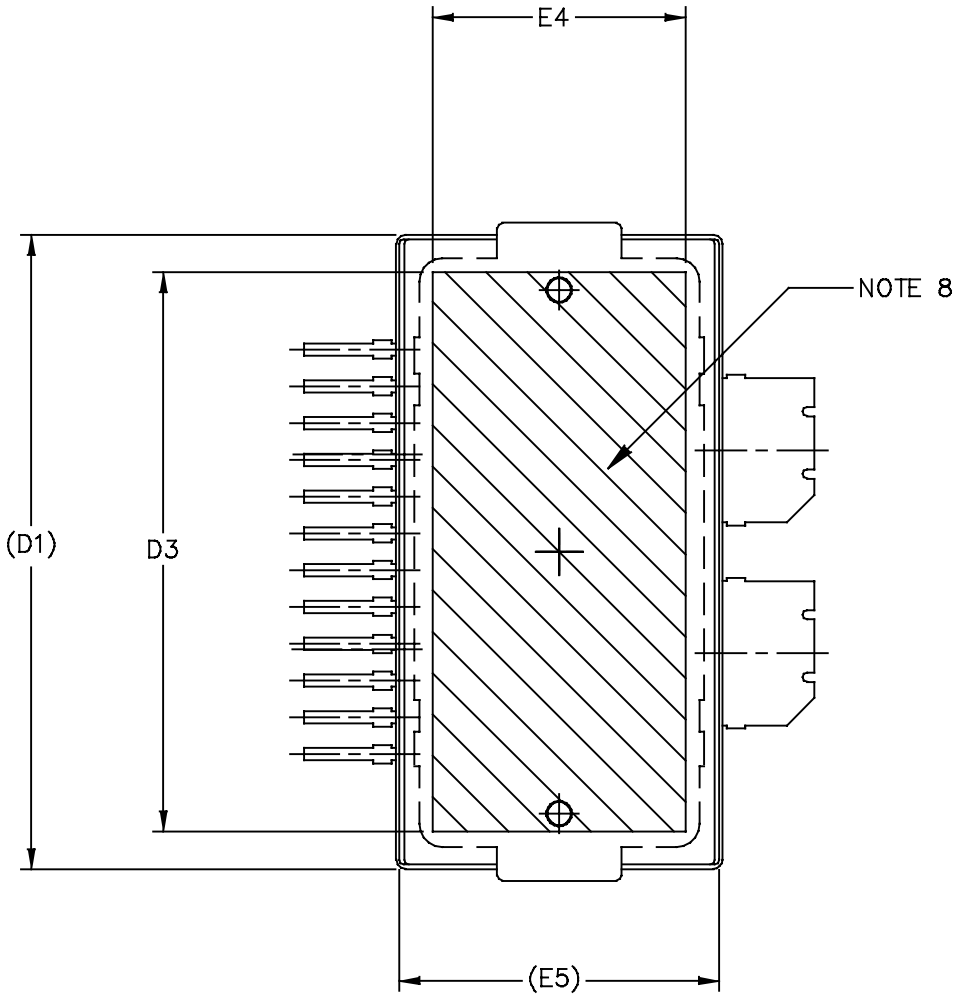
	CASE NUMBER: 1618-02	19 JUN 2007
	STANDARD: NON-JEDEC	



VIEW Y–Y

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TITLE: TO–270 WIDE BODY 14 LEAD	DOCUMENT NO: 98ASA10650D	REV: A
	CASE NUMBER: 1618–02	19 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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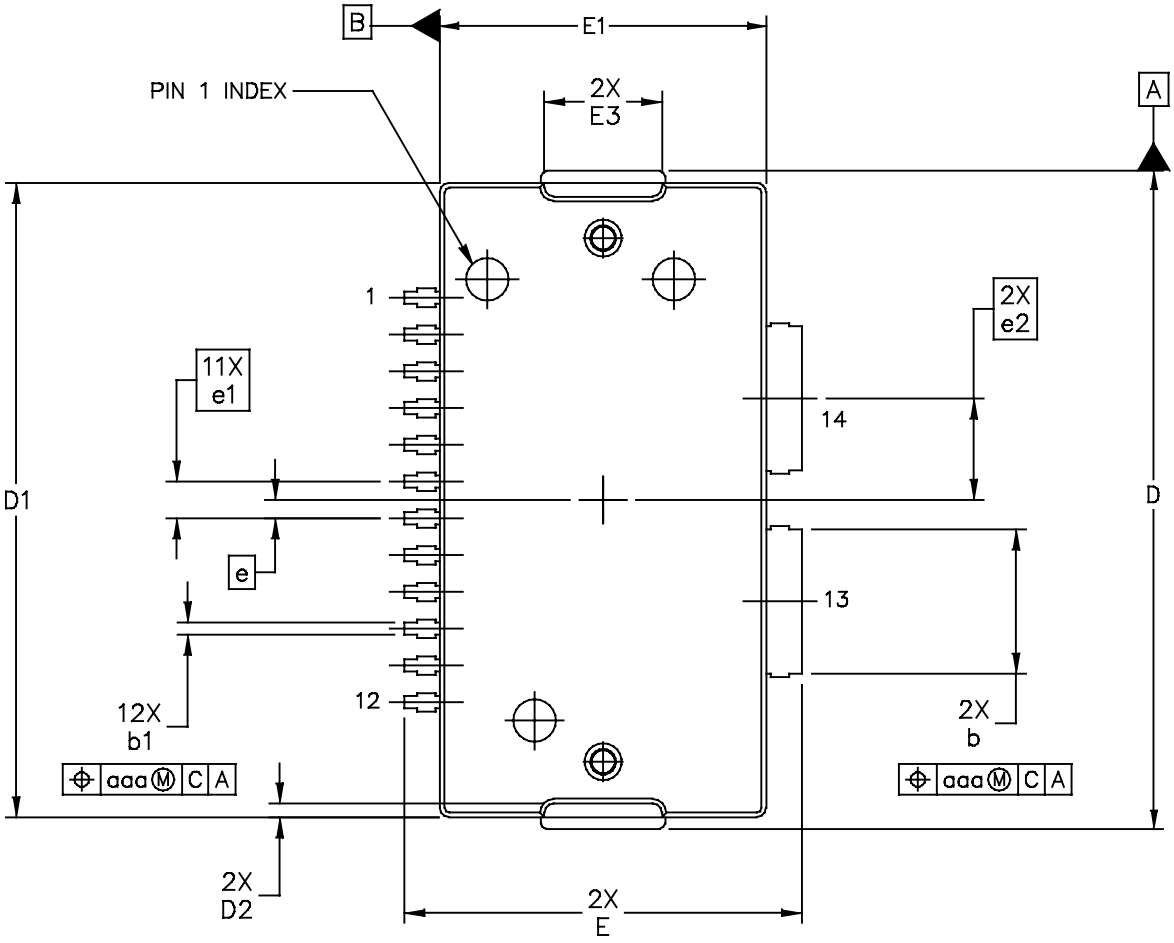
TITLE:	DOCUMENT NO: 98ASA10650D	REV: A
TO–270 WIDE BODY 14 LEAD	CASE NUMBER: 1618–02	19 JUN 2007
	STANDARD: NON–JEDEC	



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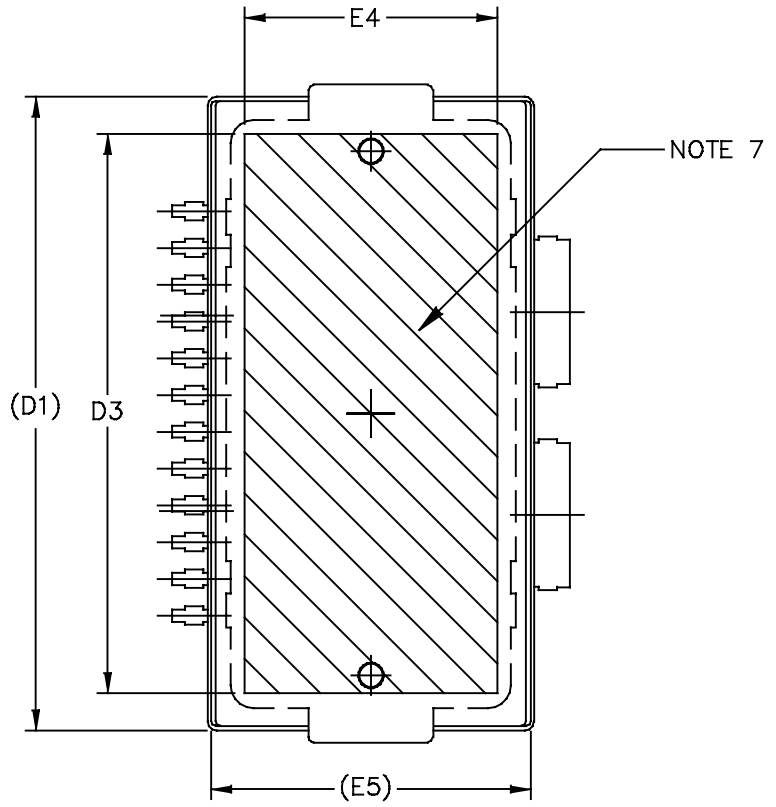
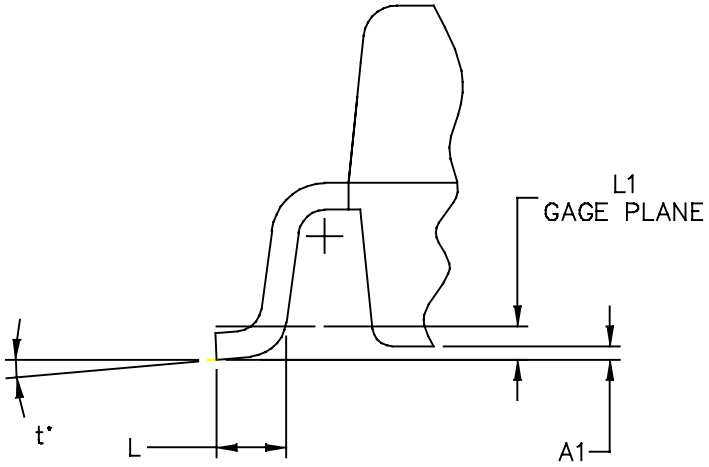
TITLE: TO-270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: A
	CASE NUMBER: 1621-02	19 JUN 2007
	STANDARD: NON-JEDEC	



VIEW Y–Y



DETAIL "Y"

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TITLE: TO–270 WIDE BODY 14 LEAD GULL WING	DOCUMENT NO: 98ASA10653D	REV: A
	CASE NUMBER: 1621–02	19 JUN 2007
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10653D	REV: A
TO–270 WIDE BODY 14 LEAD GULL WING	CASE NUMBER: 1621–02	19 JUN 2007
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2012	• Initial Release of Data Sheet

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