MAX707, MAX708

μP Supervisory Circuits

The MAX707/708 are cost−effective system supervisor circuits designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 20 μsec of V_{CC} falling through the reset voltage threshold. Reset is maintained with 200 mS of delay time after V_{CC} rise above the reset threshold. The MAX707/708 have a low quiescent current of 12 μA at V_{CC} = 3.3 V, an active−high RESET and active−low $\overline{\text{RESET}}$ with a push−pull output. The output is guaranteed valid down to V_{CC} = 1.0 V. The MAX707/708 have a Manual Reset $\overline{\text{MR}}$ input and a +1.25 V threshold detector for power−fail input PFI. These devices are available in a Micro8 and SOIC−8 package.

Features

- Precision Supply−Voltage Monitor
  MAX707: 4.63 V Reset Threshold Voltage
  MAX708: Standard Reset Threshold Voltages (Typical):
  4.38 V, 3.08 V, 2.93 V, 2.63 V
- Reset Threshold Available from 1.6 V to 4.9 V with 100 mV Increments (Factory Option)
- 200 mS (Typ) Reset Timeout Delay
- 12 μA (V_{CC} = 3.3 V) Quiescent Current
- Active_High and Active_Low Reset Output
- Guaranteed RESET_L and RESET Output Valid to V_{CC} = 1.0 V
- Voltage Monitor for Power−Fail or Low−Battery Warning
- 8 Pin SOIC or Micro8 Package
- Pb−Free Packages are Available

Applications

- Computers
- Embedded System
- Battery Powered Equipment
- Critical μP Power Supply Monitor

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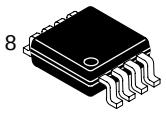
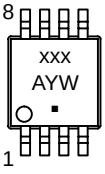
MARKING DIAGRAMS

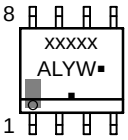


Micro8™
CUA SUFFIX
CASE 846A



xxx = Specific Device Code
A = Assembly Location
Y = Year
W = Week
▪ = Pb−Free Package

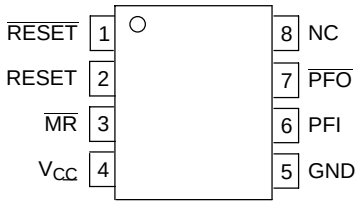
SOIC−8
ESA SUFFIX
CASE 751



xxxxx = Specific Device Code
AL = Assembly Lot Code
Y = Year
W = Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

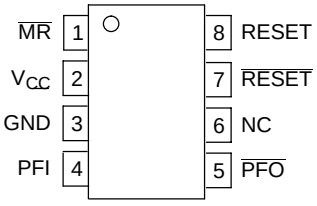
PIN CONFIGURATION

Micro8



(Top View)

SOIC−8



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

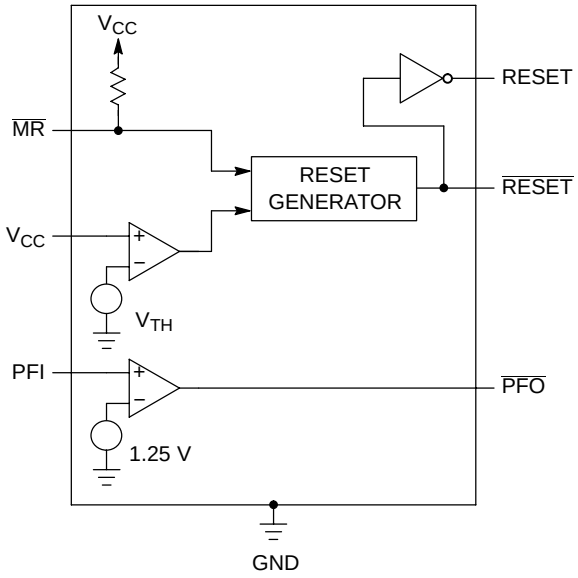


Figure 1. Representative Block Diagram

MAXIMUM RATINGS (Note 1)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	6.0	V
Output Voltage		V_{out}	−0.3 to (V_{CC} + 0.3)	V
Output Current (All Outputs)		I_{out}	20	mA
Input Current (V_{CC} and GND)		I_{in}	20	mA
Thermal Resistance Junction−to−Air		$R_{\theta JA}$		°C/W
	Micro8		248	
	SOIC−8		187	
Operating Ambient Temperature		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−40 to +125	°C
LatchUp Performance		$I_{LATCHUP}$		mA
	Positive		300	
	Negative		280	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

ELECTRICAL CHARACTERISTICS (V_{CC} = 1.0 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{CC} = 3.3 V.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}	1.0	−	5.5	V
Supply Current V_{CC} = 3.3 V V_{CC} = 5.5 V	I_{CC}	 − −	 12 16	 22 28	μA
Reset Threshold MAX707 T_A = +25°C T_A = −40°C to +85°C MAX708 T_A = +25°C T_A = −40°C to +85°C MAX708T T_A = +25°C T_A = −40°C to +85°C MAX708S T_A = +25°C T_A = −40°C to +85°C MAX708R T_A = +25°C T_A = −40°C to +85°C	V_{TH}	 4.56 4.50 4.31 4.25 3.03 3.00 2.89 2.85 2.59 2.55	 4.63 4.38 3.08 2.93 2.63 	 4.70 4.75 4.45 4.50 3.13 3.15 2.97 3.00 2.67 2.70	V
Reset Threshold Hysteresis	V_{HYS}	−	0.01 V_{TH}	−	mV
V_{CC} Falling Reset Delay (V_{CC} = V_{TH} + 0.2 V to V_{TH} − 0.2 V)	t_{PD}	−	20	−	μS
Reset Active Timeout Period	t_{RP}	140	200	330	mS
RESET_L, RESET_H Output Low Voltage V_{CC} ≥ 1.0 V, I_{ol} = 100 μA V_{CC} > 2.7 V, I_{ol} = 1.2 mA V_{CC} > 4.5 V, I_{ol} = 3.2 mA	V_{ol}	 − − −	 − − −	 0.3 0.3 0.3	V
RESET_L, RESET_H Output High Voltage V_{CC} ≥ 1.0 V, I_{oh} = 50 μA V_{CC} > 2.7 V, I_{oh} = 500 μA V_{CC} > 4.5 V, I_{oh} = 800 μA	V_{oh}	 0.8 V_{CC} 0.8 V_{CC} 0.8 V_{CC}	 − − −	 − − −	V
MR_L Pull−up Resistance	R_{MRI}	50	−	−	KΩ
MR_L Pulse Width (V_{TH} (max) < V_{CC} < 5.5 V)	t_{MR}	1.0	−	−	μS
MR_L Glitch Rejection (V_{TH} (max) < V_{CC} < 5.5 V)	−	−	0.1	−	μS
MR_L High_level Input Threshold (V_{TH} (max) < V_{CC} < 5.5 V)	V_{IH}	0.7 V_{CC}	−	−	V
MR_L Low_level Input Threshold (V_{TH} (max) < V_{CC} < 5.5 V)	V_{IL}	−	−	0.3 V_{CC}	V
MR_L to RESET_L and RESET_H Output Delay (V_{TH} (max) < V_{CC} < 5.5 V)	t_{MD}	−	0.2	−	μS
PFI Input Threshold (V_{CC} = 3.3 V, PFI Falling)	−	1.20	1.25	1.3	V
PFI Input Current	−	−250	0.01	250	nA
PFI to PFO Delay (V_{CC} = 3.3 V, $V_{OVERDRIVE}$ = 15 mV)	−	−	3.0	−	μS
PFO_L Output Low Voltage V_{CC} = 2.7 V, I_{ol} = 1.2 mA V_{CC} = 4.5 V, I_{ol} = 3.2 mA	V_{ol}	 − −	 − −	 0.3 0.3	V
PFO_L Output High Voltage V_{CC} = 2.7 V, I_{oh} = 500 μA V_{CC} = 4.5 V, I_{oh} = 800 μA	V_{oh}	 0.8 V_{CC} 0.8 V_{CC}	 − −	 − −	V

PIN DESCRIPTION (Pin No. with parentheses is for Micro8 package.)

Pin No.	Symbol	Description
1 (3)	$\overline{MR}$	Manual Reset Input. $\overline{MR}$ can be driven from TTL/CMOS logic or from a manual Reset switch. This input, when floating, is internally pulled up to V_{CC} with 50 kΩ resistor.
2 (4)	V_{CC}	Supply Voltage: C = 100 nF is recommended as a bypass capacitor between V_{CC} and GND.
3 (5)	GND	Ground Reference
4 (6)	PFI	Power Fail Voltage Monitor Input. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5 (7)	$\overline{PFO}$	Power Fail Monitor Output. When PFI is less than 1.25 V, it goes low and sinks current. Otherwise, it remains high.
6 (8)	NC	Non−connective Pin
7 (1)	$\overline{RESET}$	Active Low $\overline{RESET}$ can be triggered by V_{CC} below the threshold level or by a low signal on $\overline{MR}$. It remains low for 200 ms (typ.) after V_{CC} rises above the reset threshold.
8 (2)	RESET	Active high RESET output the inverse of $\overline{RESET}$ one.

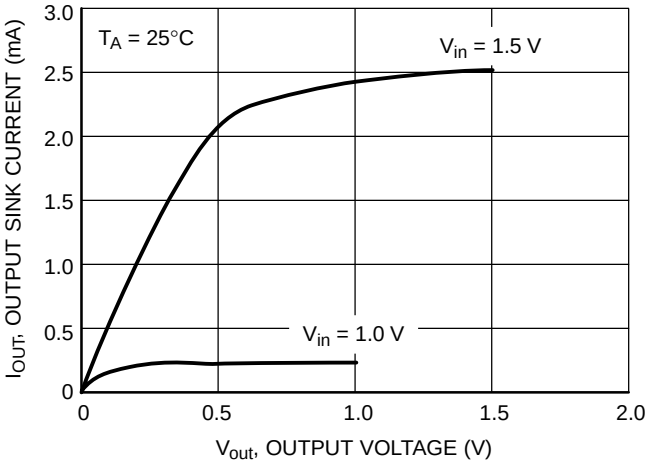


Figure 2. MAX707/708 Series 1.60 V Reset Output Sink Current vs. Output Voltage

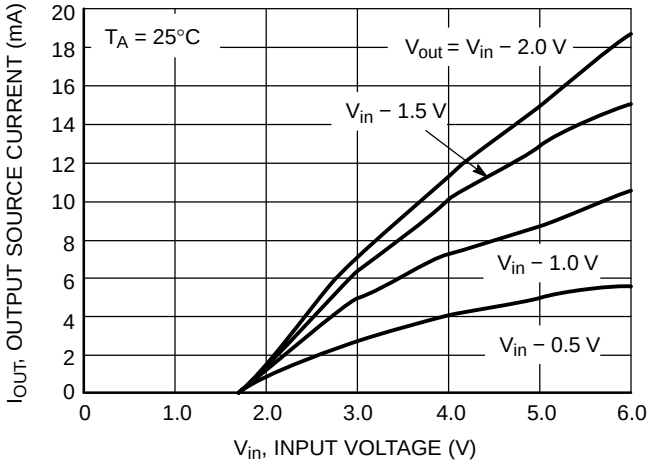


Figure 3. MAX707/708 Series 1.60 V Reset Output Source Current vs. Input Voltage

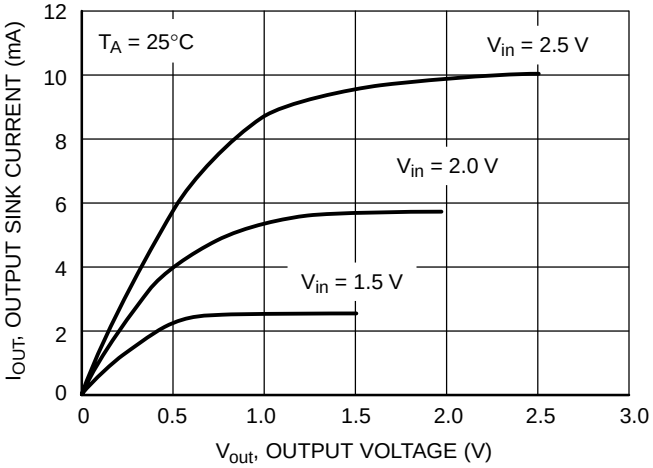


Figure 4. MAX707/708 Series 2.93 V Reset Output Sink Current vs. Output Voltage

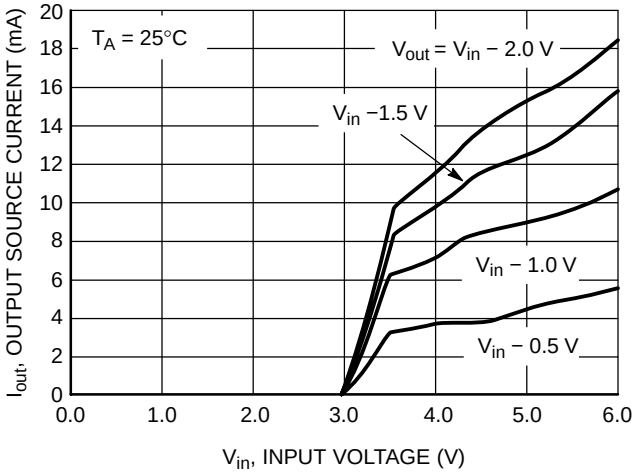


Figure 5. MAX707/708 Series 2.93 V Reset Output Source Current vs. Input Voltage

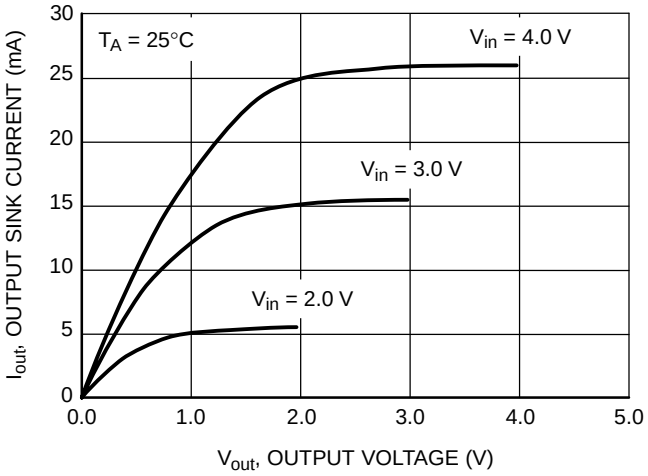


Figure 6. MAX707/708 Series 4.90 V Reset Output Sink Current vs. Output Voltage

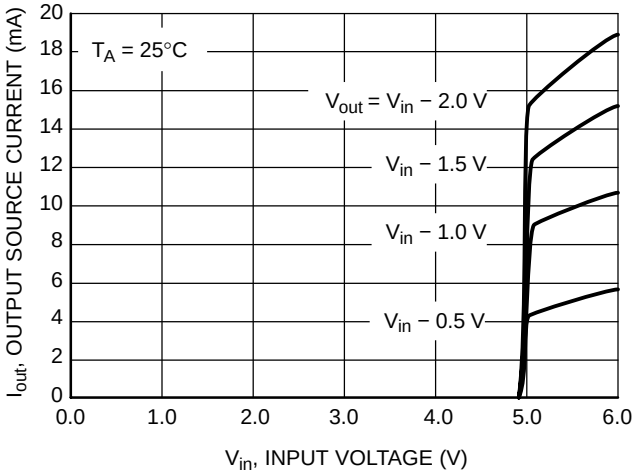


Figure 7. MAX707/708 Series 4.90 V Reset Output Source Current vs. Input Voltage

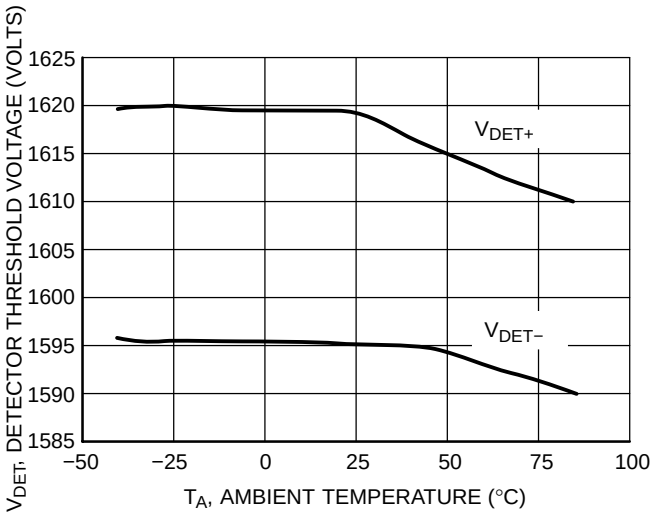


Figure 8. MAX707/708 Series 1.60 V Detector Threshold Voltage vs. Temperature

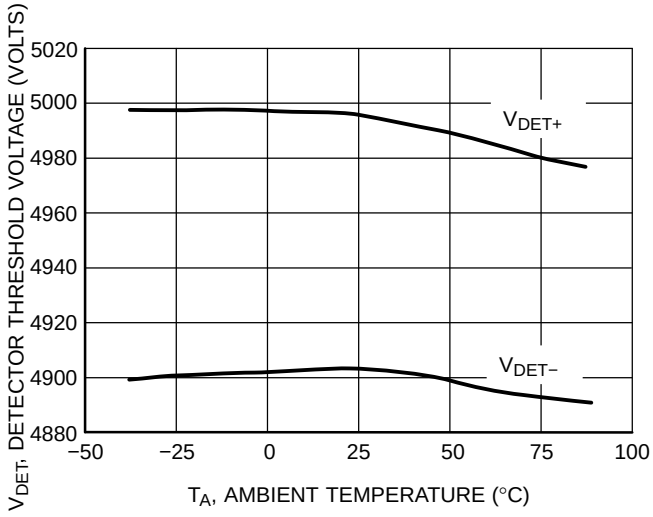


Figure 9. MAX707/708 Series 4.90 V Detector Threshold Voltage vs. Temperature

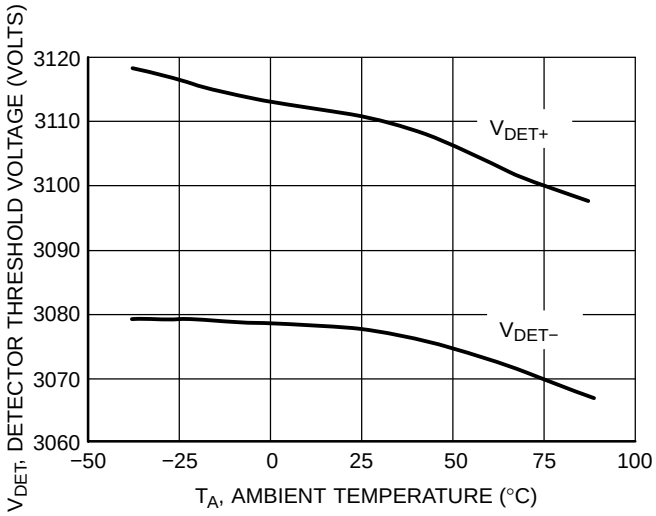


Figure 10. MAX707/708 Series 2.93 V Detector Threshold Voltage vs. Temperature

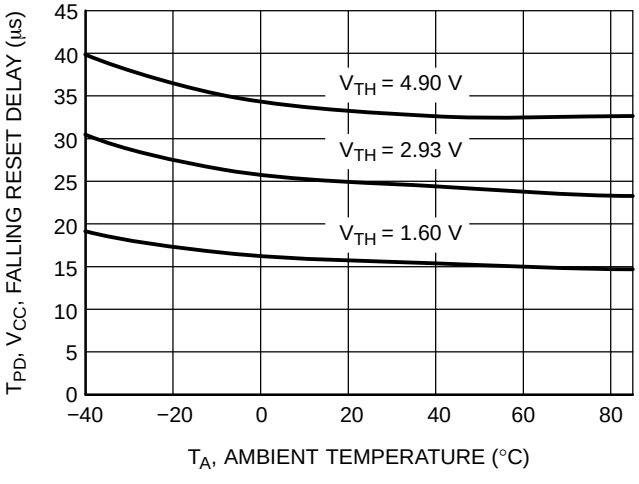


Figure 11. MAX707/708 Series V_{CC} Falling Reset Delay vs. Temperature

APPLICATIONS INFORMATION

Microprocessor Reset

To generate a processor reset, the manual Reset input allows different reset sources. A pushbutton switch can be one of these. It is effectively debounced by the 1.0 μs minimum reset pulse width. As $\overline{MR}$ is TTL/CMOS logic compatible, it can be driven by an external logic line.

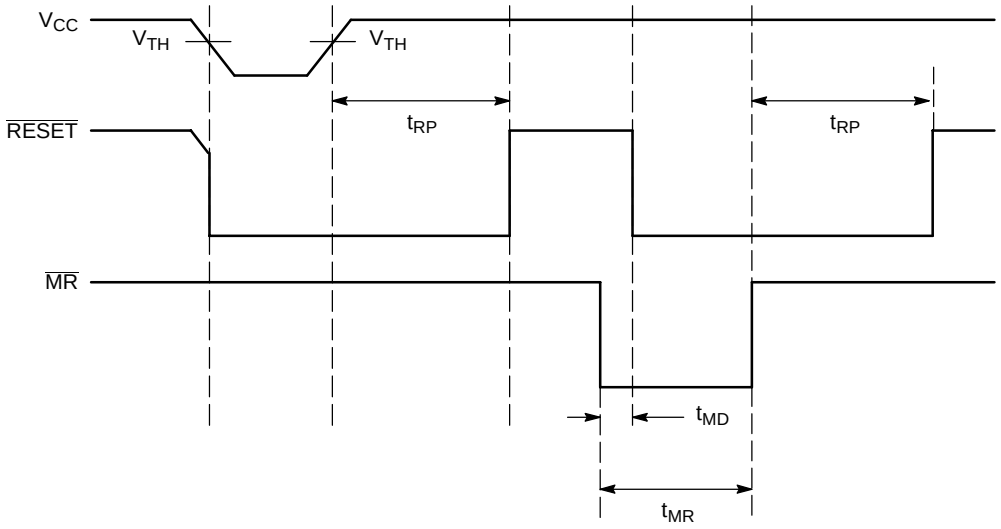


Figure 12. $\overline{RESET}$ and $\overline{MR}$ Timing

V_{CC} Transient Rejection

The MAX707/708 provides accurate V_{CC} monitoring and reset timing during power−up, power−down, and brownout/sag conditions, and rejects negative glitches on the power supply line. Figure 13 shows the maximum transient duration vs. maximum negative excursion (overdrive) for glitch rejection. For a given overdrive, the point of the curve is the maximum width of the glitch allowed before the device generates a reset signal. Transient immunity can be improved by adding a capacitor (100 nF for example) in close proximity to the V_{CC} pin of the MAX707/708.

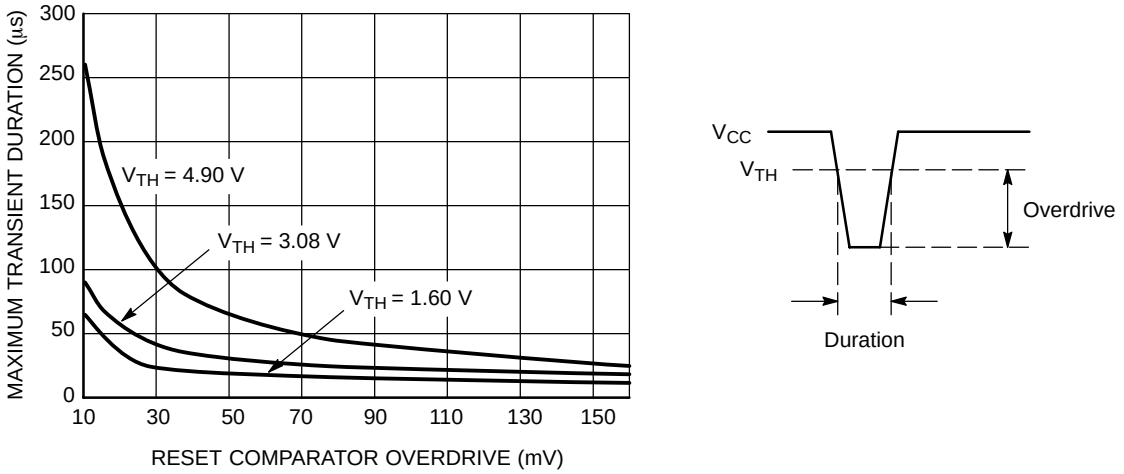


Figure 13. Maximum Transient Duration vs. Overdrive for Glitch Rejection at 25°C

$\overline{\text{RESET}}$ Signal Integrity During Power−Down

The MAX707/708 $\overline{\text{RESET}}$ output is valid until V_{CC} falls below 1.0 V. Then, the output becomes an open circuit and no longer sinks current. This means CMOS logic inputs of the μP will be floating at an undetermined voltage. Most digital systems are completely shutdown well above this voltage. However, in the case $\overline{\text{RESET}}$ must be maintained valid to V_{CC} = 0 V, a pull down resistor must be connected from $\overline{\text{RESET}}$ to ground to discharge stray capacitances and hold the output low (Figure 14). This resistor value, though not critical, should be chosen large enough not to load $\overline{\text{RESET}}$ and small enough to pull it to ground. R = 100 kΩ will be suitable for most applications.

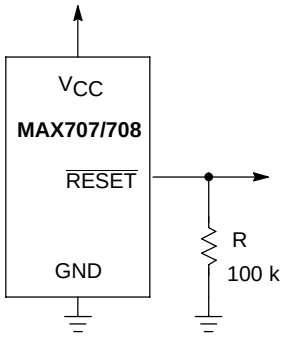


Figure 14. Ensuring $\overline{\text{RESET}}$ Valid to V_{CC} = 0 V

Interfacing with μPs with Bidirectional I/O Pins

Some μPs have bidirectional reset pins. If, for example, the $\overline{\text{RESET}}$ output is driven high and the μP wants to put it low, indeterminate logic level may result. This can be avoided by adding a 4.7 kΩ resistor in series with the output of the MAX707/708 (Figure 15). If there are other components in the system that require a reset signal, they should be buffered so as not to load the reset line. If the other components are required to follow the reset I/O of the μP, the buffer should be connected as shown with the solid line.

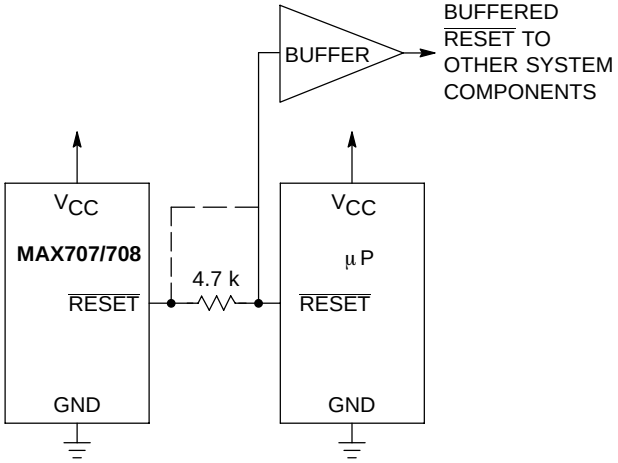
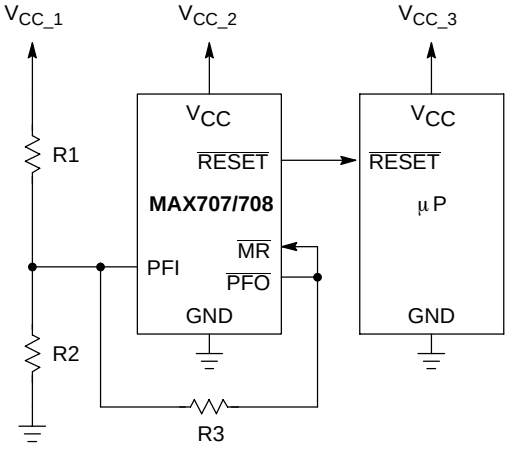
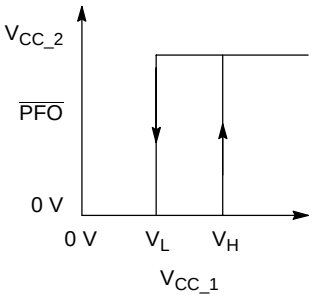


Figure 15. Interfacing to Bidirectional Reset I/O

Monitoring Additional Supply Levels

When connecting a voltage divider to PFI and adjusting it properly, you can monitor a voltage different than the unregulated DC one. As shown in Figure 16, to increase noise immunity, hysteresis may be added to the power−fail comparator just by a resistor between $\overline{\text{PFO}}$ and PFI. Not to unbalance the potential divider network, R3 should be 10 times the sum of the two resistors R1 and R2. If required, a capacitor between PFI and GND will reduce the sensitivity of the circuit to high−frequency noise on the line being monitored. The $\overline{\text{PFO}}$ output may be connected to $\overline{\text{MR}}$ input to generate a low level on the $\overline{\text{RESET}}$ when V_{CC_1} drops out of tolerance. Thus a $\overline{\text{RESET}}$ is generated when one of the two voltages is below its threshold level.





$$V_L = 1.25 + R1 \times \left(\frac{1.25}{R2} + \frac{1.25 - V_{cc\_2}}{R3}\right)$$

$$V_H = 1.25 \times (1 + R1 \times \left(\frac{R2 + R3}{R2 \times R3}\right))$$

$$V_{HYS} = V_H - V_L = \frac{R1 \times V_{cc\_2}}{R3}$$

Figure 16. Monitoring Additional Supply Levels

ORDERING INFORMATION

Device	Marking	Reset V_{CC} Threshold (V)	Package	Shipping†
MAX707ESA−T	S707	4.63	SOIC−8	2500 Tape & Reel
MAX707ESA−TG	S707	4.63	SOIC−8 (Pb−Free)	2500 Tape & Reel
MAX708ESA−T	S708	4.38	SOIC−8	2500 Tape & Reel
MAX708ESA−TG	S708	4.38	SOIC−8 (Pb−Free)	2500 Tape & Reel
MAX708RESA−T	S708R	2.63	SOIC−8	2500 Tape & Reel
MAX708RESA−TG	S708R	2.63	SOIC−8 (Pb−Free)	2500 Tape & Reel
MAX708SESA−T	S708S	2.93	SOIC−8	2500 Tape & Reel
MAX708SESA−TG	S708S	2.93	SOIC−8 (Pb−Free)	2500 Tape & Reel
MAX708TESA−T	S708T	3.08	SOIC−8	2500 Tape & Reel
MAX708TESA−TG	S708T	3.08	SOIC−8 (Pb−Free)	2500 Tape & Reel
MAX707CUA−T	SAC	4.63	Micro8	4000 Tape & Reel
MAX707CUA−TG	SAC	4.63	Micro8 (Pb−Free)	4000 Tape & Reel
MAX708CUA−T	SAD	4.38	Micro8	4000 Tape & Reel
MAX708CUA−TG	SAD	4.38	Micro8 (Pb−Free)	4000 Tape & Reel
MAX708RCUA−T	SAG	2.63	Micro8	4000 Tape & Reel
MAX708RCUA−TG	SAG	2.63	Micro8 (Pb−Free)	4000 Tape & Reel
MAX708SCUA−T	SAF	2.93	Micro8	4000 Tape & Reel
MAX708SCUA−TG	SAF	2.93	Micro8 (Pb−Free)	4000 Tape & Reel
MAX708TCUA−T	SAE	3.08	Micro8	4000 Tape & Reel
MAX708TCUA−TG	SAE	3.08	Micro8 (Pb−Free)	4000 Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

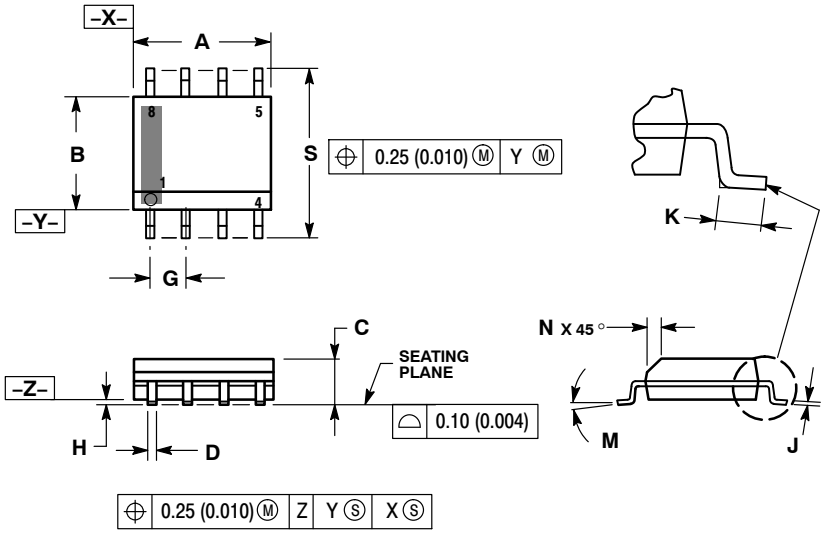
Micro8 is a trademark of International Rectifier.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

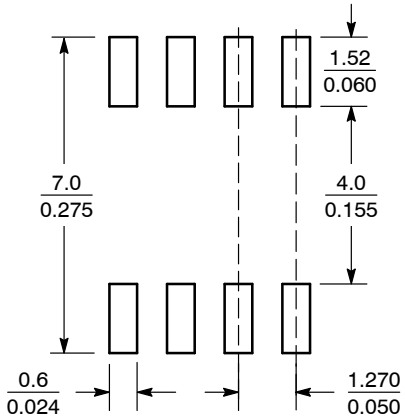
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

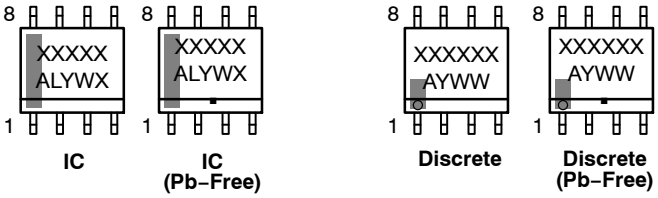
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

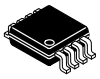
STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

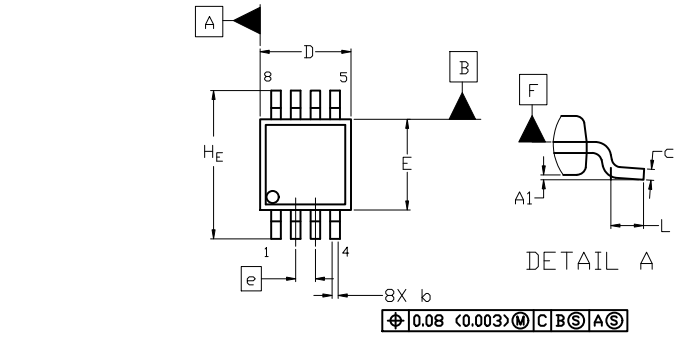
ON Semiconductor®

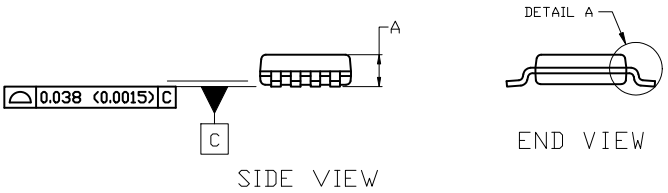


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

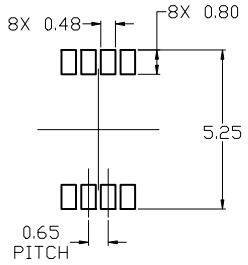
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

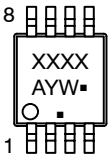


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

DOCUMENT NUMBER:	**98ASB14087C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**MICRO8**	**PAGE 1 OF 1**

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