

# NTMD6P02, NVMD6P02

## MOSFET – Power, Dual, P-Channel, SOIC-8 6 A, 20 V

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SOIC-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- These Devices are Pb-Free and are RoHS Compliant
- NVMD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

### Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-20	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 12$	V
Thermal Resistance – Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $T_A = 70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 4)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	62.5 2.0 -7.8 -5.7 0.5 -3.89 -40	$^\circ\text{C}/\text{W}$ W A A W A A
Thermal Resistance – Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $T_A = 70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 4)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	98 1.28 -6.2 -4.6 0.3 -3.01 -35	$^\circ\text{C}/\text{W}$ W A A W A A
Thermal Resistance – Junction-to-Ambient (Note 3) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $T_A = 70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 4)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	166 0.75 -4.8 -3.5 0.2 -2.48 -30	$^\circ\text{C}/\text{W}$ W A A W A A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -20$ Vdc, $V_{GS} = -5.0$ Vdc, Peak $I_L = -5.0$ Apk, $L = 40$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	500	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

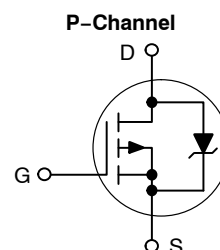
1. Mounted onto a 2" square FR-4 Board (1 in sq, 2 oz. Cu 0.06" thick single sided),  $t = 10$  seconds.



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

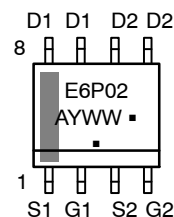
6 AMPERES, 20 VOLTS



### MARKING DIAGRAM & PIN ASSIGNMENT



SOIC-8  
CASE 751  
STYLE 11



E6P02 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMD6P02R2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NVMD6P02R2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

## NTMD6P02, NVMD6P02

2. Mounted onto a 2" square FR-4 Board (1 in sq, 2 oz. Cu 0.06" thick single sided), t = steady state.
3. Minimum FR-4 or G-10 PCB, t = steady state.
4. Pulse Test: Pulse Width = 300  $\mu$ s, Duty Cycle = 2%.

# NTMD6P02, NVMD6P02

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)\*

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	-20 -	- -11.6	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C) (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 70°C)	I <sub>DSS</sub>	- -	- -	-1.0 -5.0	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = -12 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-100	nAdc
Gate-Body Leakage Current (V <sub>GS</sub> = +12 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	-0.6 -	-0.88 2.6	-1.20 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -6.2 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -5.0 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -3.1 Adc)	R <sub>DS(on)</sub>	- - -	0.027 0.038 0.038	0.033 0.050 -	Ω
Forward Transconductance (V <sub>DS</sub> = -10 Vdc, I <sub>D</sub> = -6.2 Adc)	g <sub>FS</sub>	-	15	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ISS</sub>	-	1380	1700	pF
Output Capacitance		C <sub>OSS</sub>	-	515	775	
Reverse Transfer Capacitance		C <sub>RSS</sub>	-	250	450	

### SWITCHING CHARACTERISTICS (Notes 5 and 6)

Turn-On Delay Time	(V <sub>DD</sub> = -10 Vdc, I <sub>D</sub> = -1.0 Adc, V <sub>GS</sub> = -10 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	15	25	ns
Rise Time		t <sub>r</sub>	-	20	50	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	85	125	
Fall Time		t <sub>f</sub>	-	50	110	
Turn-On Delay Time	(V <sub>DD</sub> = -16 Vdc, I <sub>D</sub> = -6.2 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	17	-	ns
Rise Time		t <sub>r</sub>	-	65	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	50	-	
Fall Time		t <sub>f</sub>	-	80	-	
Total Gate Charge	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -6.2 Adc)	Q <sub>tot</sub>	-	20	35	nC
Gate-Source Charge		Q <sub>gs</sub>	-	4.0	-	
Gate-Drain Charge		Q <sub>gd</sub>	-	8.0	-	

### BODY-DRAIN DIODE RATINGS (Note 5)

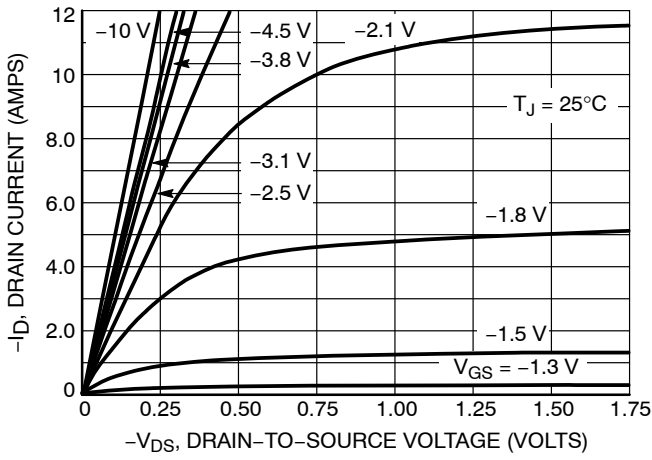
Diode Forward On-Voltage	(I <sub>S</sub> = -1.7 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = -1.7 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	-0.80 -0.65	-1.2 -	Vdc
Diode Forward On-Voltage	(I <sub>S</sub> = -6.2 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = -6.2 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	-0.95 -0.80	- -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = -1.7 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	50	80	ns
		t <sub>a</sub>	-	20	-	
		t <sub>r</sub>	-	30	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.04	-	μC

5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

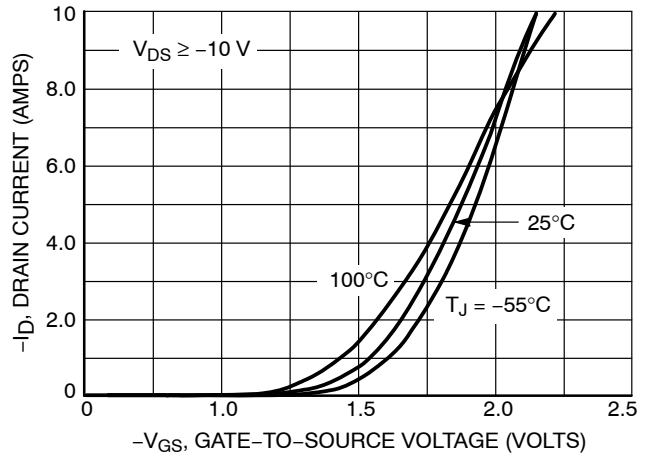
6. Switching characteristics are independent of operating junction temperature.

\*Handling precautions to protect against electrostatic discharge are mandatory.

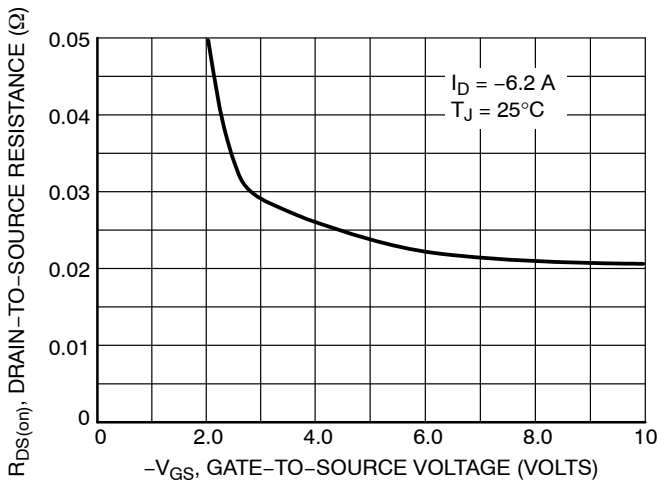
# NTMD6P02, NVMD6P02



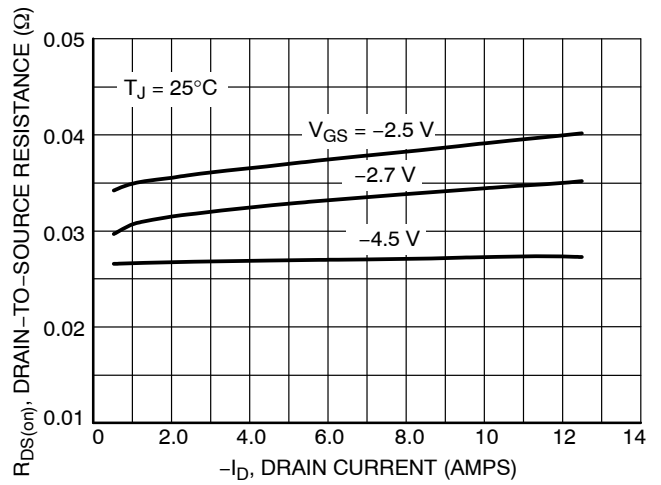
**Figure 1. On-Region Characteristics**



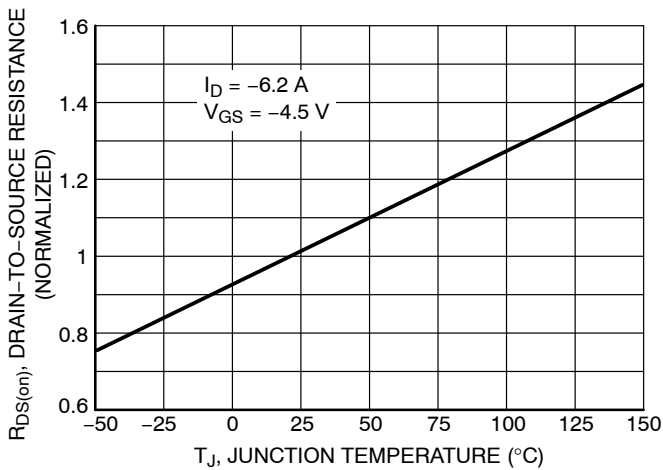
**Figure 2. Transfer Characteristics**



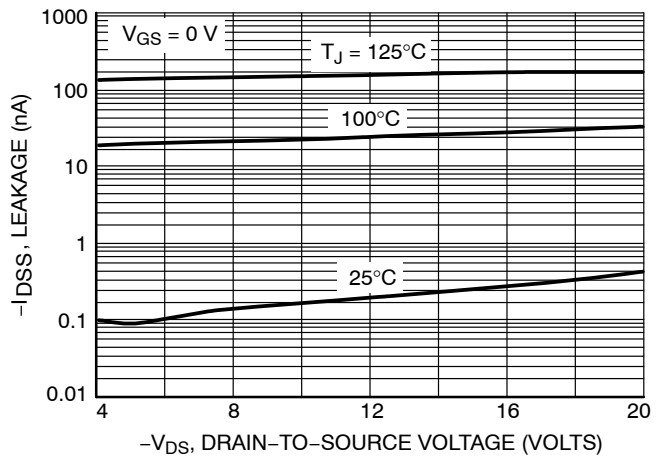
**Figure 3. On-Resistance versus Gate-To-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

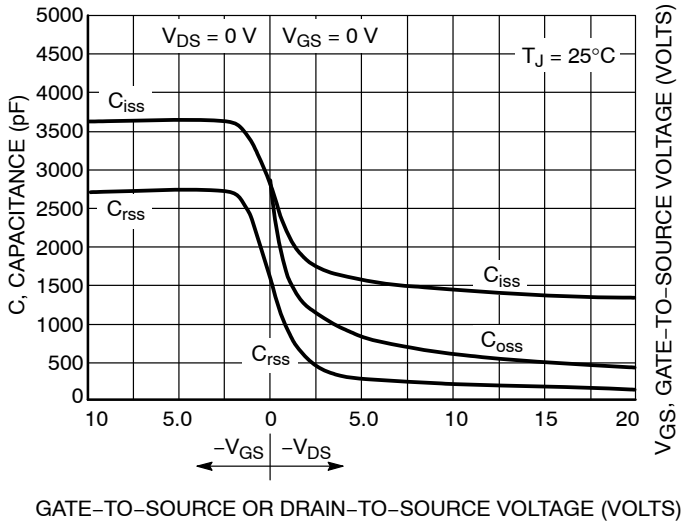


**Figure 5. On-Resistance Variation with Temperature**

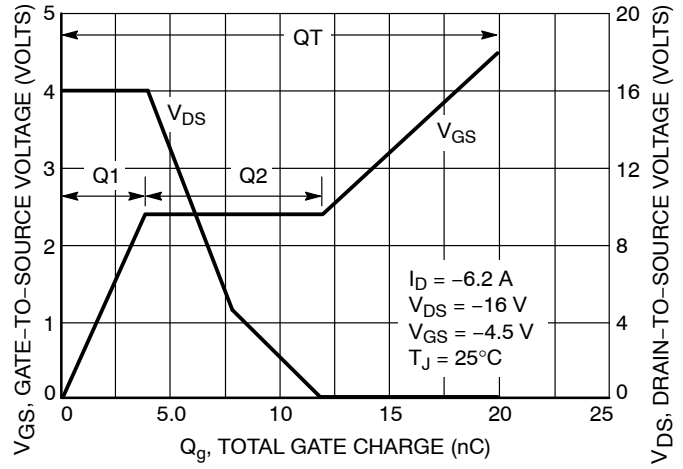


**Figure 6. Drain-To-Source Leakage Current versus Voltage**

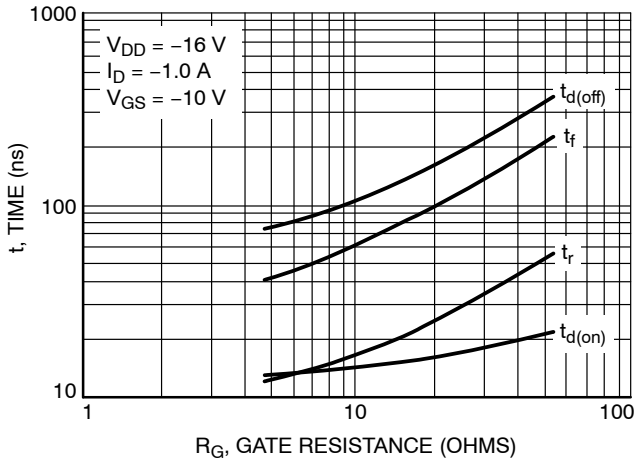
# NTMD6P02, NVMD6P02



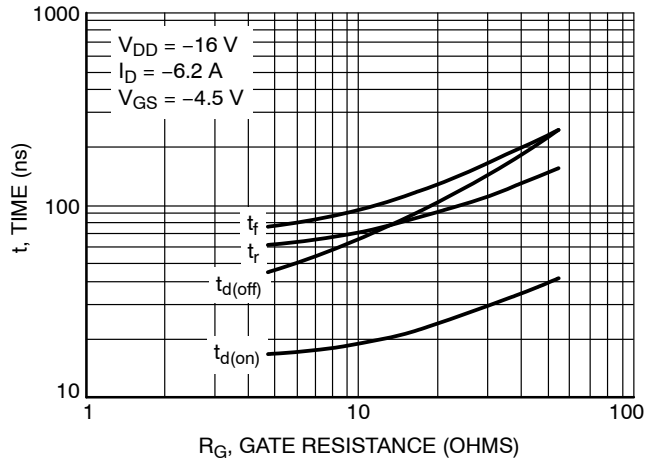
**Figure 7. Capacitance Variation**



**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**

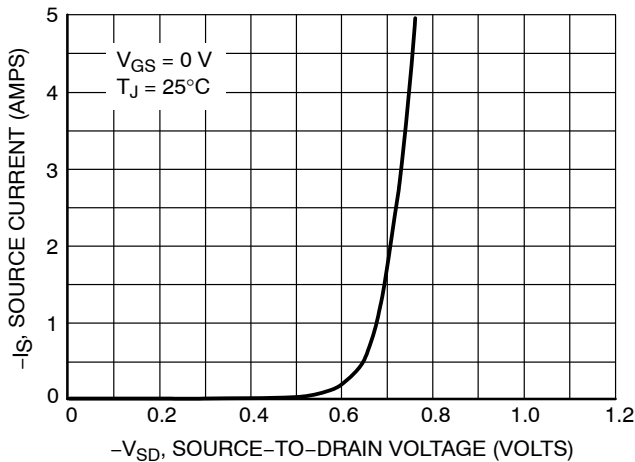


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

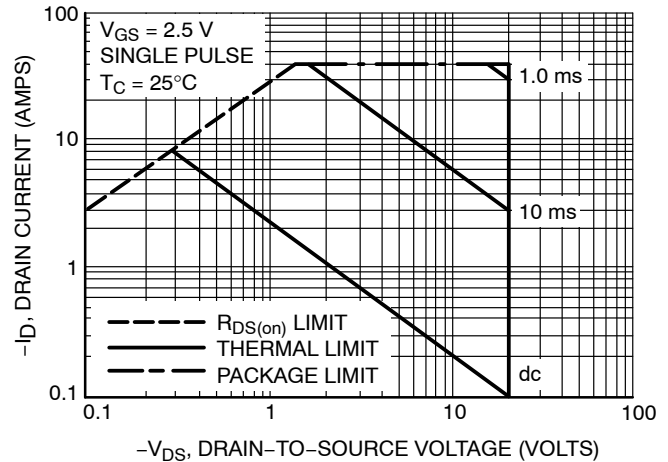


**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS



**Figure 11. Diode Forward Voltage versus Current**



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

# NTMD6P02, NVMD6P02

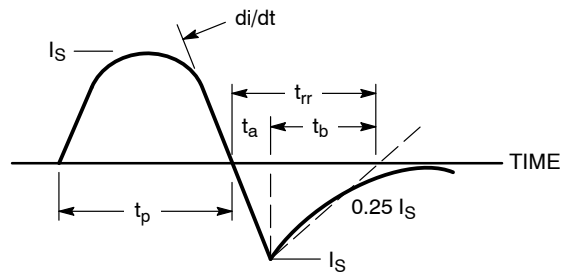


Figure 13. Diode Reverse Recovery Waveform

## TYPICAL ELECTRICAL CHARACTERISTICS

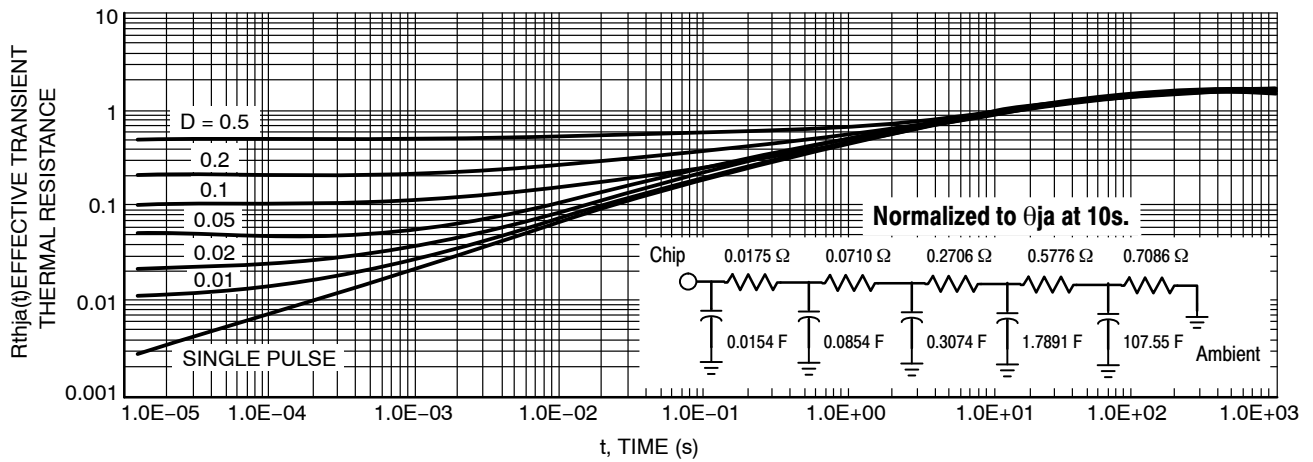


Figure 14. Thermal Response

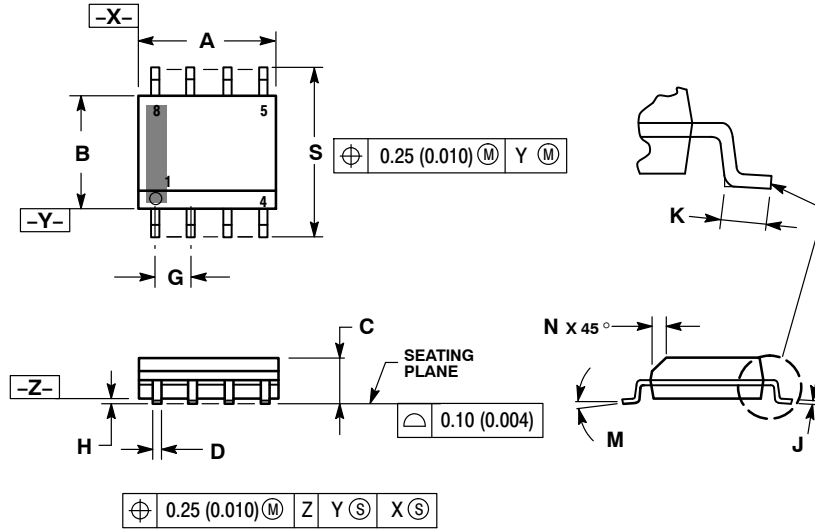
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

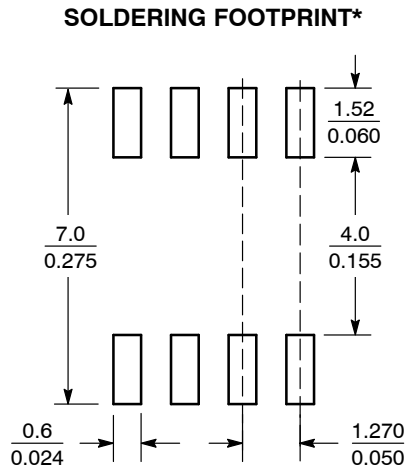
DATE 16 FEB 2011



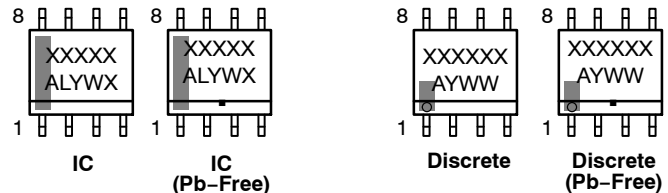
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

- |   |  |  |  |
|---|--|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. COLLECTOR<br/>         4. EMITTER<br/>         5. EMITTER<br/>         6. BASE<br/>         7. BASE<br/>         8. EMITTER</p>   | <p>STYLE 2:<br/>         PIN 1. COLLECTOR, DIE, #1<br/>         2. COLLECTOR, #1<br/>         3. COLLECTOR, #2<br/>         4. COLLECTOR, #2<br/>         5. BASE, #2<br/>         6. EMITTER, #2<br/>         7. BASE, #1<br/>         8. EMITTER, #1</p>               | <p>STYLE 3:<br/>         PIN 1. DRAIN, DIE #1<br/>         2. DRAIN, #1<br/>         3. DRAIN, #2<br/>         4. DRAIN, #2<br/>         5. GATE, #2<br/>         6. SOURCE, #2<br/>         7. GATE, #1<br/>         8. SOURCE, #1</p>                            | <p>STYLE 4:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. ANODE<br/>         4. ANODE<br/>         5. ANODE<br/>         6. ANODE<br/>         7. ANODE<br/>         8. COMMON CATHODE</p>   |
| <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. DRAIN<br/>         5. GATE<br/>         6. GATE<br/>         7. SOURCE<br/>         8. SOURCE</p>   | <p>STYLE 6:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. DRAIN<br/>         4. SOURCE<br/>         5. SOURCE<br/>         6. GATE<br/>         7. GATE<br/>         8. SOURCE</p>  | <p>STYLE 7:<br/>         PIN 1. INPUT<br/>         2. EXTERNAL BYPASS<br/>         3. THIRD STAGE SOURCE<br/>         4. GROUND<br/>         5. DRAIN<br/>         6. GATE 3<br/>         7. SECOND STAGE Vd<br/>         8. FIRST STAGE Vd</p>                    | <p>STYLE 8:<br/>         PIN 1. COLLECTOR, DIE #1<br/>         2. BASE, #1<br/>         3. BASE, #2<br/>         4. COLLECTOR, #2<br/>         5. COLLECTOR, #2<br/>         6. EMITTER, #2<br/>         7. EMITTER, #1<br/>         8. COLLECTOR, #1</p>                              |
| <p>STYLE 9:<br/>         PIN 1. EMITTER, COMMON<br/>         2. COLLECTOR, DIE #1<br/>         3. COLLECTOR, DIE #2<br/>         4. EMITTER, COMMON<br/>         5. EMITTER, COMMON<br/>         6. BASE, DIE #2<br/>         7. BASE, DIE #1<br/>         8. EMITTER, COMMON</p> | <p>STYLE 10:<br/>         PIN 1. GROUND<br/>         2. BIAS 1<br/>         3. OUTPUT<br/>         4. GROUND<br/>         5. GROUND<br/>         6. BIAS 2<br/>         7. INPUT<br/>         8. GROUND</p>  | <p>STYLE 11:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. DRAIN 2<br/>         7. DRAIN 1<br/>         8. DRAIN 1</p>   | <p>STYLE 12:<br/>         PIN 1. SOURCE<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 13:<br/>         PIN 1. N.C.<br/>         2. SOURCE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>  | <p>STYLE 14:<br/>         PIN 1. N-SOURCE<br/>         2. N-GATE<br/>         3. P-SOURCE<br/>         4. P-GATE<br/>         5. P-DRAIN<br/>         6. P-DRAIN<br/>         7. N-DRAIN<br/>         8. N-DRAIN</p>   | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. ANODE 1<br/>         3. ANODE 1<br/>         4. ANODE 1<br/>         5. CATHODE, COMMON<br/>         6. CATHODE, COMMON<br/>         7. CATHODE, COMMON<br/>         8. CATHODE, COMMON</p>               | <p>STYLE 16:<br/>         PIN 1. EMITTER, DIE #1<br/>         2. BASE, DIE #1<br/>         3. EMITTER, DIE #2<br/>         4. BASE, DIE #2<br/>         5. COLLECTOR, DIE #2<br/>         6. COLLECTOR, DIE #2<br/>         7. COLLECTOR, DIE #1<br/>         8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:<br/>         PIN 1. VCC<br/>         2. V2OUT<br/>         3. V1OUT<br/>         4. TXE<br/>         5. RXE<br/>         6. VEE<br/>         7. GND<br/>         8. ACC</p>  | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. SOURCE<br/>         4. GATE<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. CATHODE<br/>         8. CATHODE</p>   | <p>STYLE 19:<br/>         PIN 1. SOURCE 1<br/>         2. GATE 1<br/>         3. SOURCE 2<br/>         4. GATE 2<br/>         5. DRAIN 2<br/>         6. MIRROR 2<br/>         7. DRAIN 1<br/>         8. MIRROR 1</p>   | <p>STYLE 20:<br/>         PIN 1. SOURCE (N)<br/>         2. GATE (N)<br/>         3. SOURCE (P)<br/>         4. GATE (P)<br/>         5. DRAIN<br/>         6. DRAIN<br/>         7. DRAIN<br/>         8. DRAIN</p>   |
| <p>STYLE 21:<br/>         PIN 1. CATHODE 1<br/>         2. CATHODE 2<br/>         3. CATHODE 3<br/>         4. CATHODE 4<br/>         5. CATHODE 5<br/>         6. COMMON ANODE<br/>         7. COMMON ANODE<br/>         8. CATHODE 6</p>  | <p>STYLE 22:<br/>         PIN 1. I/O LINE 1<br/>         2. COMMON CATHODE/VCC<br/>         3. COMMON CATHODE/VCC<br/>         4. I/O LINE 3<br/>         5. COMMON ANODE/GND<br/>         6. I/O LINE 4<br/>         7. I/O LINE 5<br/>         8. COMMON ANODE/GND</p> | <p>STYLE 23:<br/>         PIN 1. LINE 1 IN<br/>         2. COMMON ANODE/GND<br/>         3. COMMON ANODE/GND<br/>         4. LINE 2 IN<br/>         5. LINE 2 OUT<br/>         6. COMMON ANODE/GND<br/>         7. COMMON ANODE/GND<br/>         8. LINE 1 OUT</p> | <p>STYLE 24:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR/ANODE<br/>         4. COLLECTOR/ANODE<br/>         5. CATHODE<br/>         6. CATHODE<br/>         7. COLLECTOR/ANODE<br/>         8. COLLECTOR/ANODE</p>                                      |
| <p>STYLE 25:<br/>         PIN 1. VIN<br/>         2. N/C<br/>         3. REXT<br/>         4. GND<br/>         5. IOUT<br/>         6. IOUT<br/>         7. IOUT<br/>         8. IOUT</p>   | <p>STYLE 26:<br/>         PIN 1. GND<br/>         2. dv/dt<br/>         3. ENABLE<br/>         4. ILIMIT<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. VCC</p>  | <p>STYLE 27:<br/>         PIN 1. ILIMIT<br/>         2. OVLO<br/>         3. UVLO<br/>         4. INPUT+<br/>         5. SOURCE<br/>         6. SOURCE<br/>         7. SOURCE<br/>         8. DRAIN</p>  | <p>STYLE 28:<br/>         PIN 1. SW_TO_GND<br/>         2. DASIC_OFF<br/>         3. DASIC_SW_DET<br/>         4. GND<br/>         5. V_MON<br/>         6. VBULK<br/>         7. VBULK<br/>         8. VIN</p>  |
| <p>STYLE 29:<br/>         PIN 1. BASE, DIE #1<br/>         2. EMITTER, #1<br/>         3. BASE, #2<br/>         4. EMITTER, #2<br/>         5. COLLECTOR, #2<br/>         6. COLLECTOR, #2<br/>         7. COLLECTOR, #1<br/>         8. COLLECTOR, #1</p>                        | <p>STYLE 30:<br/>         PIN 1. DRAIN 1<br/>         2. DRAIN 1<br/>         3. GATE 2<br/>         4. SOURCE 2<br/>         5. SOURCE 1/DRAIN 2<br/>         6. SOURCE 1/DRAIN 2<br/>         7. SOURCE 1/DRAIN 2<br/>         8. GATE 1</p>                           |  |  |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42564B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC-8 NB</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative