CY2071A

Single-PLL General-Purpose EPROM Programmable Clock Generator

Features

- Single phase-locked loop architecture
- EPROM programmability
- Factory-programmable (CY2071A, CY2071AI) or field-programmable (CY2071AF, CY2071AFI) device options
- Up to three configurable outputs
- Low skew, low jitter, high-accuracy outputs
- Internal loop filter
- Power management (OE)
- Frequency select options
- Configurable 5V or 3.3V operation
- 8-pin 150-mil SOIC package

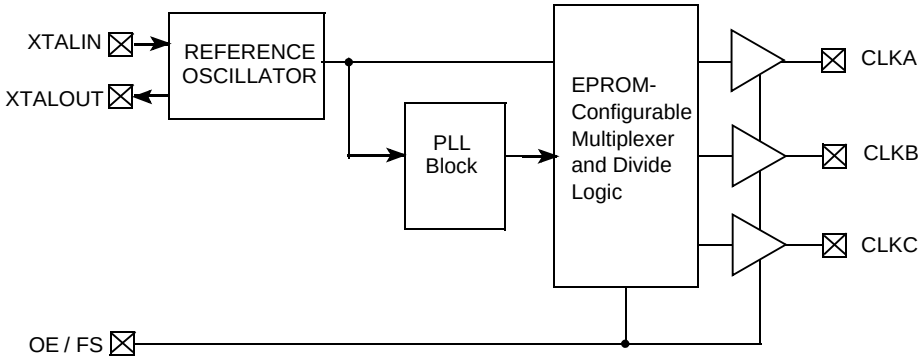
Benefits

- Generates a custom frequency from an external source
- Easy customization and fast turnaround
- Programming support available for all opportunities
- Generates three related frequencies from a single device
- Meets critical industry standard timing requirements
- Alleviates the need for external components
- Supports low-power applications
- Three outputs with two user-selectable frequencies
- Supports industry standard design platforms
- Industry standard packaging saves on board space

Selector Guide

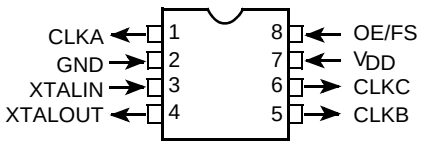
Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2071A	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–130 MHz (5V) 500 kHz–100 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2071AI	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2071AF	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	***Field Programmable*** Commercial Temperature
CY2071AFI	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–90 MHz (5V) 500 kHz–66.6 MHz (3.3V)	***Field Programmable*** Industrial Temperature

Logic Block Diagram for CY2071A



Pin Configuration

8-pin SOIC
Top View



Pin Summary

Name	Number	Description
CLKA	1	Configurable Clock Output
GND	2	Ground
XTALIN[1]	3	Reference Crystal Input or External Reference Clock Input
XTALOUT[1, 2]	4	Reference Crystal Feedback
CLKB	5	Configurable Clock Output
CLKC	6	Configurable Clock Output
V_{DD}	7	Voltage Supply
OE / FS	8	Output Control Pin, either Output Enable or Frequency Select Input (Active HIGH, internal pull-up resistor to V_{DD})

Functional Description

The CY2071A is a general-purpose clock synthesizer designed for use in applications such as modems, disk drives, CD-ROM drives, video CD players, games, set-top boxes, and data/telecommunications. The device offers up to three configurable clock outputs in an 8-pin, 150-mil SOIC package and can operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10 MHz to 25 MHz crystals. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used.

The CY2071A has one PLL and outputs three factory-EPROM configurable clocks: CLKA, CLKB, and CLKC. The output clocks can originate either from the PLL or the reference, or selected dividers thereof. Additionally, pin 8 can be configured to be an Output Enable or a Select input.

The CY2071A can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to the manufacturer. Hence, these devices are ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard-disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

CyClocks Software

CyClocks™ is an easy-to-use software application that allows you to configure any one of the EPROM-Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. You can download a copy of CyClocks free on the Cypress Semiconductor Corporation web site at www.cypress.com.

Use the CY2081 for applications that require unrelated output frequencies. Use the CY2291, CY2292, or CY2907 for applications that require more than three output clocks.

Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmer is a portable programmer designed to custom program our family of EPROM Field Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Absolute Maximum Conditions[3, 4]

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Analog Supply Voltage		–0.5	7.0	V
V_{IN}	DC Input Voltage		–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Maximum Soldering (10 sec)	Functional	–	260	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V

Notes
1. For best accuracy, use a parallel-resonant crystal, C_L = 17 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).
3. Stresses greater than those listed in this table may cause permanent damage to the device.
4. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Operating Conditions[5]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5.0V Operation	4.5	5.5	V
V_{DD}	Supply Voltage, 3.3V Operation	3.0	3.6	V
T_A	Commercial Operating Temperature, Ambient	0	70	°C
	Industrial Operating Temperature, Ambient	–40	85	°C
C_L	Max. Load Capacitance per Output (5V Operation)	–	25	pF
	Max. Load Capacitance per Output (3.3V Operation)	–	15	pF
f_{REF}	External Reference Crystal	10.0	25.0	MHz
	External Reference Clock[6, 7]	1.0	30.0	MHz
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics, Commercial 5.0V: V_{DD} = 5V ±10%, T_A = 0°C to +70°C[8]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = –4.0 mA	2.4	–	–	V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA	–	–	0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except Crystal Pins	2.0	–	–	V
V_{IL}	LOW-Level Output Voltage[9]	Except Crystal Pins	–	–	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V	–	–	10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V	–	–	150	µA
I_{OZ}	Output Leakage Current	Three State Outputs	–	–	250	µA
I_{DD}	V_{DD} Supply Current[10]	V_{DD} = V_{DD} max. 5V operation, C_L = 25 pF		40	60	mA

Electrical Characteristics, Commercial 3.3V: V_{DD} = 3.3V ±10%, T_A = 0°C to 70°C[8]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = –4.0 mA	2.4	–	–	V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA	–	–	0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except Crystal Pins	2.0	–	–	V
V_{IL}	LOW-Level Output Voltage[9]	Except Crystal Pins	–	–	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V	–	–	10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V	–	–	150	µA
I_{OZ}	Output Leakage Current	Three State Outputs	–	–	250	µA
I_{DD}	V_{DD} Supply Current[10]	V_{DD} = V_{DD} max. 3.3V operation, C_L = 15 pF	–	24	40	mA

Notes:

5. Electrical parameters are guaranteed with these operating conditions. Values for 3.3V operation are shown in parentheses.
6. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
7. Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
8. See “CY2071A and CY2907 Clock Generators” Application Note for important customer clarification.
9. Xtal inputs have CMOS thresholds.
10. Load = max, typical configuration, f_{REF} = 14.318 MHz. Specific configurations may vary. A close approximation of I_{DD} can be derived by the following formula: $I_{DD}(mA) = V_{DD}*(6.25+(0.055*F_{REF}) + (0.0017*C_{LOAD}*(F_{CLKA}+F_{CLKB}+F_{CLKC}))$. C_{LOAD} is specified in pF and F is specified in MHz.

Electrical Characteristics, Industrial 5.0V: V_{DD} = 5.0V ±10%, T_A = –40°C to 85°C[8]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = –4.0 mA	2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except Crystal Pins	2.0			V
V_{IL}	LOW-Level Output Voltage[9]	Except Crystal Pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V			150	µA
I_{OZ}	Output Leakage Current	Three State Outputs			250	µA
I_{DD}	V_{DD} Supply Current[10]	V_{DD} = V_{DD} max. 5V operation, C_L = 25 pF		40	75	mA

Electrical Characteristics, Industrial 3.3V V_{DD} =3.3V ±10%, T_A = –40°C to +85°C[8]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = –4.0 mA	2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA			0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except Crystal Pins	2.0			V
V_{IL}	LOW-Level Output Voltage[9]	Except Crystal Pins			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD} – 0.5V			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V			150	µA
I_{OZ}	Output Leakage Current	Three State Outputs			250	µA
I_{DD}	V_{DD} Supply Current[10]	V_{DD} = V_{DD} max. 3.3V operation, C_L = 15 pF		24	50	mA

Switching Characteristics, Commercial 5.0V[11]

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range 5V operation 25-pF load	CY2071A	7.692 [130 MHz]		2000 [500 kHz]	ns
			CY2071AF	10 [100 MHz]		2000 [500 kHz]	ns
t_{1A}	Clock Jitter	Peak-to-peak period jitter (t_1 max. – t_1 min.), % of clock period, $f_{OUT} \leq$ 16 MHz			0.8	1	%
t_{1B}	Clock Jitter	Peak-to-peak period jitter (16 MHz ≤ f_{OUT} ≤ 50 MHz)			350	500	ps
t_{1C}	Clock Jitter[12]	Peak-to-peak period jitter ($f_{OUT} \geq$ 50 MHz)			250	350	ps
	Output Duty Cycle	Duty cycle[13, 14] for outputs, ($t_2 \div t_1$) $f_{OUT} \leq$ 60 MHz		45%	50%	55%	
	Output Duty Cycle[12]	Duty cycle[14] for outputs, ($t_2 \div t_1$), f_{OUT} > 60 MHz		40%	50%	60%	
t_3	Rise Time[12]	Output clock rise time			1.5	2.5	ns
t_4	Fall Time[12]	Output clock fall time			1.5	2.5	ns
t_5	Skew	Skew delay between any two outputs with identical frequencies (generated by the PLL)				0.5	ns

Notes:
11. Guaranteed by design, not 100% tested.
12. When the output clock frequency is between 100 MHz and 130 MHz at 5V, the maximum capacitive load for these measurements is 15 pF.
13. Reference Output duty cycle depends on XTALIN duty cycle.
14. Measured at 1.4V.

Switching Characteristics, Commercial 3.3V[11]

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range 3.3V operation 15-pF load	CY2071AS	10 [100 MHz]		2000 [500 kHz]	ns
			CY2071AF	12.50 [80 MHz]		2000 [500 kHz]	ns
t_{1A}	Clock Jitter	Peak-to-peak period jitter (t_1 max. – t_1 min.), % of clock period, $f_{OUT} \leq 16$ MHz			0.8	1	%
t_{1B}	Clock Jitter	Peak-to-peak period jitter (16 MHz ≤ $f_{OUT} \leq 50$ MHz)			350	500	ps
t_{1C}	Clock Jitter[12]	Peak-to-peak period jitter ($f_{OUT} \geq 50$ MHz)			250	350	ps
	Output Duty Cycle	Duty cycle[13, 14] for outputs, ($t_2 \div t_1$) $f_{OUT} \leq 60$ MHz		45%	50%	55%	
	Output Duty Cycle[12]	Duty cycle[14] for outputs, ($t_2 \div t_1$), $f_{OUT} > 60$ MHz		40%	50%	60%	
t_3	Rise Time[12]	Output clock rise time			1.5	2.5	ns
t_4	Fall Time[12]	Output clock fall time			1.5	2.5	ns
t_5	Skew	Skew delay between any two outputs with identical frequencies (generated by the PLL)				0.5	ns

Switching Characteristics, Industrial 5.0V[11]

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range 5.0V operation 25-pF load	CY2071AI	10 [100 MHz]		2000 [500 kHz]	ns
			CY2071AFI	11.1 [90 MHz]		2000 [500 kHz]	ns
t_{1A}	Clock Jitter	Peak-to-peak period jitter (t_1 max. – t_1 min.), % of clock period, $f_{OUT} \leq 16$ MHz			0.8	1	%
t_{1B}	Clock Jitter	Peak-to-peak period jitter (16 MHz ≤ $f_{OUT} \leq 50$ MHz)			350	500	ps
t_{1C}	Clock Jitter[12]	Peak-to-peak period jitter ($f_{OUT} \geq 50$ MHz)			250	350	ps
	Output Duty Cycle	Duty cycle[13, 14] for outputs, ($t_2 \div t_1$) $f_{OUT} \leq 60$ MHz		45%	50%	55%	
	Output Duty Cycle[12]	Duty cycle[14] for outputs, ($t_2 \div t_1$), $f_{OUT} > 60$ MHz		40%	50%	60%	
t_3	Rise time[12]	Output clock rise time			1.5	2.5	ns
t_4	Fall time[12]	Output clock fall time			1.5	2.5	ns
t_5	Skew	Skew delay between any two outputs with identical frequencies (generated by the PLL)				0.5	ns

Switching Characteristics, Industrial 3.3V[11]

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range 3.3V operation 15-pF load	CY2071AI	12.50 [80 MHz]		2000 [500 kHz]	ns
			CY2071AFI	15.0 [66.6 MHz]		2000 [500 kHz]	ns
t_{1A}	Clock Jitter	Peak-to-peak period jitter (t_1 max. – t_1 min.), % of clock period, $f_{OUT} \leq 16$ MHz			0.8	1	%
t_{1B}	Clock Jitter	Peak-to-peak period jitter (16 MHz ≤ f_{OUT} ≤ 50 MHz)			350	500	ps
t_{1C}	Clock Jitter[12]	Peak-to-peak period jitter ($f_{OUT} \geq 50$ MHz)			250	350	ps
	Output Duty Cycle	Duty cycle[13, 14] for outputs, ($t_2 \div t_1$) $f_{OUT} \leq 60$ MHz		45%	50%	55%	
	Output Duty Cycle[12]	Duty cycle[14] for outputs, ($t_2 \div t_1$), $f_{OUT} > 60$ MHz		40%	50%	60%	
t_3	Rise time[12]	Output clock rise time			1.5	2.5	ns
t_4	Fall time[12]	Output clock fall time			1.5	2.5	ns
t_5	Skew	Skew delay between any two outputs with identical frequencies (generated by the PLL)				0.5	ns

Switching Waveforms

Figure 1. All Outputs Duty Cycle and Rise/Fall Time

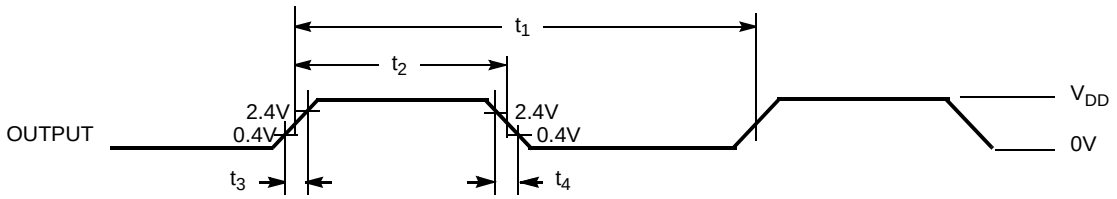
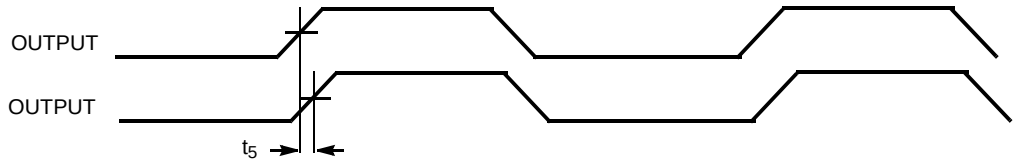
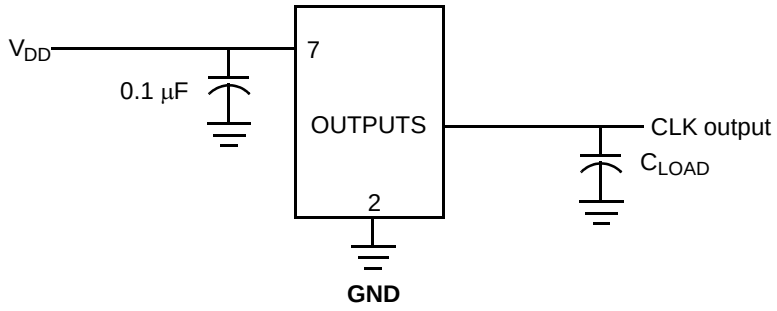


Figure 2. Output-Output Clock Skew



Test Circuit



Ordering Information

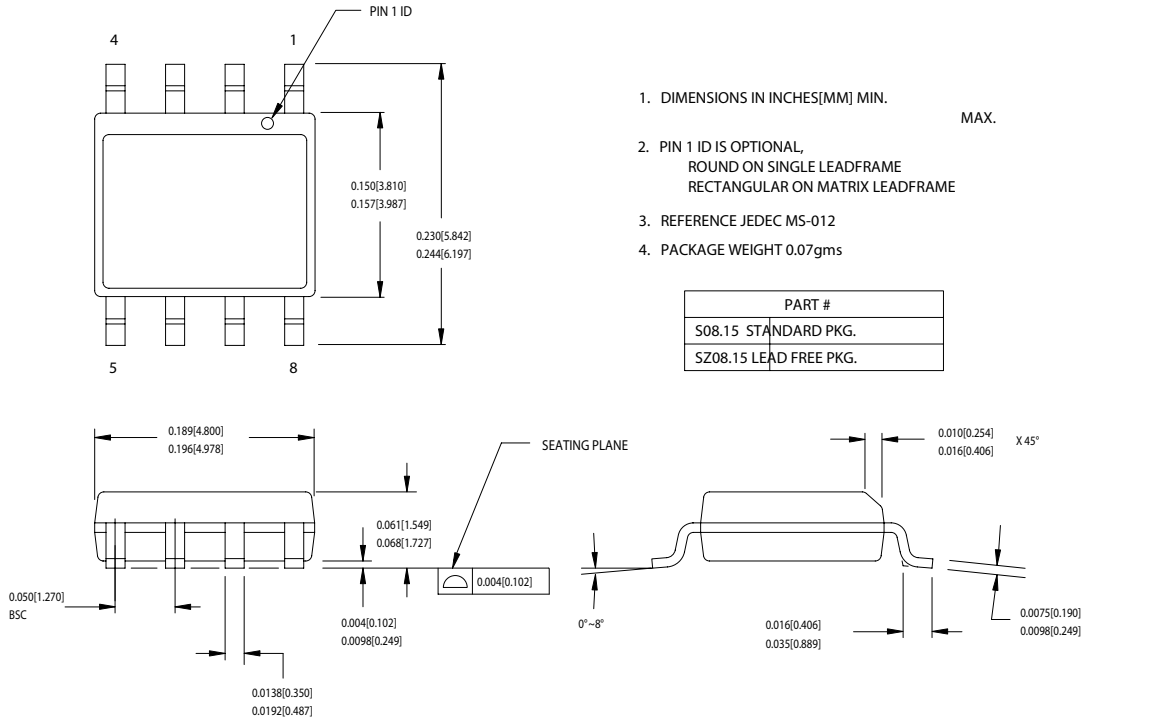
Ordering Code	Package Type	Operating Range
CY2071ASC-XXX	8-Pin (150-Mil) SOIC	5.0V, Commercial, Factory Programmable
CY2071ASC-XXXT	8-Pin (150-Mil) SOIC – Tape and Reel	5.0V, Commercial, Factory Programmable
CY2071ASL-XXX	8-Pin (150-Mil) SOIC	3.3V, Commercial, Factory Programmable
CY2071ASL-XXXT	8-Pin (150-Mil) SOIC – Tape and Reel	3.3V, Commercial, Factory Programmable
CY2071ASI-XXX	8-Pin (150-Mil) SOIC	5V/3.3V, Industrial, Factory Programmable
CY2071ASI-XXXT	8-Pin (150-Mil) SOIC – Tape and Reel	5V/3.3V, Industrial, Factory Programmable
CY2071AF	8-Pin (150-Mil) SOIC	5V/3.3V, Commercial, Field Programmable
CY2071AFT	8-Pin (150-Mil) SOIC – Tape and Reel	5V/3.3V, Commercial, Field Programmable
CY2071AFI	8-Pin (150-Mil) SOIC	5V/3.3V, Industrial, Field Programmable
CY2071AFIT	8-Pin (150-Mil) SOIC – Tape and Reel	5V/3.3V, Industrial, Field Programmable
CY3670	FTG Programmer	Custom programming for Field Programmable Clocks
Lead-Free		
CY2071ASXC-XXX	8-Pin (150-Mil) SOIC	5.0V, Commercial, Factory Programmable
CY2071ASXC-XXXT	8-Pin (150-Mil) SOIC - Tape and Reel	5.0V, Commercial, Factory Programmable
CY2071ASXL-XXX	8-Pin (150-Mil) SOIC	3.3V, Commercial, Factory Programmable
CY2071ASXL-XXXT	8-Pin (150-Mil) SOIC- Tape and Reel	3.3V, Commercial, Factory Programmable
CY2071ASXI-XXX	8-Pin (150-Mil) SOIC	5V/3.3V, Industrial, Factory Programmable
CY2071ASXI-XXXT	8-Pin (150-Mil) SOIC- Tape and Reel	5V/3.3V, Industrial, Factory Programmable
CY2071AFXC	8-Pin (150-Mil) SOIC	5V/3.3V, Commercial, Field Programmable
CY2071AFXCT	8-Pin (150-Mil) SOIC- Tape and Reel	5V/3.3V, Commercial, Field Programmable
CY2071AFXI	8-Pin (150-Mil) SOIC	5V/3.3V, Industrial, Field Programmable
CY2071AFXIT	8-Pin (150-Mil) SOIC- Tape and Reel	5V/3.3V, Industrial, Field Programmable

Package Characteristics

Package	θ_{JA} (C/W)	θ_{JC} (C/W)	Transistor Count
8 Pin SOIC	170	35	5436

Package Drawing and Dimensions

Figure 3. 8-lead (150-Mil) SOIC S8



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Document History Page

Document Title: CY2071A Single-PLL General-Purpose EPROM Programmable Clock Generator Document Number: 38-07139				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110248	12/17/01	SZV	Change from Spec number: 38-00521 to 38-07139
*A	121827	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	279389	See ECN	RGL	Added lead-free devices
*C	296792	See ECN	RGL	Minor Typo: missed one letter (C) in the ordering code
*D	492389	See ECN	RGL	Added a note on all Electrical specs table specifying the Application notes name for customer's clarification Reformatted using new template