

Low Offset, Low Drift single JFET Input Operational Amplifier

■GENERAL DESCRIPTION

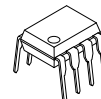
The **NJM2748/2748A** is a Precision dual JFET input operational amplifier which includes low input offset voltage: 0.7mV (typ) / 2.0mV (max) and 6 μ V/°C typical offset drift.

The **NJM2748A** is guaranteed 20 μ V/°C maximum offset drift to perform a 100% tested.

The **NJM2748/2748A** have the following features: low bias current of 50pA (typ), high slew rate of 13V/ μ s (typ).

These features are suitable for signal processing amplifiers of instrumentation, measurement and industrial applications such as sensor amplifier, current sensing and sample-and-hold circuit.

■PACKAGE OUTLINE



NJM2748D/2748AD

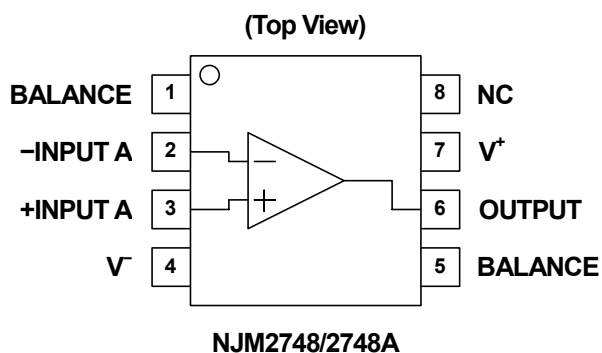


NJM2748M/2748AM

■FEATURES

- | | |
|-----------------------------|--|
| ●Input Offset Voltage Drift | NJM2748: $\Delta V_{IO}/\Delta T = 6\mu\text{V}/^\circ\text{C}$ typ.
NJM2748A: $\Delta V_{IO}/\Delta T = 20\mu\text{V}/^\circ\text{C}$ max. |
| ●Input Offset Voltage | 2.0mV max. @Ta=25°C ~ 85°C
3.0mV max. @Ta= -40°C |
| ●Input Bias Current | $I_B = 50\text{pA}$ typ. 200pA max. @Ta=25°C |
| ●Slew Rate | SR=13V/ μ s typ. @Ta=25°C |
| ●Operating Voltage | Vopr= $\pm 6.0\text{V} \sim \pm 16\text{V}$ |
| ●Voltage Gain | $A_v = 100\text{dB}$ typ. |
| ●Bipolar Technology | |
| ●Package Outline | NJM2748D, NJM2748AD :DIP8
NJM2748M, NJM2748AM :DMP8 |

■PIN CONFIGURATION



NJM2748/2748A

■ABSOLUTE MAXIMUM RATING (Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V ⁺ /V ⁻	±18	V
Common Mode Input Voltage	V _{ICM}	±15 (Note1)	V
Differential Input Voltage	V _{ID}	±30	V
Power Dissipation	P _D	500 [DIP8], 300 [DMP8]	mW
		430 [DMP8] (Note2)	mW
		580 [DMP8] (Note3)	mW
Operating Temperature Range	T _{opr}	-40 ~ +85	°C
Storage Temperature Range	T _{stg}	-50 ~ +125	°C

(Note1) For supply voltage less than ±18V, the maximum input voltage is equal to the supply voltage.

(Note2) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, two layer, FR-4).

(Note3) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, four layer, FR-4).

■RECOMMENDED OPERATING VOLTAGE (Ta=25°C)

PARAMETER	SYMBOL	RATING	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V ⁺ /V ⁻		±6	-	±16	V

■ELECTRONIC CHARACTERISTICS

●DC CHARACTERISTICS (V⁺/V⁻=±15V, Ta=-40 to +85°C (Note4) unless otherwise specified)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage Drift	ΔV _{IO} /ΔT	NJM2748A (Note5, 6)	-	6	20	μV/°C
		NJM2748	-	6	-	
Input Offset Voltage1	V _{IO1}	R _S =50Ω, Ta=+85°C (Note6, 7)	-	0.6	2.0	mV
Input Offset Voltage2	V _{IO2}	R _S =50Ω, Ta=+25°C (Note6, 7)	-	0.7	2.0	mV
Input Offset Voltage3	V _{IO3}	R _S =50Ω, Ta=-40°C (Note6, 7)	-	0.9	3.0	mV
Common Mode Rejection Ratio	CMR	V _{ICM} =±10V (Note8)	76	92	-	dB
Supply Voltage Rejection Ratio	SVR	V ⁺ /V ⁻ =±6V ~ ±16V (Note7, 9)	80	100	-	dB
Input Common Mode Voltage Range 1	V _{ICM1}	CMR≥76dB (Note10)	+10	+14.5	-	V
Input Common Mode Voltage Range 2	V _{ICM2}	CMR≥76dB (Note10)	-	-11	-10	V
Input Bias Current 1	I _{B1}	Ta=+25°C (Note7)	-	50	200	pA
Input Bias Current 2	I _{B2}	Ta=+85°C (Note7)	-	-	4	nA
Input Offset Current 1	I _{IO1}	Ta=+25°C (Note7)	-	25	100	pA
Input Offset Current 2	I _{IO2}	Ta=+85°C (Note7)	-	-	2	nA
Voltage Gain 1	Av1	R _L =2kΩ, V _o =±10V, Ta=+25°C	88	100	-	dB
Voltage Gain 2	Av2	R _L =2kΩ, V _o =±10V	82	100	-	dB
Maximum Output Voltage 1	V _{OM1}	R _L =10kΩ	±12	±13.5	-	V
Maximum Output Voltage 2	V _{OM2}	R _L =2kΩ	±10	±11.5	-	V
Supply Current	I _{CC}	Voltage Follower, R _L =∞ (Note7)	-	2.0	3.4	mA

(Note4) These devices are measured under three temperature conditions of $T_a = -40^\circ\text{C}$, $+25^\circ\text{C}$, $+85^\circ\text{C}$.

(Note5) Temperature coefficient is calculated by specified change in offset voltage. (Changes $T_a = +25^\circ\text{C}$ to -40°C and $T_a = +25^\circ\text{C}$ to $+85^\circ\text{C}$)

NJM2748A is guaranteed maximum specification because these are 100% tested to operating temperature range.

NJM2748 is guaranteed only typical specification.

(Note6) Written by the absolute rate.

(Note7) Measured at $V_{ICM} = 0\text{V}$

(Note8) CMR is calculated by specified change in offset voltage. ($V_{ICM} = 0\text{V}$ to $+10\text{V}$ and $V_{ICM} = 0\text{V}$ to -10V)

(Note9) SVR is calculated by specified change in offset voltage. ($V^+ / V^- = \pm 6\text{V}$ to $\pm 16\text{V}$)

(Note10) V_{ICM} is input common mode voltage when tested meets specified change in offset voltage is $\text{CMR} \geq 76\text{dB}$.

(A point of reference is offset voltage of $V_{ICM} = 0\text{V}$)

•AC CHARACTERISTICS ($V^+ / V^- = \pm 15\text{V}$, $T_a = +25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Gain Bandwidth Product	GB	$f = 10\text{kHz}$	-	2.2	-	MHz
Unity Gain Frequency	f_T	$A_V = +100$, $R_S = 100\Omega$, $R_L = \infty$, $C_L = 10\text{pF}$	-	2	-	MHz
Phase Margin	Φ_M	$A_V = +100$, $R_S = 100\Omega$, $R_L = \infty$, $C_L = 10\text{pF}$	-	55	-	deg
Input Noise Voltage1	V_{NI1}	$f = 1\text{kHz}$, $A_V = +100$, $R_S = 100\Omega$, $R_L = \infty$	-	20	-	nV/ $\sqrt{\text{Hz}}$
Input Noise Voltage2	V_{NI2}	RIAA, $R_S = 2.2\text{k}\Omega$, 30kHz , LPF	-	2.5	-	μVrms
Total Harmonic Distortion	THD	$f = 1\text{kHz}$, $A_V = +10$, $R_S = 1\text{k}\Omega$, $R_L = \infty$, $V_O = 5\text{Vrms}$	-	0.005	-	%

•TRANSIENT CHARACTERISTICS ($V^+ / V^- = \pm 15\text{V}$, $T_a = +25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive Slew Rate	+SR	$A_V = +1$, $V_{IN} = 2\text{Vpp}$, $R_L = 10\text{k}\Omega$, $C_L = 10\text{pF}$	-	14	-	V/ μs
Negative Slew Rate	-SR	$A_V = +1$, $V_{IN} = 2\text{Vpp}$, $R_L = 10\text{k}\Omega$, $C_L = 10\text{pF}$	-	12	-	V/ μs

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■IMPORTANT CONSIDERATIONS FOR USE OF NJM2748/2748A

●Supply Current

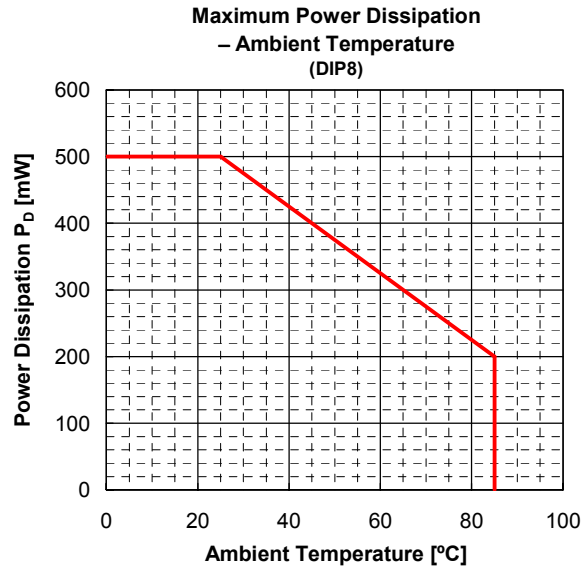
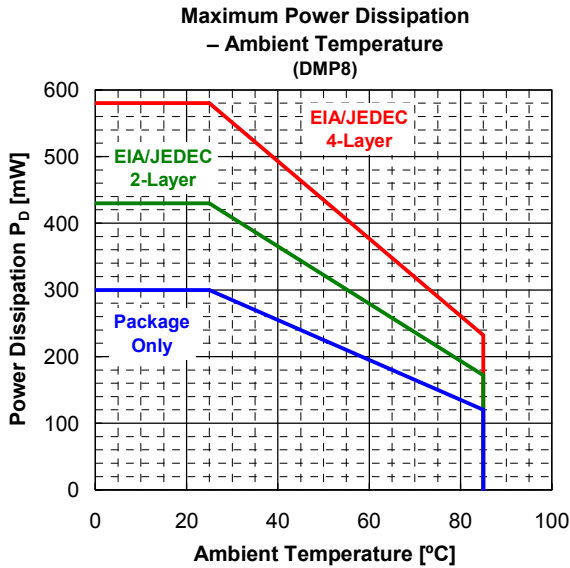
When $T_a \geq 25^\circ\text{C}$, Power Dissipation P_D is limited by junction temperature ($T_j = 125^\circ\text{C}$)

So maximum supply current is influenced by package, mounting board (board size, area of copper foil), Mounting condition and etc.

Following DMP8 Power Dissipation characteristic is a characteristic when mounted the following conditions supply.

- Two layer board: EIA/JEDEC 76.2×114.3×1.6mm, FR-4
- Four layer board: EIA/JEDEC 76.2×114.3×1.6mm, FR-4

Please refer to "Method of measuring the package thermal characteristic" published in our company web site for detailed information on the thermal characteristic.

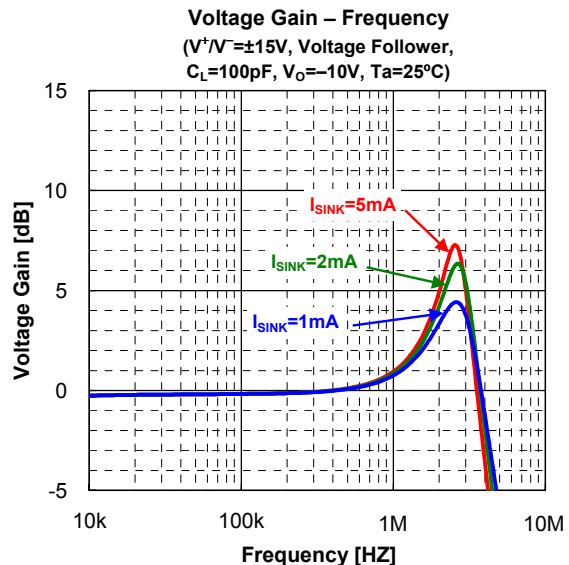
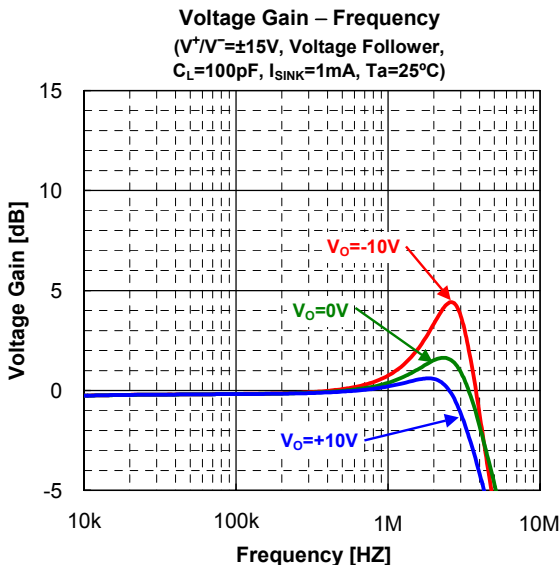


●THE OSCILLATION WITH A CAPACITIVE LOAD

NJM2748/2748A tends to oscillate easily when it uses voltage-follower, and driving capacitive load.

The figure below is a "Voltage Gain - Frequency characteristic" in the Voltage-Follower. (It is not the one to guarantee the characteristic of the product.)

Especially, it becomes easy to oscillate in the condition that the input voltage (output voltage) is near the minus supply voltage side and the condition with large output sink current. We will recommend use by some circuit gains.



■ **IMPORTANT CONSIDERATIONS FOR USE OF NJM2748/2748A**

● **INPUT COMMON MODE VOLTAGE RANGE**

In this product, the input offset voltage drift is measured based on the input offset voltage at $V_{ICM}=0V$, and the input voltage range that satisfies the common mode rejection ratio 76dB is defined as the input common mode voltage range.

As an electric characteristic, $V_{ICM}=-10V\sim+10V$ at Supply Voltage $V^+/V^-=\pm 15V$ is guaranteed.

It becomes below formula about the input common mode voltage range when the supply voltage changes.

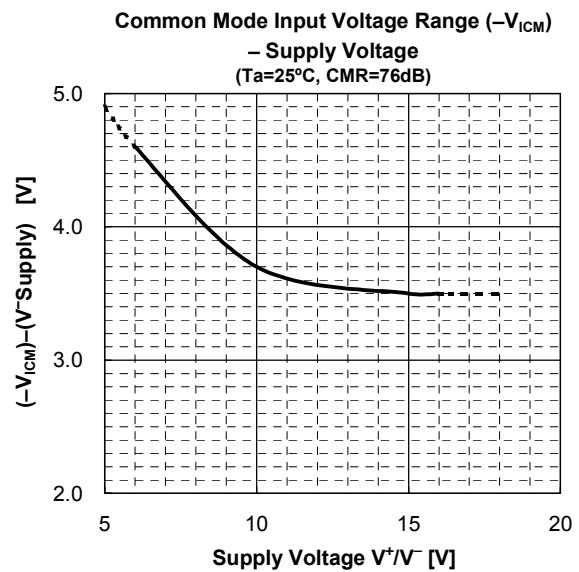
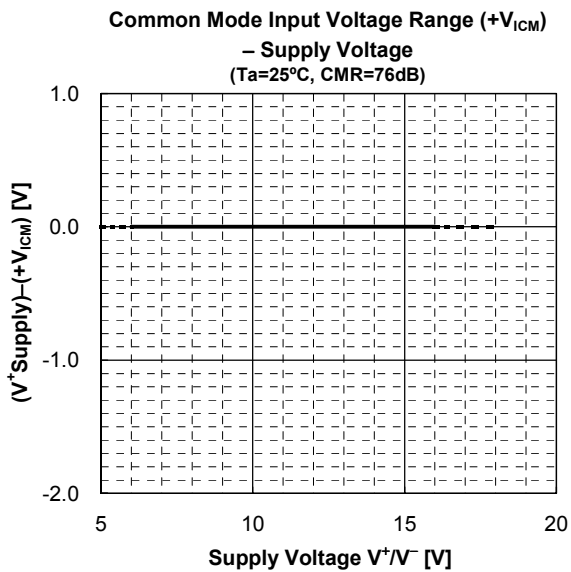
$$+V_{ICM}: (V^+ \text{ supply}) - 5 [V] \cdots \text{reference}$$

$$-V_{ICM}: (V^- \text{ supply}) + 5 [V] \cdots \text{reference}$$

This figure below is "Input common mode voltage range – Supply voltage characteristics". (It is not the one to guarantee the characteristic of the product.)

+ V_{ICM} is limited by the absolute maximum rating (V^+ supply) within the input common mode voltage range.

Moreover, $-V_{ICM}$ tends to rise by lowering of the supply voltage.



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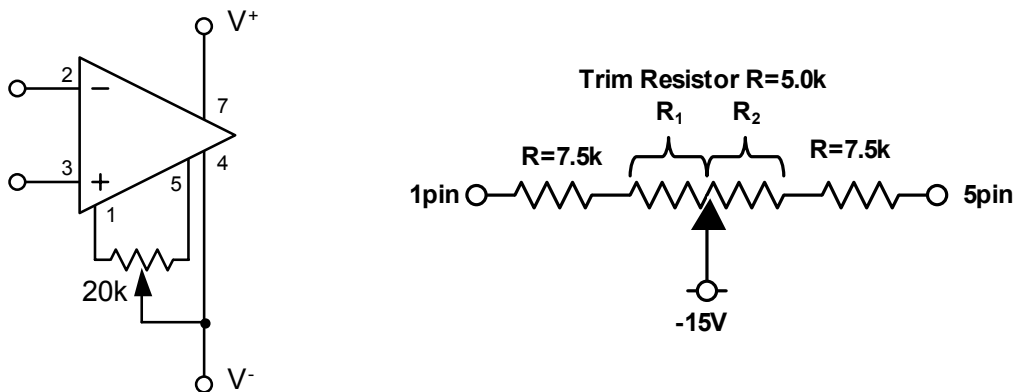
■ OFFSET VOLTAGE TRIM CIRCUIT

The NJM2748 provides offset voltage trim connections on pin 1 and 5.

The offset voltage can be adjusted by connecting Potentiometer as shown in figure.

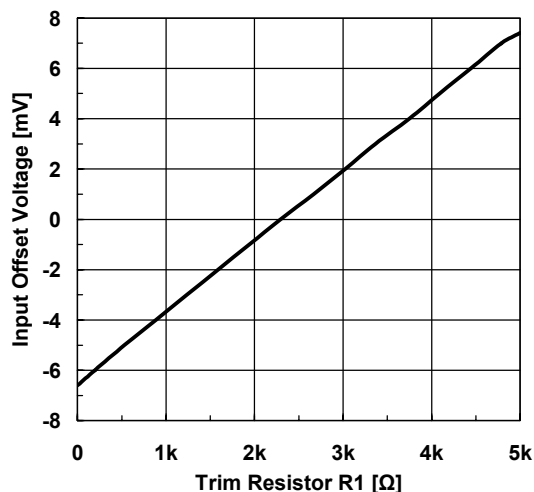
This function adjusts an initial offset voltage, and it doesn't become an improvement of the temperature drift.

Please make pin1 and pin5 open when you don't use this function.



Input Offset Voltage vs. Trim Resistor R1

V⁺/V⁻=±15V, R_{trim}=5kΩ, R=7.5kΩ, T_a=25°C



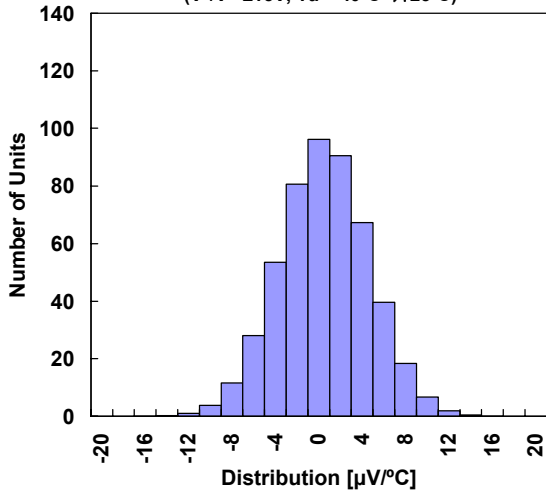
● OTHERS

For the NJM2748/2748A are high-precision products, a surface leak by dirt and/or condensation on package can have a detrimental effect on precise characteristics of these products.

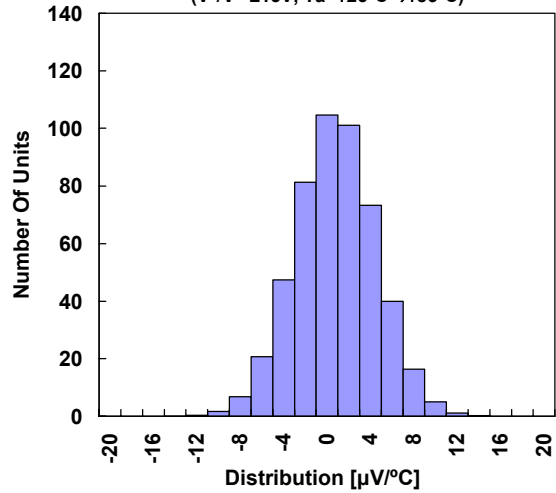
You should pay close attention to environment of storage and usage.

■ TYPICAL CHARACTERISTICS

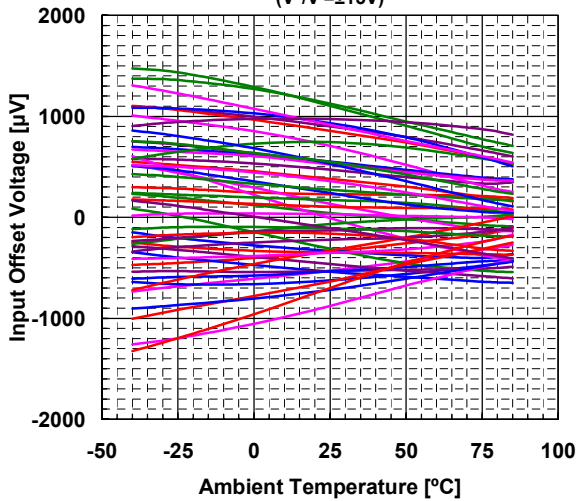
Input Offset Voltage Temperature Coefficient Distribution
($V^+/V^-=\pm 15V$, $T_a=-40^\circ C \rightarrow +25^\circ C$)



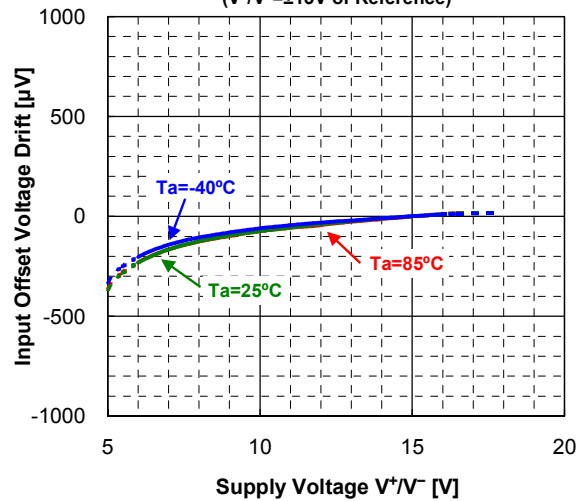
Input Offset Voltage Temperature Coefficient Distribution
($V^+/V^-=\pm 15V$, $T_a=+25^\circ C \rightarrow +85^\circ C$)



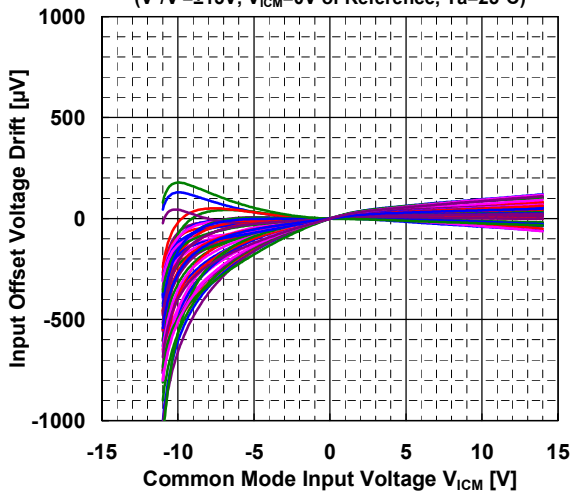
Input Offset Voltage – Ambient Temperature
($V^+/V^-=\pm 15V$)



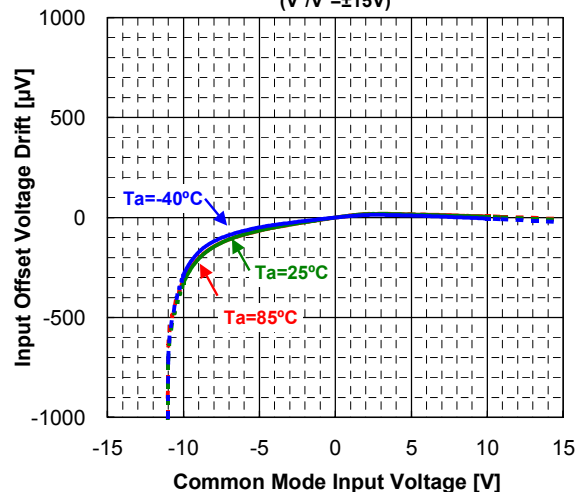
Input Offset Voltage Drift – Supply Voltage
($V^+/V^-=\pm 15V$ of Reference)



Input Offset Voltage Drift – Common Mode Input Voltage
($V^+/V^-=\pm 15V$, $V_{ICM}=0V$ of Reference, $T_a=25^\circ C$)

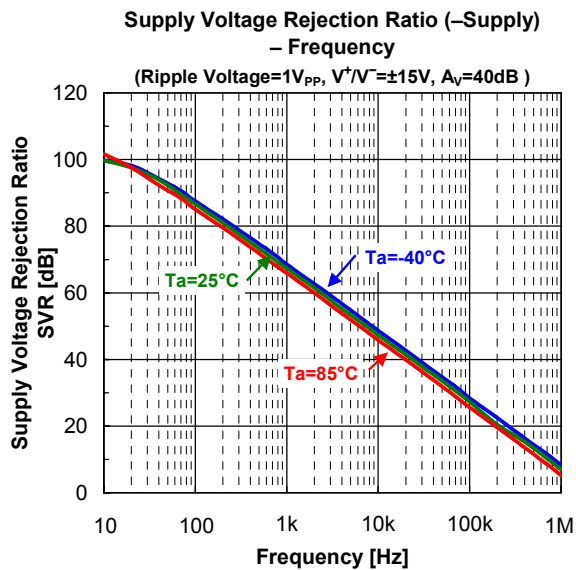
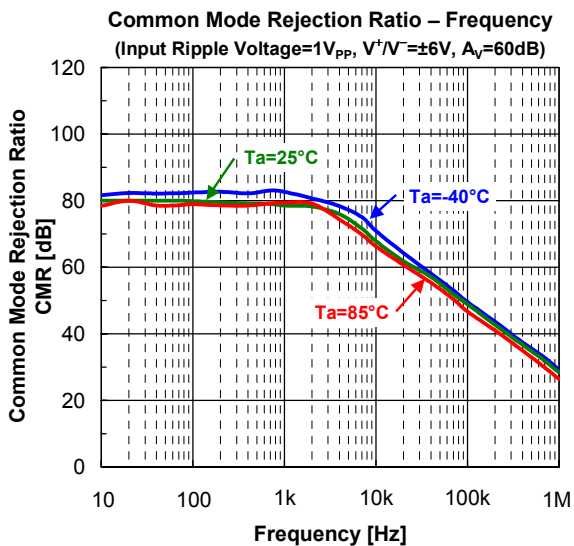
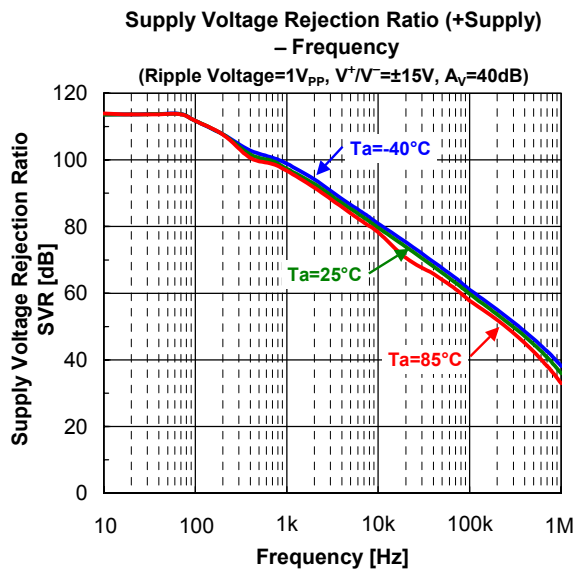
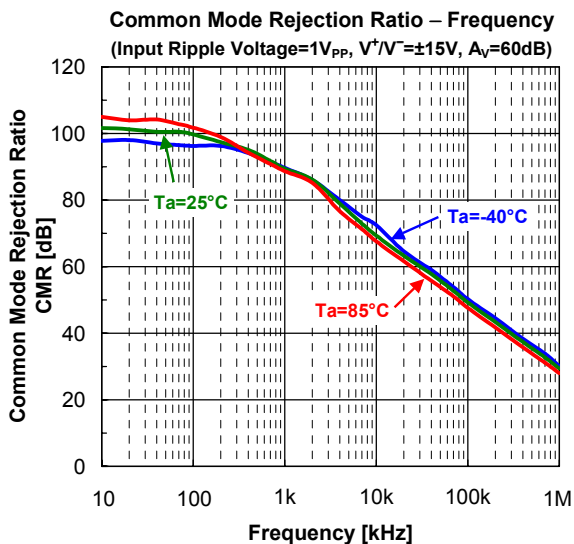
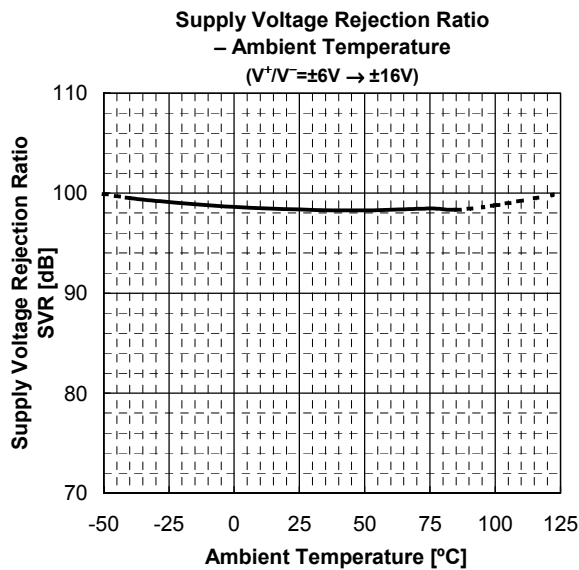
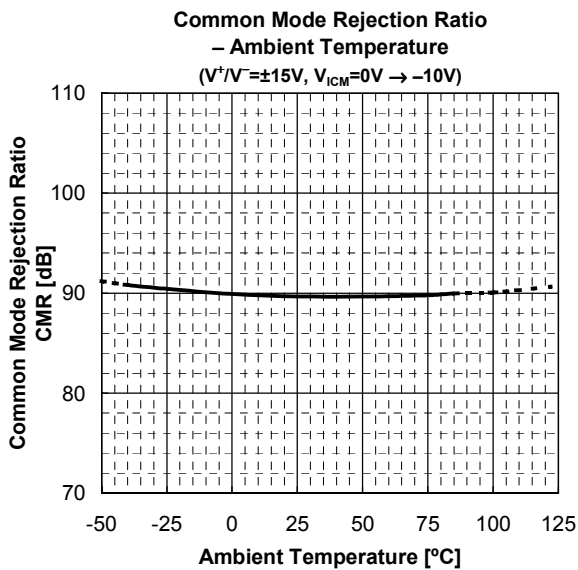


Input Offset Voltage Drift – Common Mode Input Voltage
($V^+/V^-=\pm 15V$)

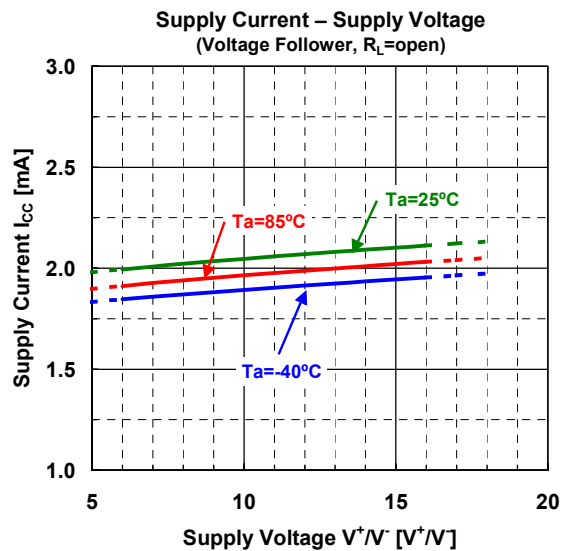
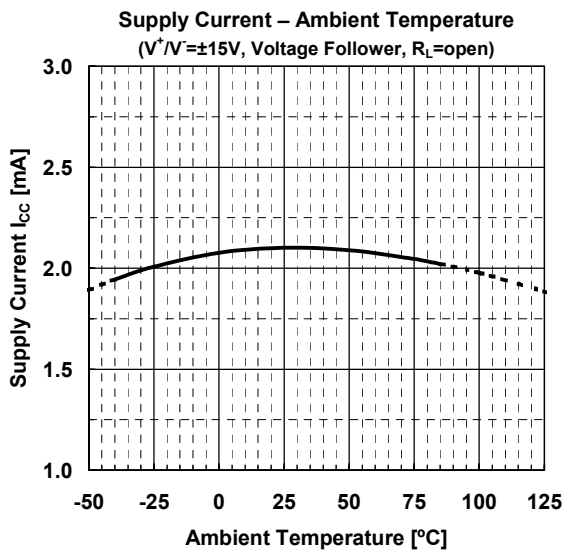
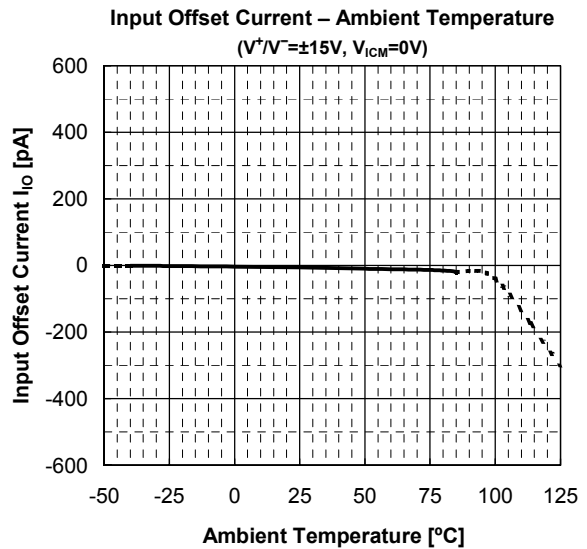
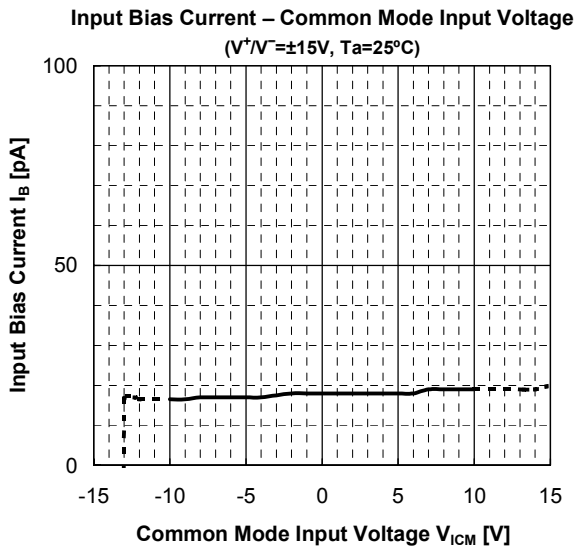
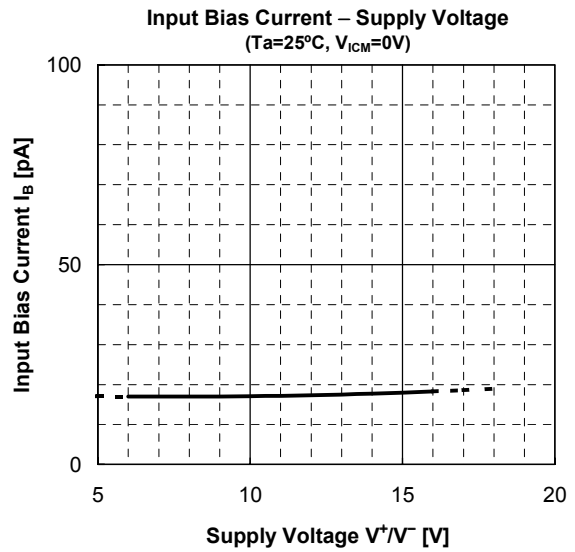
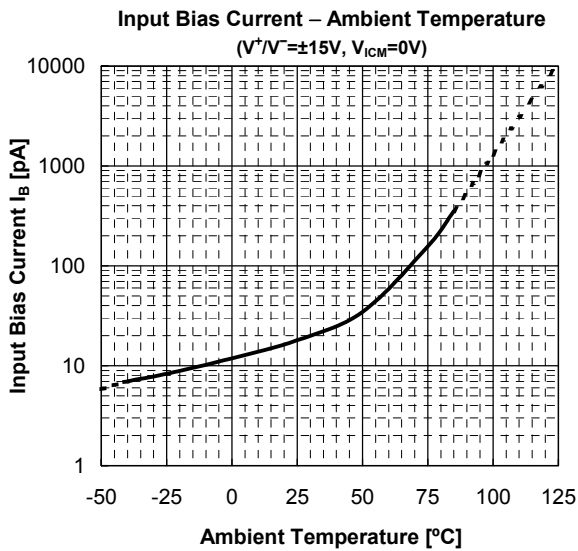


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TYPICAL CHARACTERISTICS

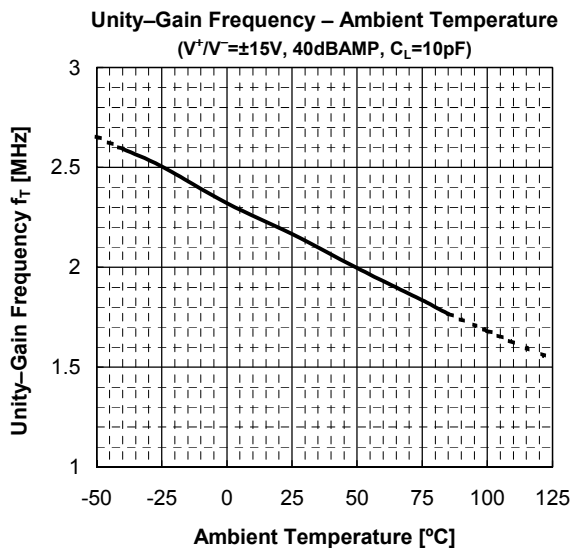
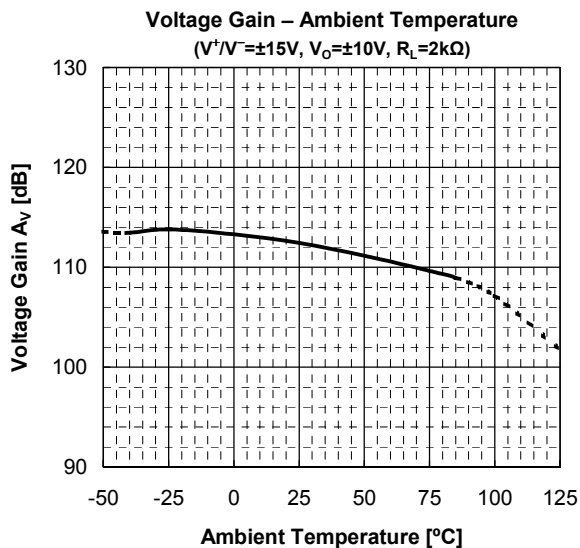
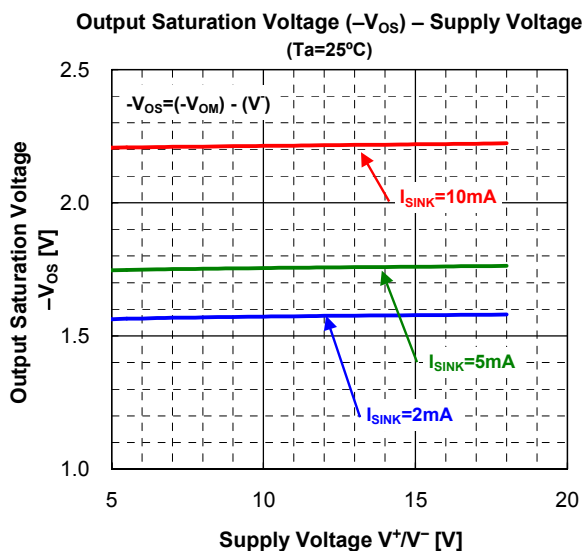
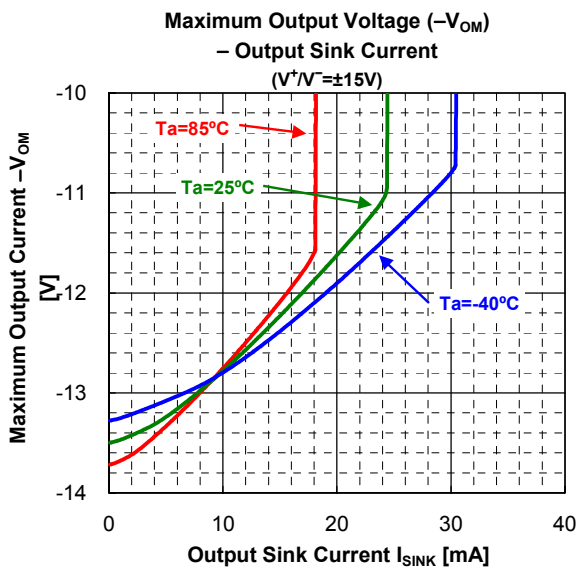
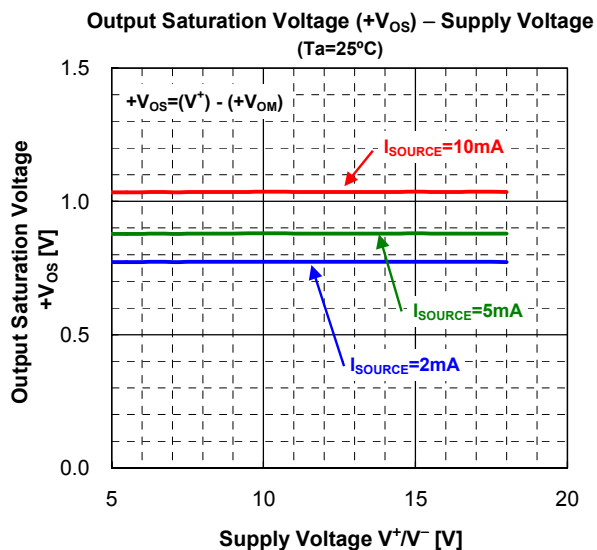
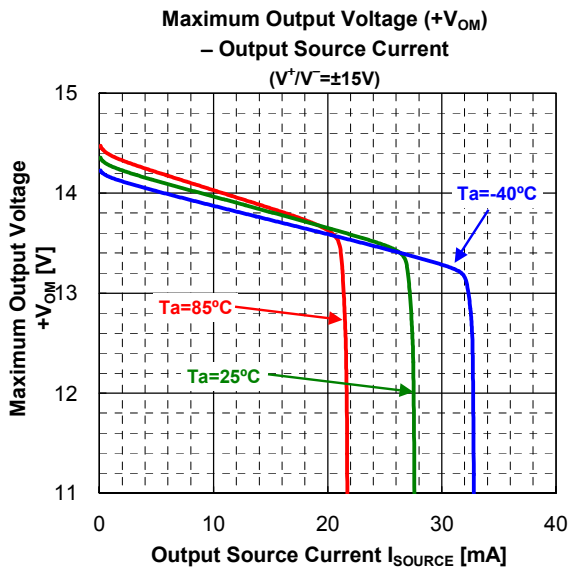


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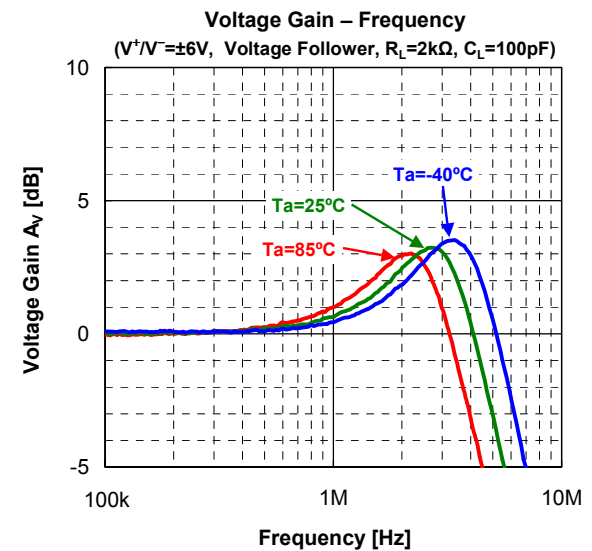
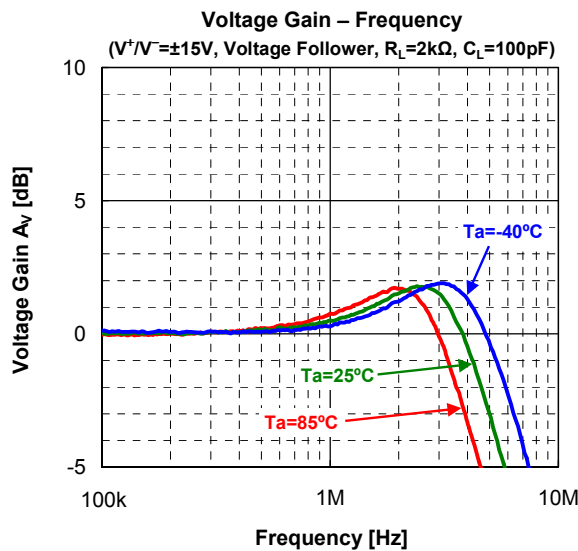
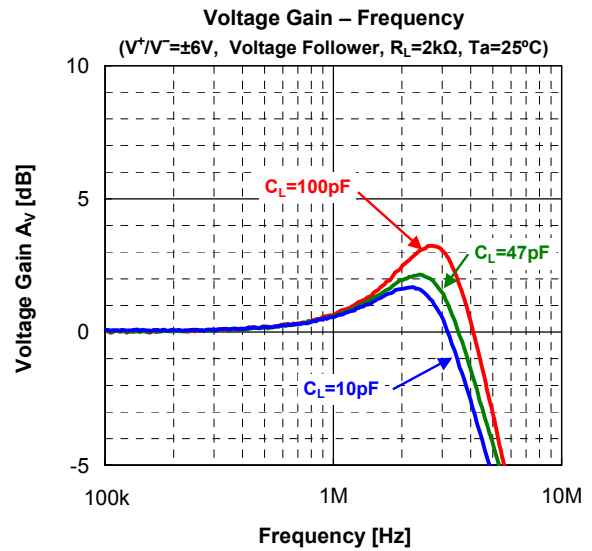
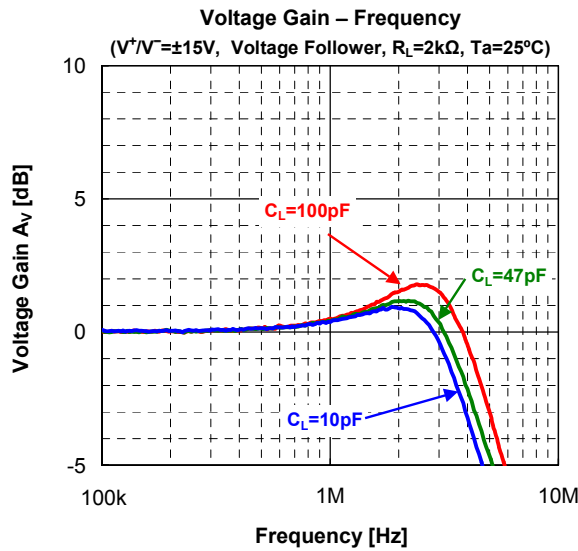
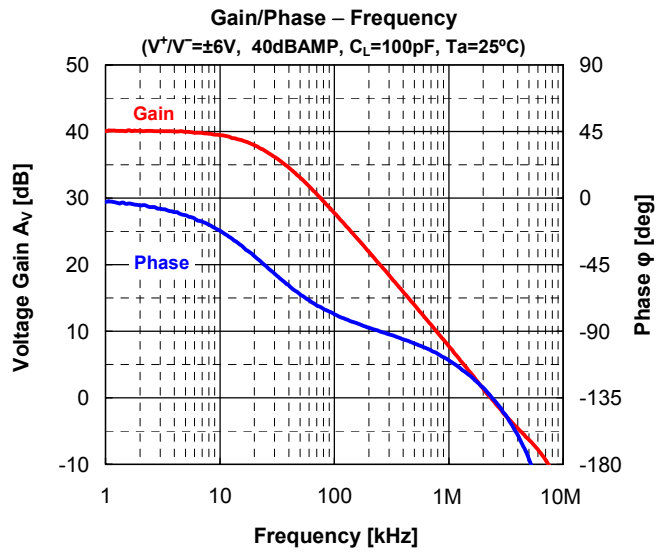
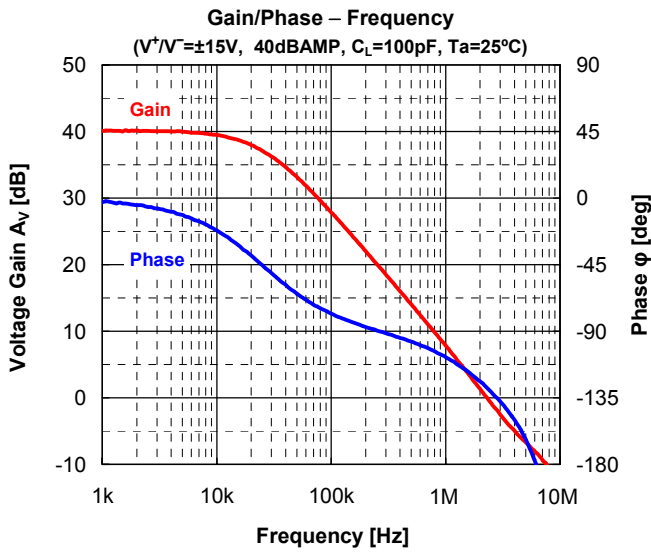


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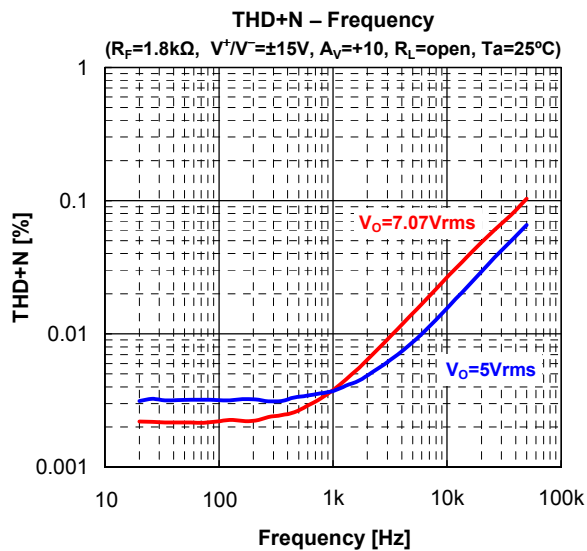
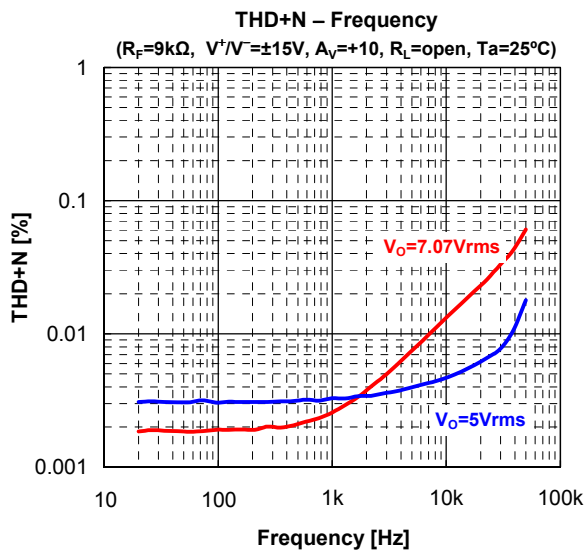
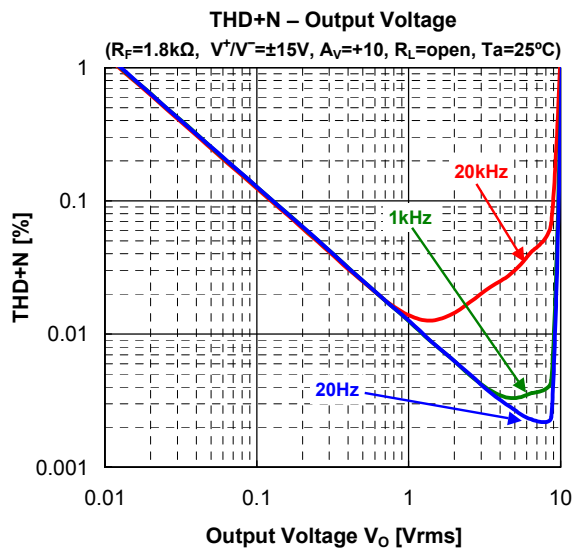
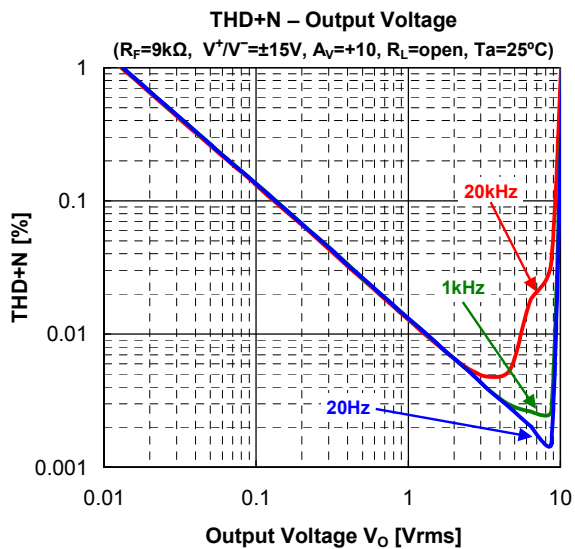
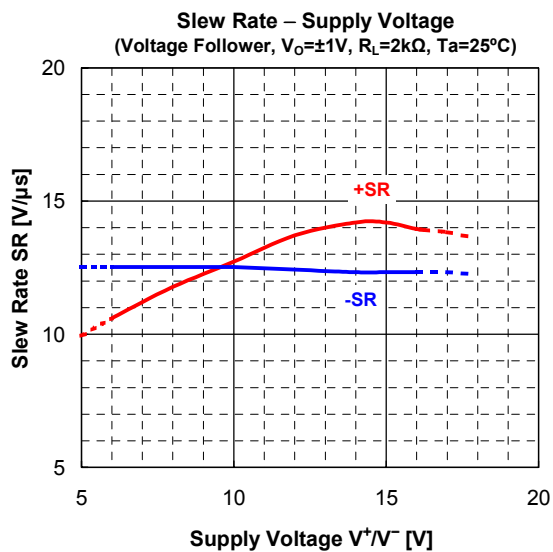
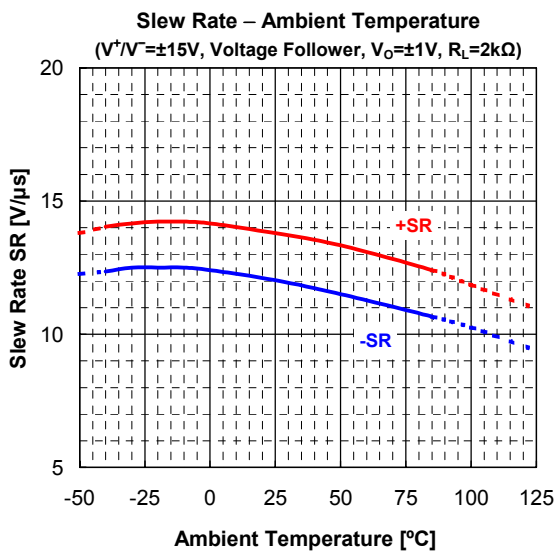


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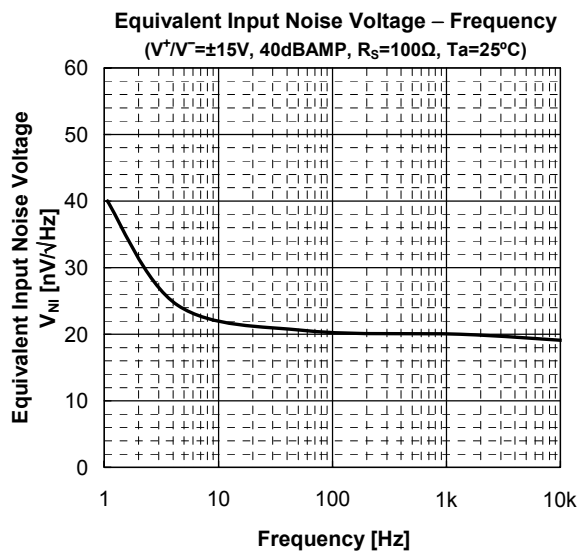


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TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



[CAUTION]

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