

74F113 Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 74F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:

- LOW input to \overline{S}_D sets Q to HIGH level
- Set is independent of clock

Features

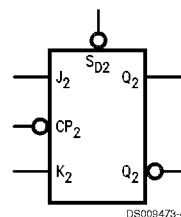
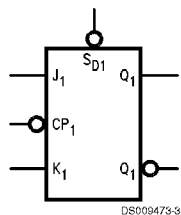
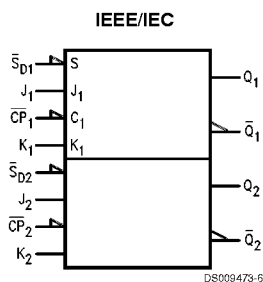
- Guaranteed 4000V minimum ESD protection

Ordering Code:

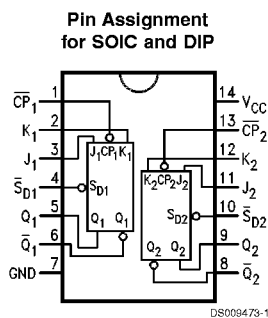
Commercial	Package Number	Package Description
74F113PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74F113SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F113SJ (Note 1)	M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

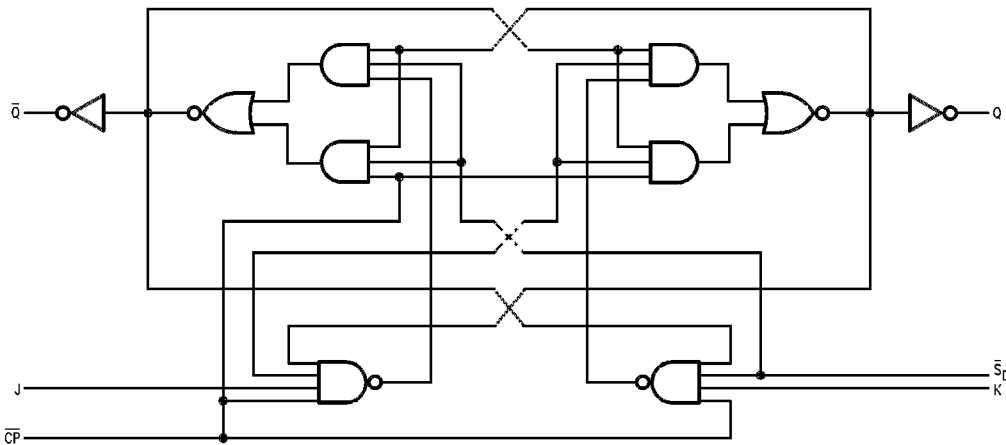
Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	20 μA / -0.6 mA
$\overline{CP}_1, \overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μA / -2.4 mA
$\overline{SD}_1, \overline{SD}_2$	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA / -3.0 mA
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs	50/33.3	-1 mA / 20 mA

Truth Table

Inputs				Outputs	
\overline{SD}	\overline{CP}	J	K	Q	\overline{Q}
L	X	X	X	H	L
H	\sim	h	h	\overline{Q}_o	Q_o
H	\sim	l	h	L	H
H	\sim	h	l	H	L
H	\sim	l	l	Q_o	\overline{Q}_o

H(h) = HIGH Voltage Level
 L(l) = LOW Voltage level
 \sim = HIGH-to-LOW Clock Transition
 X = Immaterial
 $Q_o(\overline{Q}_o)$ = Before HIGH-to-LOW Transition of Clock
 Lower case letters indicate the state of the referenced input or output prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



DS000473-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -2.4 -3.0	mA	Max	V _{IN} = 0.5V (J _n , K _n) V _{IN} = 0.5V (CP _n) V _{IN} = 0.5V (S _{Dn})
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		12	19	mA	Max	

AC Electrical Characteristics

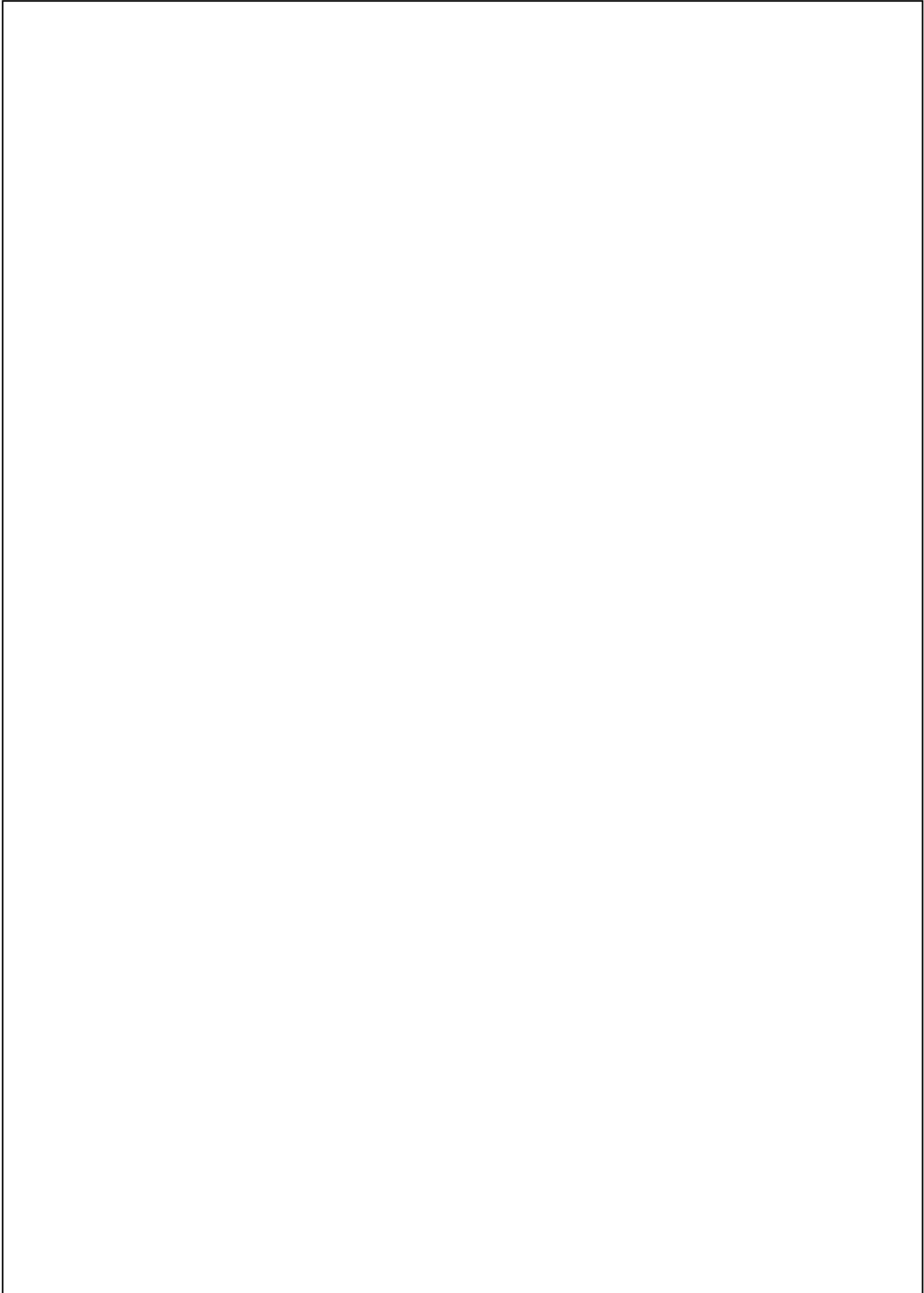
Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	85	105		80		MHz

AC Electrical Characteristics (Continued)

Symbol	Parameter	74F			74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.0	4.0	6.0	2.0	7.0	ns
t _{PHL}	\overline{CP}_n to Q _n or \overline{Q}_n	2.0	4.0	6.0	2.0	7.0	
t _{PLH}	Propagation Delay	2.0	4.5	6.5	2.0	7.5	ns
t _{PHL}	\overline{SD}_n to Q _n or \overline{Q}_n	2.0	4.5	6.5	2.0	7.5	

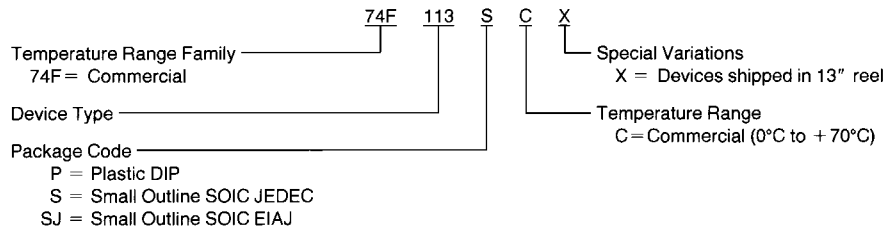
AC Operating Requirements

Symbol	Parameter	74F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Com		
		Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW	4.0		5.0		ns
t _s (L)	J _n or K _n to \overline{CP}_n	3.0		3.5		
t _h (H)	Hold Time, HIGH or LOW	0		0		
t _h (L)	J _n or K _n to \overline{CP}_n	0		0		
t _w (H)	\overline{CP}_n Pulse Width	4.5		5.0		ns
t _w (L)	HIGH or LOW	4.5		5.0		
t _w (L)	\overline{SD}_n Pulse Width, LOW	4.5		5.0		ns
t _{rec}	\overline{SD}_n to \overline{CP}_n Recovery Time	4.0		5.0		ns



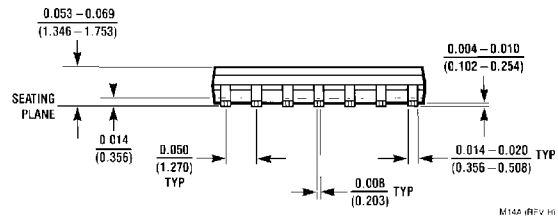
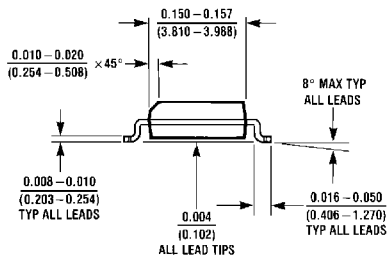
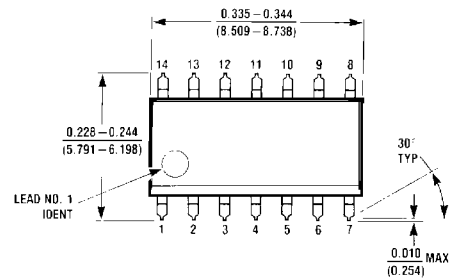
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



DS009473-7

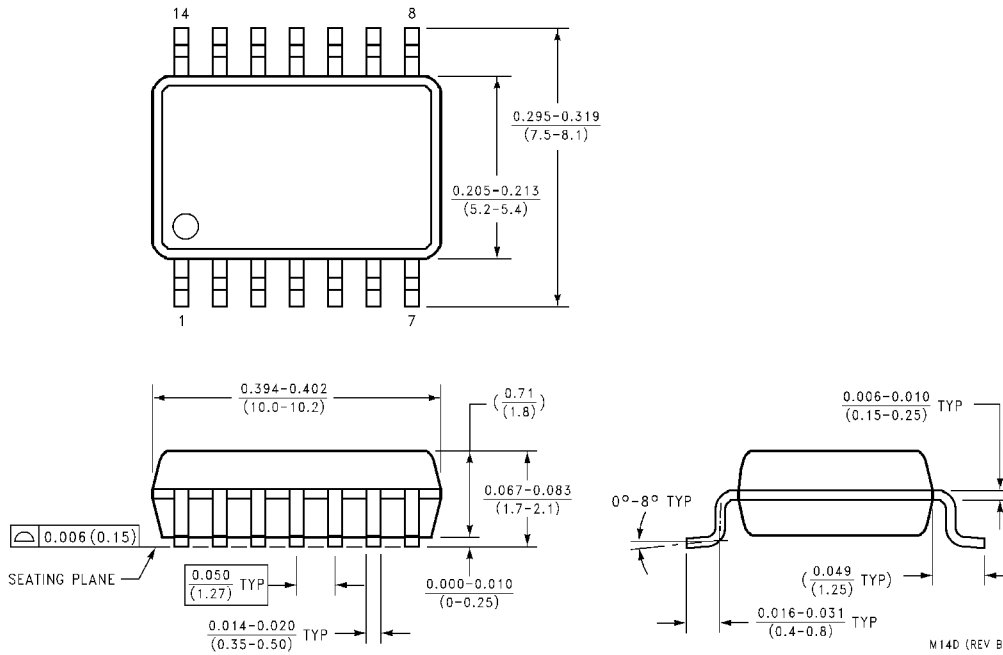
Physical Dimensions inches (millimeters) unless otherwise noted



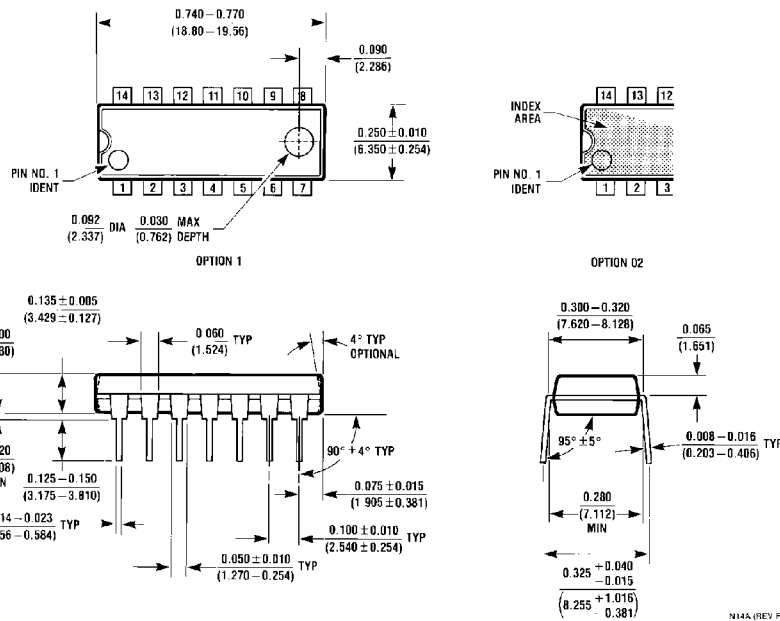
M14A (REV 16)

14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M14D**



**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N14A**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europa.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179