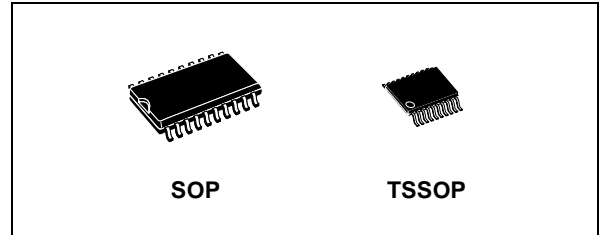


## LOW VOLTAGE CMOS OCTAL D-TYPE LATCH WITH 3 STATE OUTPUTS NON INVERTING

- HIGH SPEED:  
 $t_{PD} = 5.8 \text{ ns (TYP.) at } V_{CC} = 3.3 \text{ V}$
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- LOW NOISE:  
 $V_{OLP} = 0.5\text{V (TYP.) at } V_{CC} = 3.3\text{V}$
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 12\text{mA (MIN) at } V_{CC} = 3.0 \text{ V}$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 2\text{V to } 3.6\text{V (1.2V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 573
- IMPROVED LATCH-UP IMMUNITY



**Table 1: Order Codes**

PACKAGE	T & R
SOP	74LVQ573MTR
TSSOP	74LVQ573TTR

### DESCRIPTION

The 74LVQ573 is a low voltage CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and low noise 3.3V applications.

These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input (OE).

While the LE input is held at a high level, the Q outputs will follow the data input precisely. When the LE is taken low, the Q outputs will be latched precisely at the logic level of D input data. While the (OE) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state. In order to enhance PC board layout, the 74LVQ573 offers a pinout having inputs and outputs on opposite side of the package. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

**Figure 1: Pin Connection And IEC Logic Symbols**

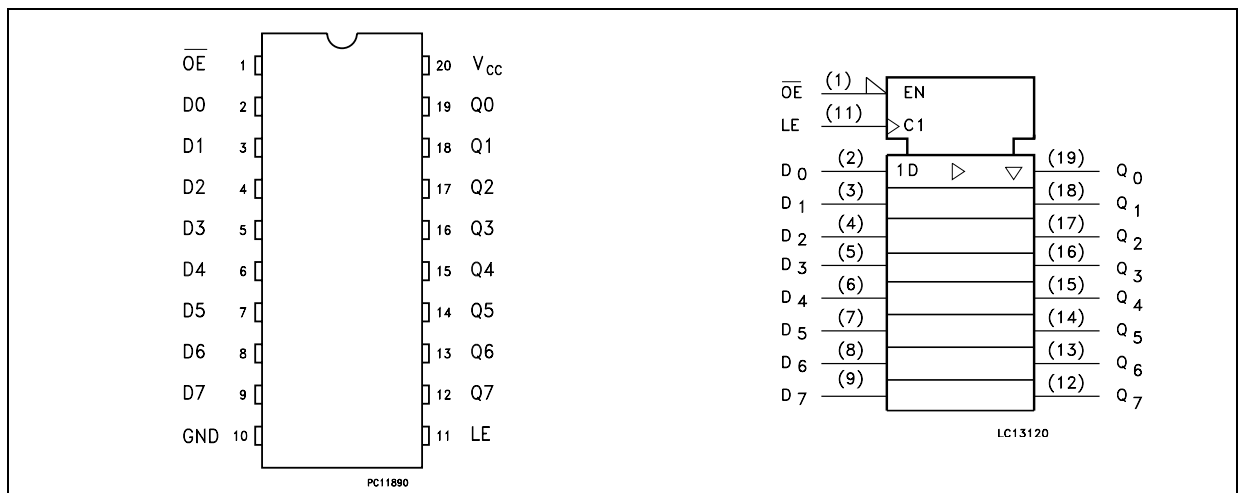


Figure 2: Input And Output Equivalent Circuit

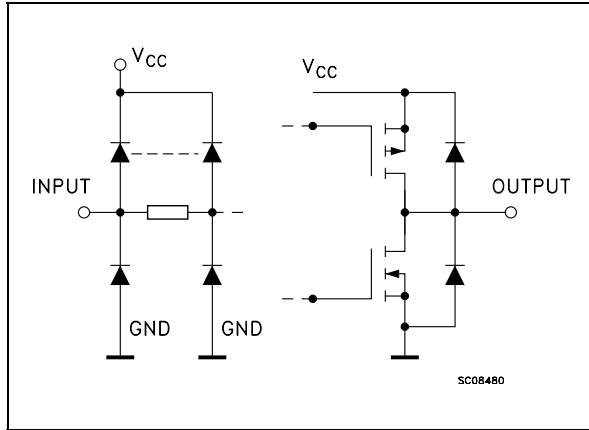


Table 2: Pin Description

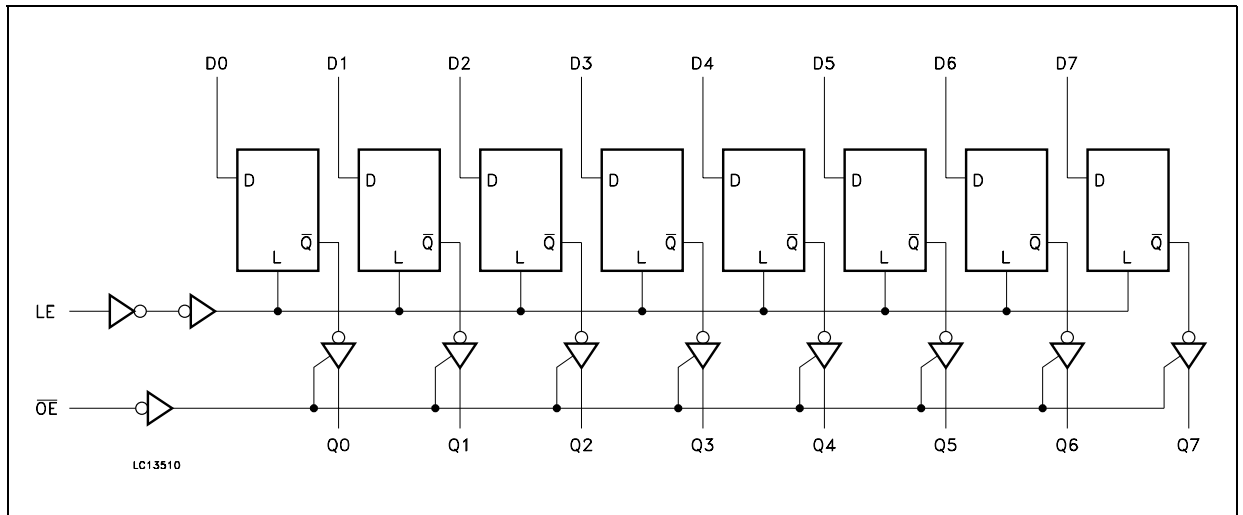
PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Latch Outputs
11	LE	Latch Enable Input
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE*
L	H	L	L
L	H	H	H

X : Don't Care  
 Z : High Impedance  
 \* : Q outputs are latched at the time when the LE input is taken low logic level

Figure 3: Logic Diagram



**Table 4: Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 400$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

**Table 5: Recommended Operating Conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (note 1)	2 to 3.6	V
$V_I$	Input Voltage	0 to $V_{CC}$	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0V$ (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2)  $V_{IN}$  from 0.8V to 2V

**Table 6: DC Specifications**

Symbol	Parameter	Test Condition		Value						Unit	
		$V_{CC}$ (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$V_{IH}$	High Level Input Voltage	3.0 to 3.6		2.0			2.0		2.0		V
$V_{IL}$	Low Level Input Voltage				0.8		0.8		0.8		V
$V_{OH}$	High Level Output Voltage	3.0	$I_O = -50 \mu\text{A}$	2.9	2.99		2.9		2.9		V
			$I_O = -12 \text{ mA}$	2.58			2.48		2.48		
			$I_O = -24 \text{ mA}$				2.2		2.2		
$V_{OL}$	Low Level Output Voltage	3.0	$I_O = 50 \mu\text{A}$		0.002	0.1		0.1		0.1	V
			$I_O = 12 \text{ mA}$		0	0.36		0.44		0.44	
			$I_O = 24 \text{ mA}$					0.55		0.55	
$I_I$	Input Leakage Current	3.6	$V_I = V_{CC}$ or GND			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	High Impedance Output Leakage Current	3.6	$V_I = V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND			$\pm 0.25$		$\pm 2.5$		$\pm 5.0$	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	3.6	$V_I = V_{CC}$ or GND			4		40		40	$\mu\text{A}$
$I_{OLD}$	Dynamic Output Current (note 1, 2)	3.6	$V_{OLD} = 0.8 \text{ V max}$				36		25		mA
$I_{OHD}$			$V_{OHD} = 2 \text{ V min}$				-25		-25		mA

1) Maximum test duration 2ms, one output loaded at a time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 75Ω

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C <sub>L</sub> = 50 pF		0.5	0.8					V
V <sub>OLV</sub>				-0.8	-0.6						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	3.3		2						V	
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					V

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

Table 8: AC Electrical Characteristics (C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω, Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time LE to Q	2.7			7.2	11.5		13.5		15.5	ns
		3.3(*)			5.8	9.0		10.5		12.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time D to Q	2.7			7.2	11.5		13.5		15.5	ns
		3.3(*)			5.8	9.0		10.5		12.0	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	2.7			8.7	14.0		16.0		18.5	ns
		3.3(*)			7.4	11.5		13.5		15.5	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.7			8.5	14.0		16.0		18.5	ns
		3.3(*)			7.5	11.5		13.5		15.5	
t <sub>W</sub>	LE Pulse Width HIGH	2.7			2.0	5.0		6.0		6.0	ns
		3.3(*)			1.5	4.0		4.0		4.0	
t <sub>sL</sub> t <sub>sH</sub>	Setup Time D to LE HIGH or LOW	2.7			0.0	4.0		4.5		4.5	ns
		3.3(*)			0.0	3.0		3.0		3.0	
t <sub>hL</sub> t <sub>hH</sub>	Hold Time D to LE, HIGH or LOW	2.7			0.0	1.5		1.5		1.5	ns
		3.3(*)			0.0	1.5		1.5		1.5	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output To Output Skew Time (note1, 2)	2.7			0.5	1.0		1.0		1.0	ns
		3.3(*)			0.5	1.0		1.0		1.0	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|)

2) Parameter guaranteed by design

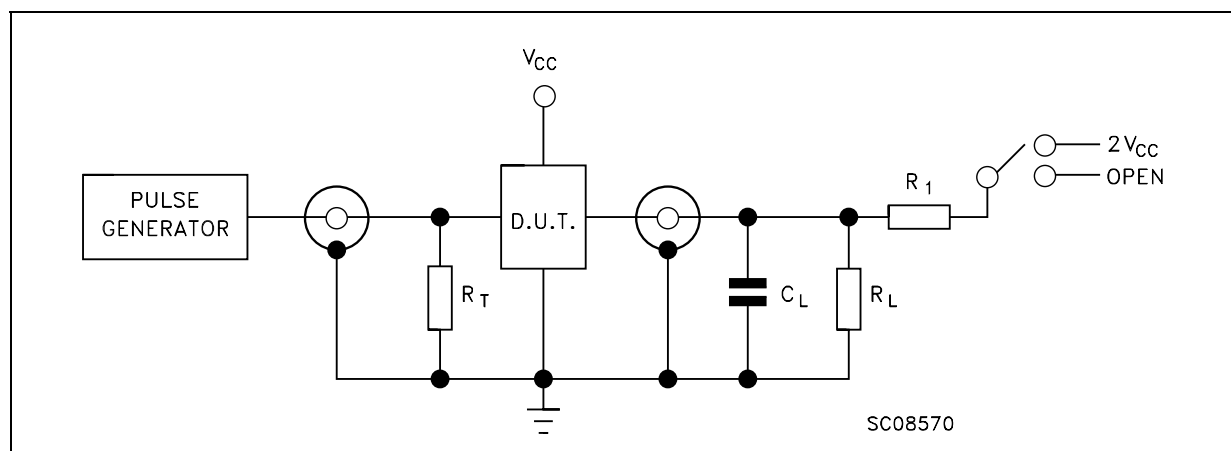
(\*) Voltage range is 3.3V ± 0.3V

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance	3.3			4						pF
C <sub>OUT</sub>	Output Capacitance	3.3			8						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3	f <sub>IN</sub> = 10MHz		10						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(oper)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC/n</sub> (per latch)

Figure 4: Test Circuit



TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	2V <sub>CC</sub>
t <sub>PZH</sub> , t <sub>PHZ</sub>	Open

C<sub>L</sub> = 50pF or equivalent (includes jig and probe capacitance)

R<sub>L</sub> = R<sub>1</sub> = 500Ω or equivalent

R<sub>T</sub> = Z<sub>OUT</sub> of pulse generator (typically 50Ω)

Figure 5: Waveform - LE To Qn Propagation Delays, LE Minimum Pulse Width, Dn To LE Setup And Hold Times (f=1MHz; 50% duty cycle)

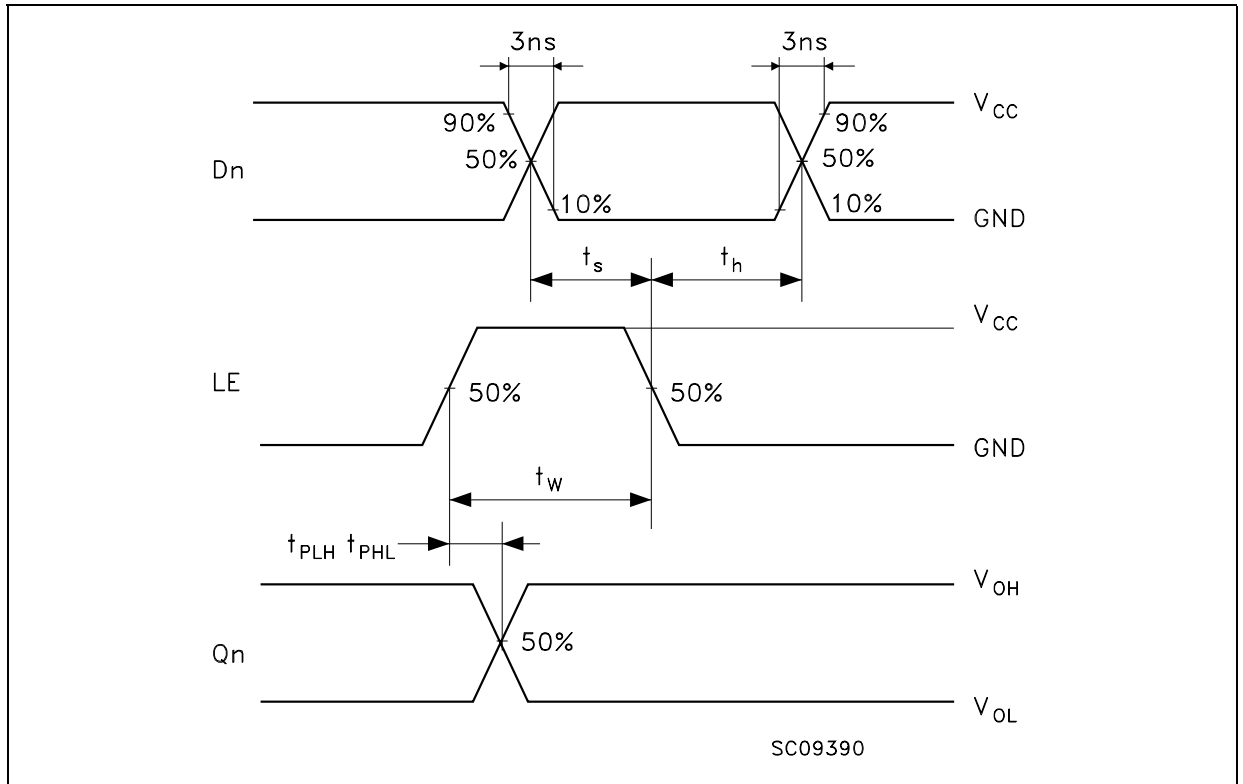


Figure 6: Waveform - Output Enable And Disable Times (f=1MHz; 50% duty cycle)

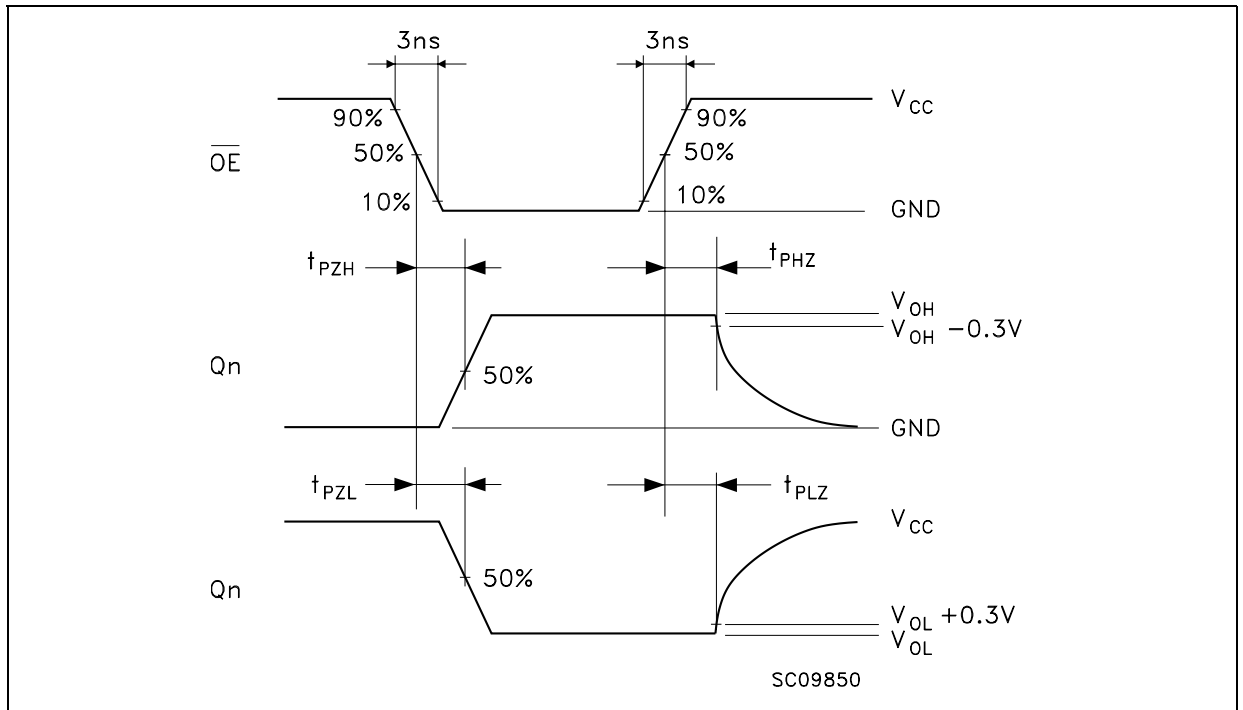
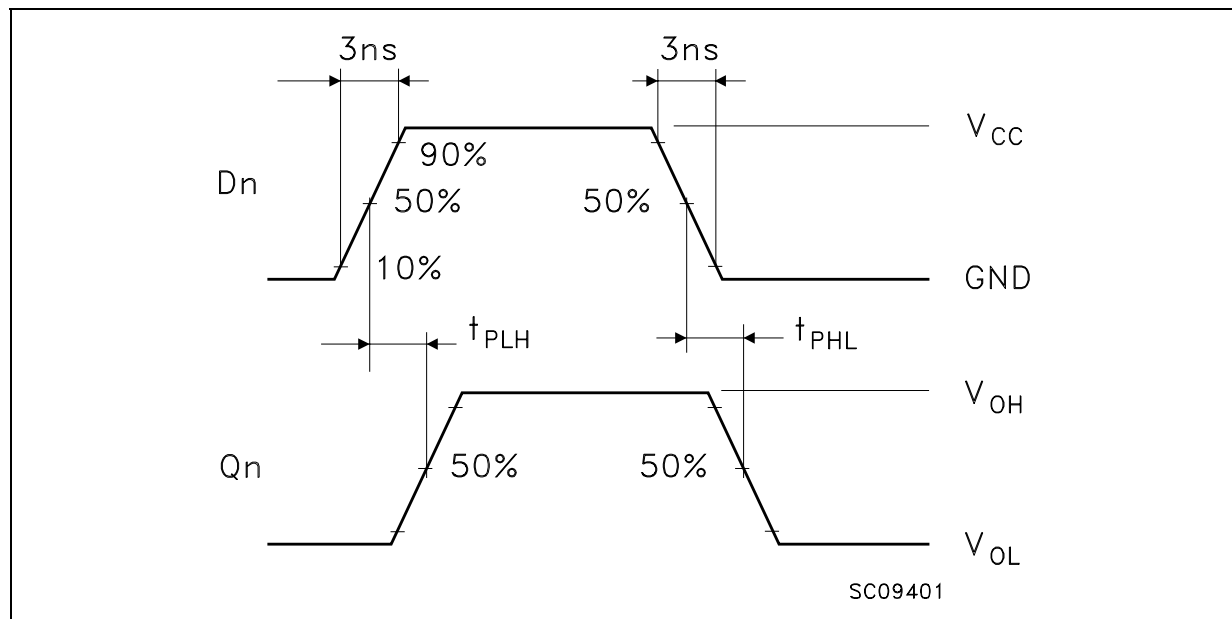
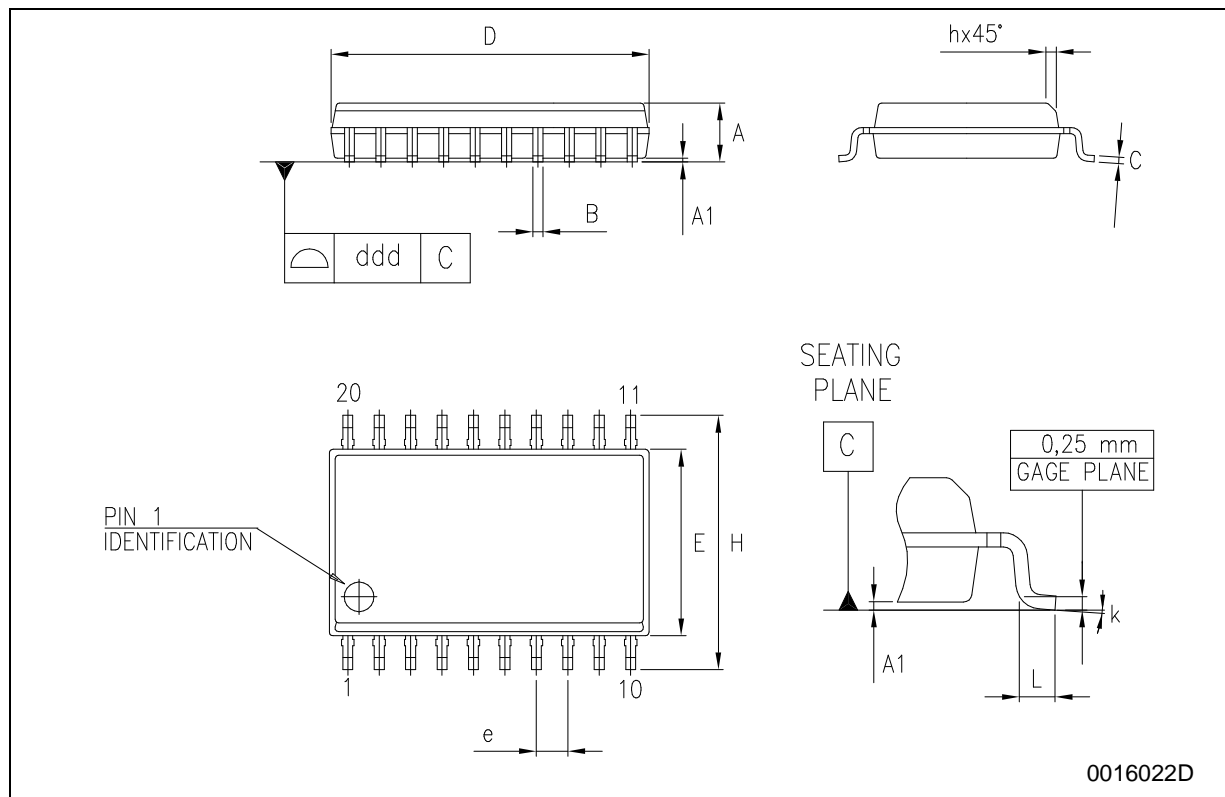


Figure 7: Waveform - Dn To Qn Propagation Delay Time (f=1MHz; 50% duty cycle)



## SO-20 MECHANICAL DATA

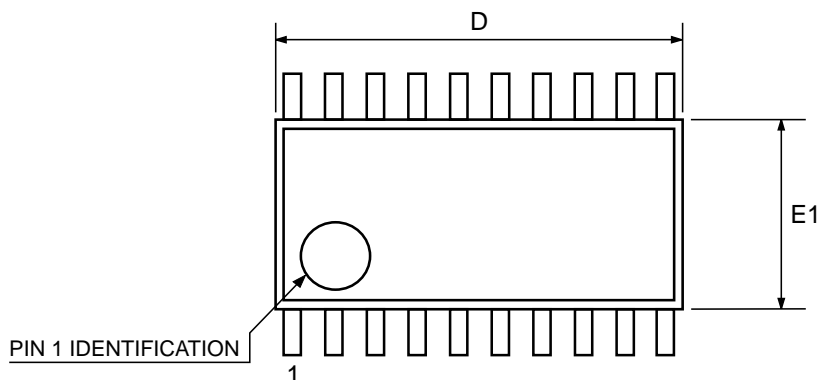
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004





## TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0087225C

## Tape &amp; Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



## Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



**Table 10: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
29-Jul-2004	5	Ordering Codes Revision - pag. 1.

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