

MCR8SDG, MCR8SMG, MCR8SNG

Sensitive Gate Silicon Controlled Rectifiers Reverse Blocking Thyristors

Designed primarily for half-wave ac control applications, such as motor controls, heating controls, and power supplies; or wherever half-wave, silicon gate-controlled devices are needed.

Features

- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- Blocking Voltage to 800 V
- On-State Current Rating of 8 A RMS at 80°C
- High Surge Current Capability – 80 A
- Rugged, Economical TO-220AB Package
- Glass Passivated Junctions for Reliability and Uniformity
- Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- Immunity to dv/dt – 5 V/ μ sec Minimum at 110°C
- These are Pb-Free Devices*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) ($T_J = -40$ to 110°C , Sine Wave, 50 to 60 Hz)	V_{DRM} , V_{RRM}	400 600 800	V
On-State RMS Current (180° Conduction Angles; $T_C = 80^\circ\text{C}$)	$I_{T(RMS)}$	8.0	A
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 110^\circ\text{C}$)	I_{TSM}	80	A
Circuit Fusing Consideration ($t = 8.33$ ms)	I^2t	26.5	A ² sec
Forward Peak Gate Power (Pulse Width ≤ 10 μ s, $T_C = 80^\circ\text{C}$)	P_{GM}	5.0	W
Forward Average Gate Power ($t = 8.3$ ms, $T_C = 80^\circ\text{C}$)	$P_{G(AV)}$	0.5	W
Forward Peak Gate Current (Pulse Width ≤ 10 μ s, $T_C = 80^\circ\text{C}$)	I_{GM}	2.0	A
Operating Junction Temperature Range	T_J	-40 to 110	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-40 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

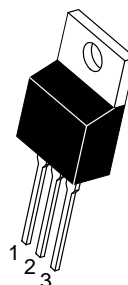
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

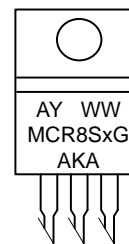
www.onsemi.com

SCRs
8 AMPERES RMS
400 thru 800 VOLTS



TO-220AB
CASE 221A-09
STYLE 3

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- x = D, M, or N
- G = Pb-Free Package
- AKA = Diode Polarity

PIN ASSIGNMENT

Pin	Assignment
1	Cathode
2	Anode
3	Gate
4	Anode

ORDERING INFORMATION

Device	Package	Shipping
MCR8SDG	TO-220AB (Pb-Free)	50 Units / Rail
MCR8SMG	TO-220AB (Pb-Free)	50 Units / Rail
MCR8SNG	TO-220AB (Pb-Free)	50 Units / Rail

MCR8SDG, MCR8SMG, MCR8SNG

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.2	$^{\circ}C/W$
Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current (Note 3) ($V_D = \text{Rated } V_{DRM} \text{ and } V_{RRM}; R_{GK} = 1 \text{ k}\Omega$)	I_{DRM} , I_{RRM}	-	-	10	μA
		-	-	500	

ON CHARACTERISTICS

Peak Forward On-State Voltage (Note 2) ($I_{TM} = 16 \text{ A}$)	V_{TM}	-	-	1.8	V
Gate Trigger Current (Continuous dc) (Note 4) ($V_D = 12 \text{ V}; R_L = 100 \Omega$)	I_{GT}	5.0	25	200	μA
Holding Current (Note 3) ($V_D = 12 \text{ V}$, Gate Open, Initiating Current = 200 mA)	I_H	-	0.5	6.0	mA
Latch Current (Note 4) ($V_D = 12 \text{ V}, I_G = 200 \mu A$)	I_L	-	0.6	8.0	mA
Gate Trigger Voltage (Continuous dc) (Note 4) ($V_D = 12 \text{ V}; R_L = 100 \Omega$)	V_{GT}	0.3	0.65	1.0	V
		-	-	1.5	
Gate Non-Trigger Voltage ($V_D = 12 \text{ V}, R_L = 100 \Omega$)	V_{GD}	0.2	-	-	V

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_D = 67\% V_{DRM}, R_{GK} = 1 \text{ K}\Omega, C_{GK} = 0.1 \mu F, T_J = 110^{\circ}C$)	dv/dt	5.0	15	-	$V/\mu s$
Critical Rate of Rise of On-State Current $IPK = 50 \text{ A}, Pw = 40 \mu sec, diG/dt = 1 \text{ A}/\mu sec, Igt = 10 \text{ mA}$	di/dt	-	-	100	$A/\mu s$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Indicates Pulse Test: Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2\%$.
- $R_{GK} = 1000 \text{ Ohms}$ included in measurement.
- Does not include R_{GK} in measurement.

MCR8SDG, MCR8SMG, MCR8SNG

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On State Voltage
I_H	Holding Current

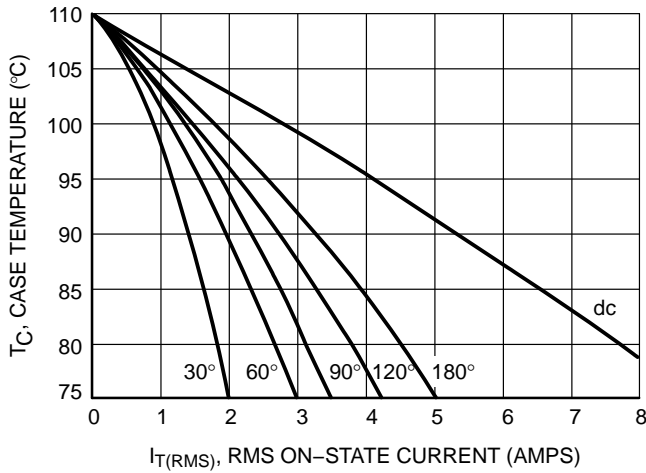
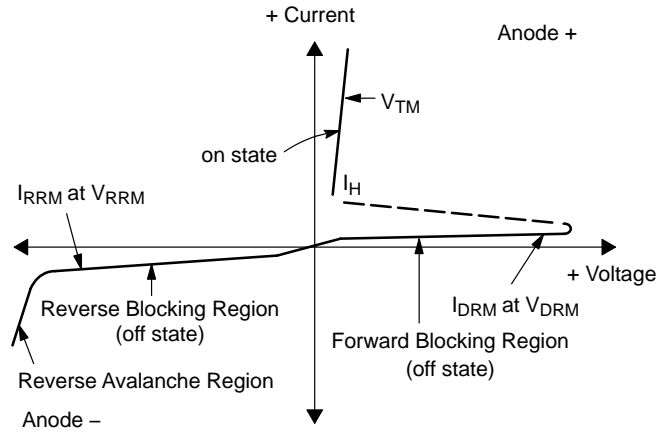


Figure 1. Typical RMS Current Derating

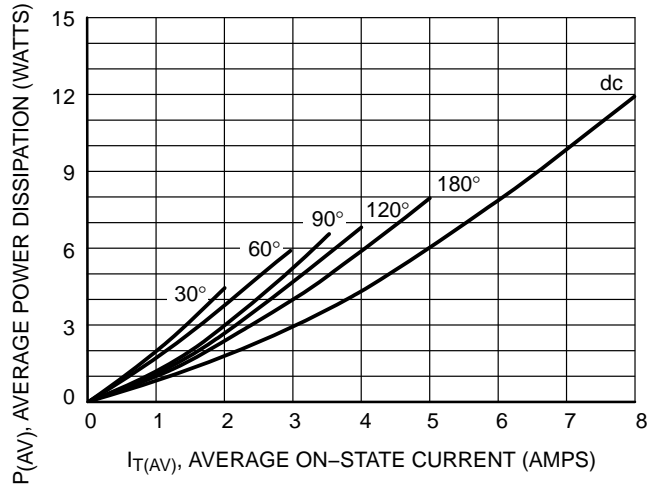


Figure 2. On-State Power Dissipation

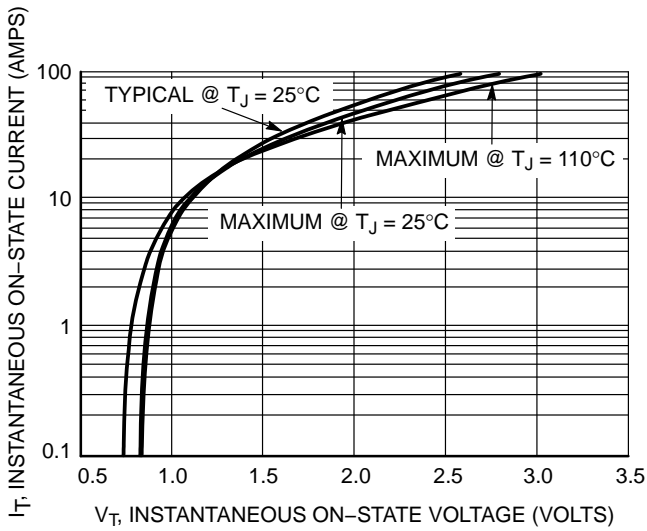


Figure 3. Typical On-State Characteristics

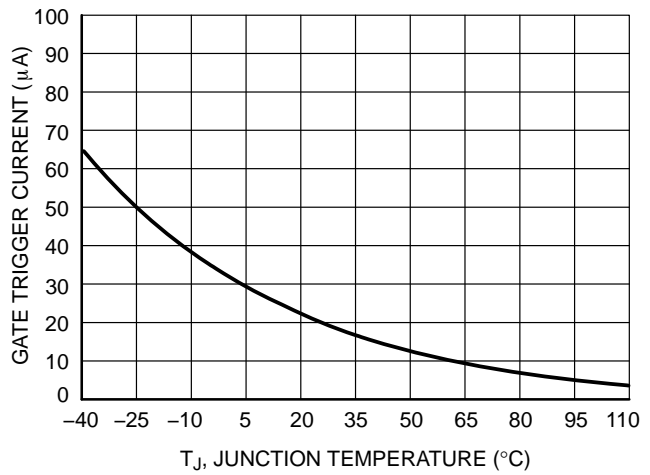


Figure 4. Typical Gate Trigger Current versus Junction Temperature

MCR8SDG, MCR8SMG, MCR8SNG

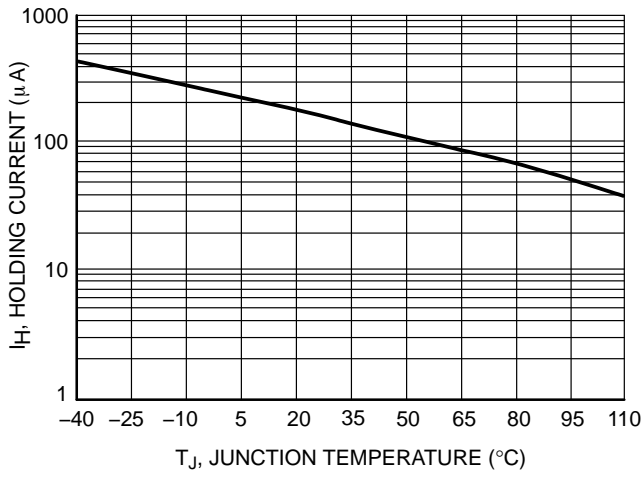


Figure 5. Typical Holding Current versus Junction Temperature

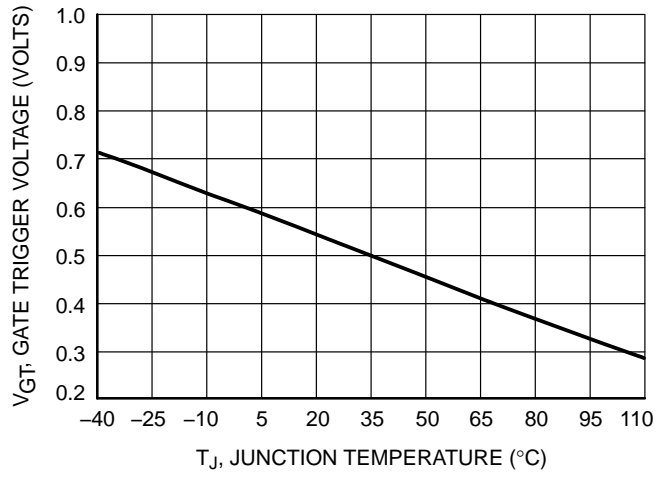


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

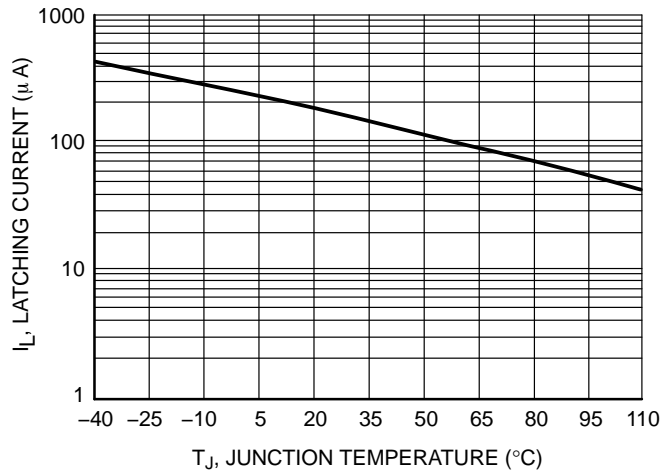
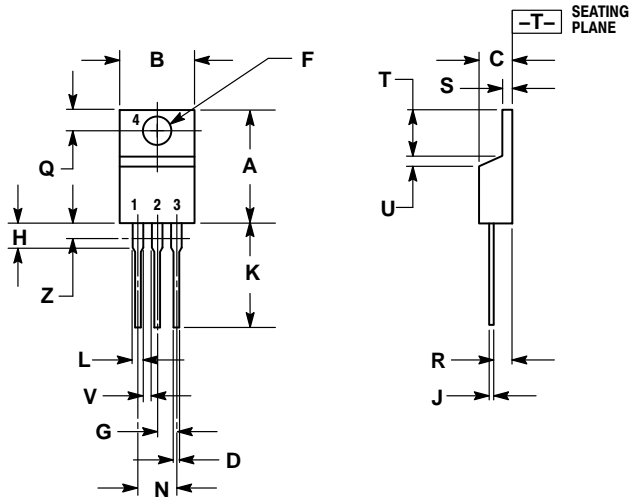


Figure 7. Typical Latching Current versus Junction Temperature

MCR8SDG, MCR8SMG, MCR8SNG

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AH




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 3:

- PIN 1: CATHODE
2. ANODE
3. GATE
4. ANODE

ON Semiconductor and the  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative