General Description

The MAX7328/MAX7329 are 2-wire serial-interfaced peripherals with eight I/O ports. Any port can be used as a logic input or an open-drain output.

All input ports are continuously monitored for state changes (transition detection). Transitions are alerted through the open-drain, 5.5V-tolerant $\overline{INT}$ output.

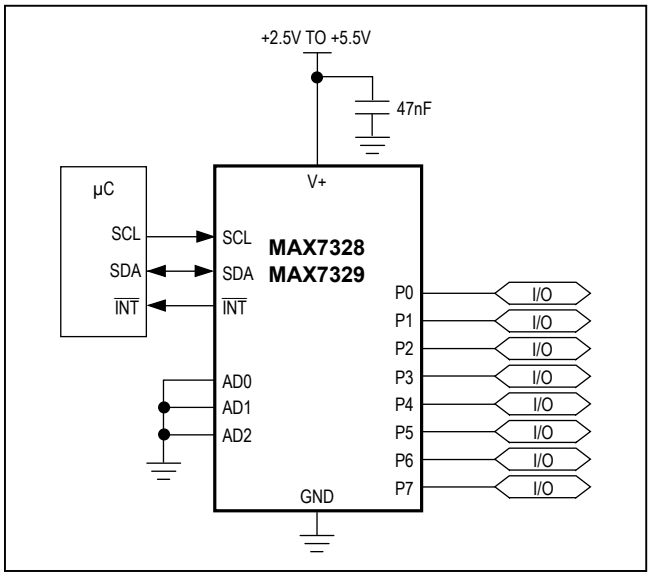
The MAX7328 and MAX7329 versions differ only by their slave ID address ranges. The MAX7328 has a slave ID range of 0100xxx (0x20 to 0x27). The MAX7329 has a slave ID range of 0111xxx (0x38 to 0x3F).

For a similar part with overvoltage-protected I/Os and a bus $\overline{RST}$ input that clears the I²C serial interface, refer to the MAX7321 data sheet. The MAX7328/MAX7329 are members of a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see the *Selector Guide*).

Applications

- RAID
- Servers
- Notebooks
- Industrial

Typical Application Circuit



Features

- 100kHz, 5.5V-Tolerant, I²C-Compatible Serial Interface
- 2.5V to 5.5V Operating Supply Voltage Range
- Low-Standby-Current Consumption of 10µA (max)
- I²C Bus-to-Parallel-Port Expander
- Open-Drain Interrupt Output $\overline{INT}$
- 8-Bit Remote I/O Port for the I²C Bus
- Latched Outputs with High-Current-Drive Capability for Directly Driving LEDs
- Address by Three Hardware Address Pins for Use of Up to Eight Devices (Up to 16 Using Both MAX7328/MAX7329)
- Second Sources to PCF8574 and PCF8574A

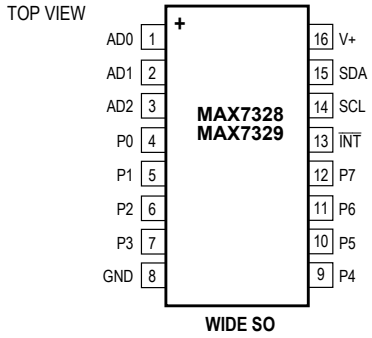
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7328AWE	-40°C to +125°C	16 Wide SO
MAX7328AAP	-40°C to +125°C	20 SSOP
MAX7328AUP*	-40°C to +125°C	20 TSSOP
MAX7329AWE	-40°C to +125°C	16 Wide SO
MAX7329AAP	-40°C to +125°C	20 SSOP
MAX7329AUP*	-40°C to +125°C	20 TSSOP

**Future product—contact factory for availability.*

Devices are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering.

Pin Configurations



WIDE SO

Pin Configurations continued at end of data sheet.

maxim integrated™

Absolute Maximum Ratings

(Voltage with respect to GND.)
V+, SCL, SDA, AD0, AD1, AD2, $\overline{INT}$ .....-0.3V to +6V
P0–P7 .....-0.3V to (V+ + 0.3V)
P0–P7, SDA, $\overline{INT}$ Output Sink Current 25mA
SCL, SDA, AD0, AD1, AD2, $\overline{INT}$, P0–P7 Input Current 20mA
Total V+ Current.....100mA
Total GND Current 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Wide SO (derate 9.5mW/°C over +70°C).....762mW
20-Pin SSOP (derate 8mW/°C over +70°C).....640mW
20-Pin TSSOP (derate 11mW/°C over +70°C).....879mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		2.5		5.5	V
Supply Current (Interface Running)	I+	f_{SCL} = 100kHz, other digital inputs at V+ or GND		40	100	µA
Standby Current (Interface Idle)	I+	SCL, SDA, and other digital inputs at V+ or GND		1	10	µA
Power-On Reset Voltage	V_{POR}			1.3	2.4	V
Input Low Voltage SDA, SCL, AD0, AD1, AD2, P0–P7	V_{IL}				0.3 x V+	V
Input High Voltage SDA, SCL, AD0, AD1, AD2, P0–P7	V_{IH}		0.7 x V+			V
Maximum Allowed Input Current through Protection Diode P0–P7	I_{PPROT}				±400	µA
Output Low Current SDA	I_{OLSDA}	V_{SDA} = 0.4V	3			mA
Input Leakage Current SDA, SCL, AD0, AD1, AD2, P0–P7	I_{IH}, I_{IL}	Pin at V+ or GND	-0.25		+0.25	µA
Input Capacitance SDA, SCL, AD0, AD1, AD2	C_{I2C}	Pin at GND (Note 2)			7	pF
Port Output-Low Output Current P0–P7	I_{OL}	V_{OL} = 1V, V+ = 5V	10	25		mA
Ports Output-High Output Current P0–P7	I_{OH}	V_{OH} = GND	30		300	µA
Output-High Transient Pullup Current P0–P7	I_{OHt}	Sources during acknowledge, V_{OH} = GND, V+ = 2.5V		1		mA
Input Capacitance P0–P7	C_P	(Note 2)			10	pF
Interrupt Output-Low Current $\overline{INT}$	I_{OLINT}	V_{OLINT} = 0.4V	1.6			mA

Port And Interrupt $\overline{INT}$ Timing Characteristics

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t_{PPV}	$C_L \le 100pF$			4	µs
Port Input Setup Time	t_{PSU}	$C_L \le 100pF$	0			µs
Port Input Hold Time	t_{PH}	$C_L \le 100pF$	4			µs
$\overline{INT}$ Input Data Valid Time	t_{IV}	$C_L \le 100pF$			4	µs
$\overline{INT}$ Reset Delay Time from Acknowledge	t_{IR}	$C_L \le 100pF$			4	µs

Timing Characteristics

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = 5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				100	kHz
Tolerable Spike Width on Bus	t_{SP}	(Note 2)			100	ns
Bus Free Time between STOP and START	t_{BUF}		4.7			µs
START or Repeated START Setup Time	$t_{SU, STA}$		4.7			µs
START or Repeated START Hold Time	$t_{HD, STA}$		4			µs
SCL Clock Low Period	t_{LOW}		4.7			µs
SCL Clock High Period	t_{HIGH}		4			µs
SDA and SCL Rise Time	t_R	(Note 2)			1	µs
SDA and SCL Fall Time	t_F	(Note 2)			300	ns
Data Setup Time	$t_{SU, DAT}$		250			ns
Data Hold Time	$t_{HD, DAT}$	(Note 3)			0.9	µs
SCL Low to Data-Out Valid	$t_{VD, DAT}$	SCL low to SDA output valid			3.4	µs
STOP Condition Setup Time	$t_{SU, STO}$		4			µs
Capacitive Load for Each Bus Line	C_b	(Note 2)			400	pF

Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Pin Description

PIN		NAME	FUNCTION
SO	SSOP/TSSOP		
1, 2, 3	6, 7, 9	AD0, AD1, AD2	Address Inputs. AD0, AD1, and AD2 set device slave address. Connect AD0, AD1, and AD2 to either GND or V+. See Tables 1 and 2.
4–7, 9–12	10, 11, 12, 14, 16, 17, 19, 20	P0–P7	Input/Output Ports. P0–P7 are open-drain I/Os.
8	15	GND	Ground
13	1	$\overline{INT}$	Interrupt Output. $\overline{INT}$ is an open-drain output rated at 5.5V.
14	2	SCL	I2C-Compatible Serial-Clock Input
15	4	SDA	I2C-Compatible Serial-Data I/O
16	5	V+	Positive Supply Voltage. Bypass V+ to GND with a 0.047µF ceramic capacitor.
—	3, 8, 13, 18	N.C.	No Connection. Internally not connected.

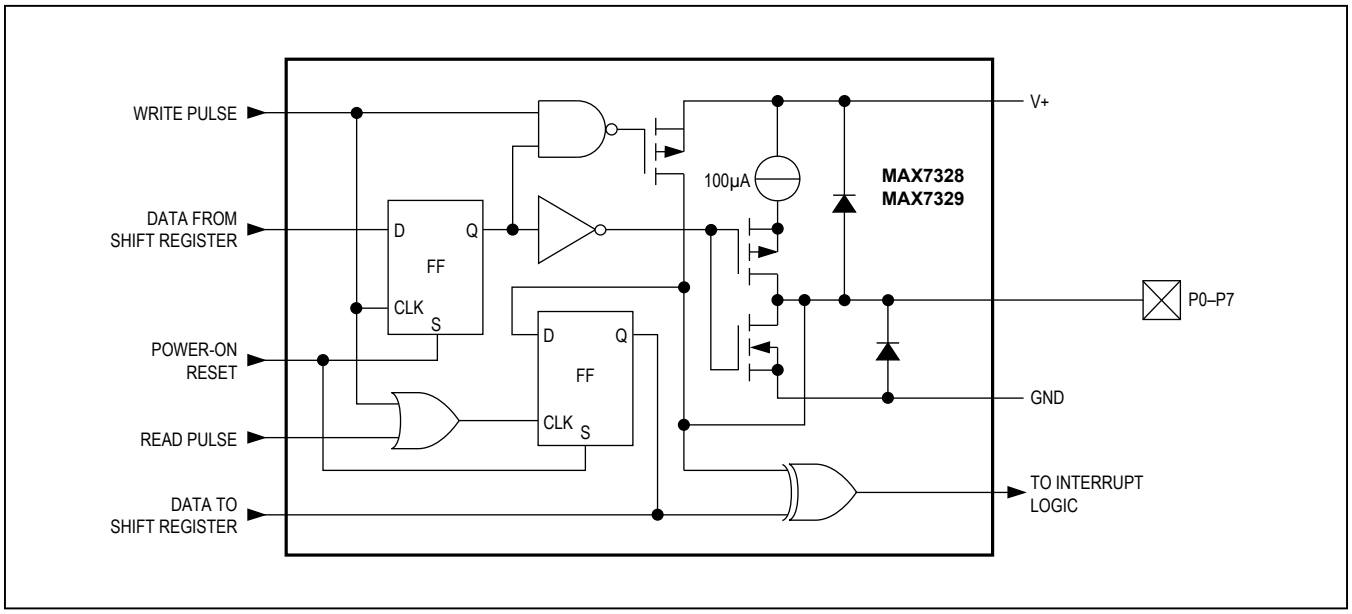


Figure 1. Block Diagram

Table 1. MAX7328 Slave ID Address Selection

PIN CONNECTION			DEVICE ADDRESS							PORTS POWER-UP DEFAULT							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0
GND	GND	GND	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1
GND	GND	V+	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1
GND	V+	GND	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1
GND	V+	V+	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
V+	GND	GND	0	1	0	0	1	0	0	1	1	1	1	1	1	1	1
V+	GND	V+	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1
V+	V+	GND	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1
V+	V+	V+	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1

Table 2. MAX7329 Slave ID Address Selection

PIN CONNECTION			DEVICE ADDRESS							PORTS POWER-UP DEFAULT							
AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0
GND	GND	GND	0	1	1	1	0	0	0	1	1	1	1	1	1	1	1
GND	GND	V+	0	1	1	1	0	0	1	1	1	1	1	1	1	1	1
GND	V+	GND	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1
GND	V+	V+	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1
V+	GND	GND	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1
V+	GND	V+	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1
V+	V+	GND	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1
V+	V+	V+	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Detailed Description

Functional Overview

The MAX7328/MAX7329 are general-purpose port expanders operating from a 2.5V to 5.5V supply that provide eight open-drain input/output ports with a 20mA sink capability. The devices are rated to sink up to 100mA at once, from any combination of ports. The port outputs can drive loads connected to any voltage up to the MAX7328/MAX7329's supply voltage.

The MAX7328 is set to one of eight I2C slave addresses 0x20 to 0x27, and the MAX7329 is set to one of eight I2C slave addresses, 0x38 to 0x3F, using the address inputs AD2, AD1, and AD0. The parts are accessed over an I2C serial interface up to 100kHz.

Any port can be configured as a logic input by setting the port output logic-high. The MAX7328/MAX7329 do not distinguish between a port used as an input and a port used as an output that happens to be high. When a MAX7328 or MAX7329 is read through the serial interface, the actual logic levels at the port pins are read back.

When an I/O port is high, an internal pullup to V+ is active. The pullup is enabled only when the output is high, and is turned off when the output is low to reduce quiescent current. An additional strong pullup to V+ allows fast-rising edges into heavily loaded outputs. These strong pullups turn on when an output is written high, and are switched off by the falling edge of SCL (Figure 2).

The MAX7328/MAX7329 provide an open-drain output ($\overline{INT}$). An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{IV}, the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port that generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal

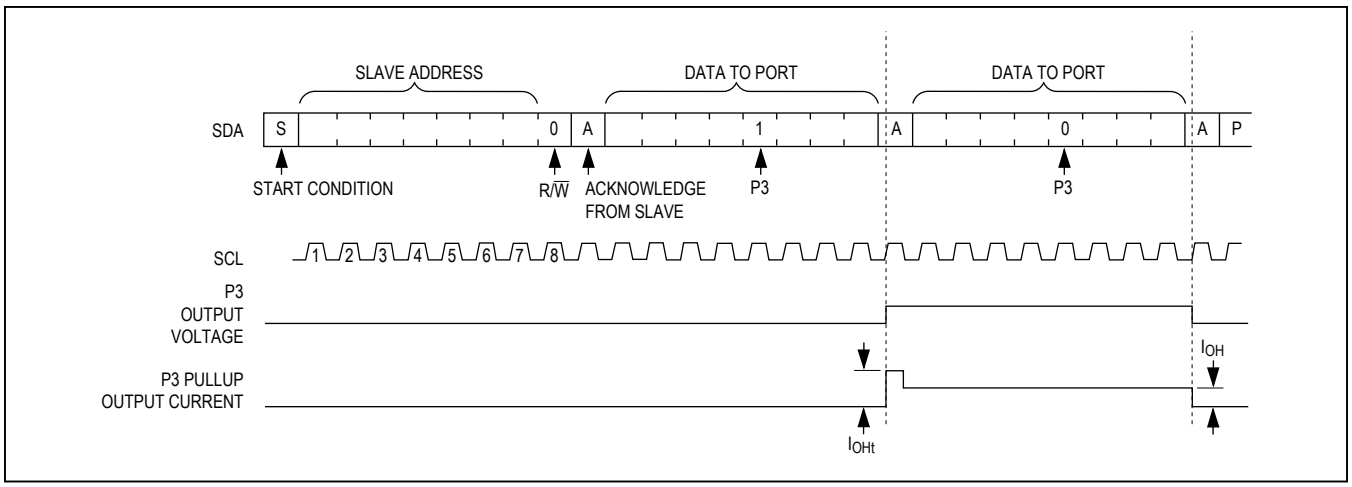


Figure 2. Repeated Write Operation Showing Transient Pullup Current

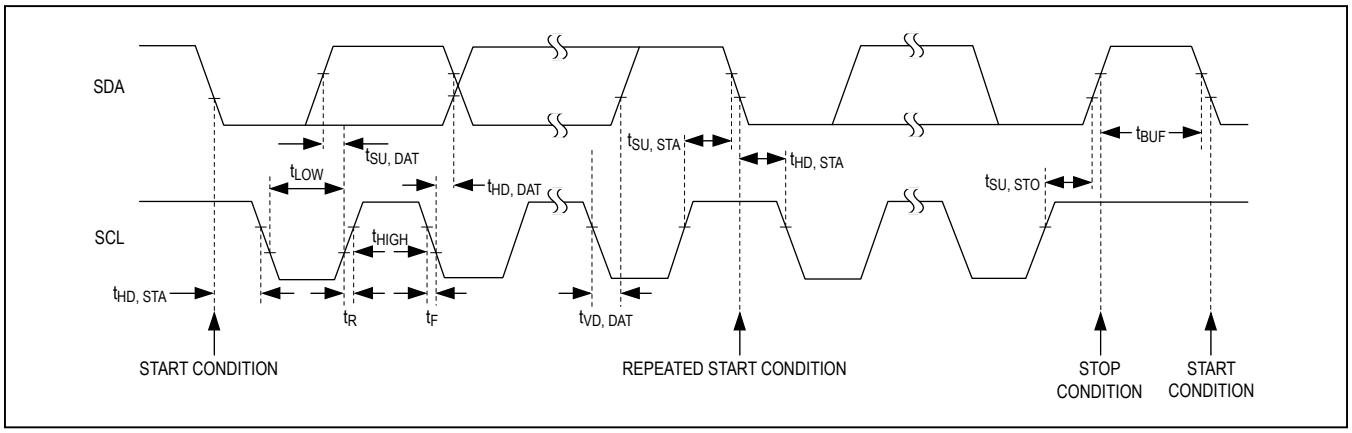


Figure 3. 2-Wire Serial-Interface Timing Details

Interrupts that occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as $\overline{INT}$.

MAX7328/MAX7329 Initial Power-Up

On power-up, the power-up default states of the eight I/O ports are high, and therefore, can be used as inputs or outputs. The interrupt output $\overline{INT}$ is reset, and $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted).

Serial Interface

Serial Addressing

The MAX7328/MAX7329 operate as slave devices that send and receive data through an I2C-compatible, 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master initiates all data transfers to and from the MAX7328 or MAX7329, and generates the SCL clock that synchronizes the data transfer (Figure 3).

The MAX7328 or MAX7329 SDA line operates as both an input and an open-drain output. A pullup resistor,

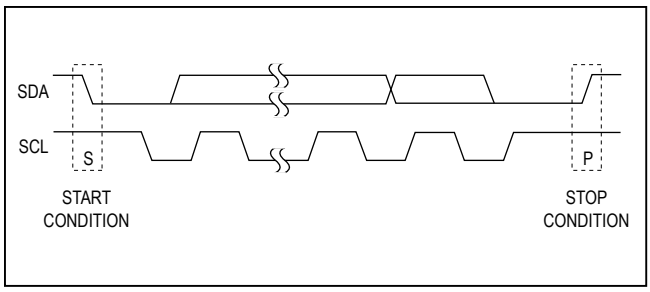


Figure 4. START and STOP Conditions

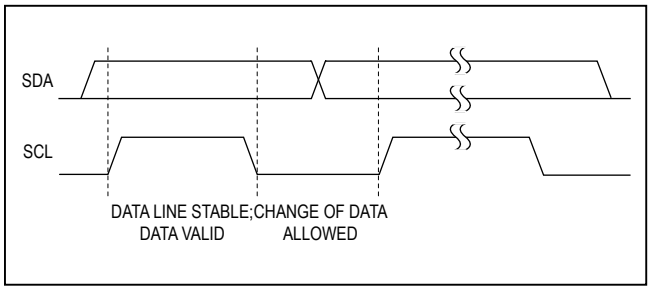


Figure 5. Bit Transfer

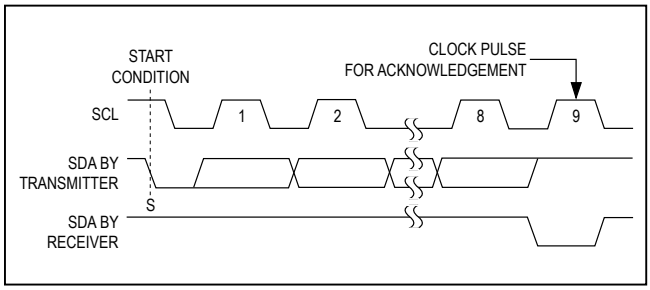


Figure 6. Acknowledge

typically 4.7kΩ, is required on SDA. The MAX7328 or MAX7329 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 4) sent by a master, followed by the MAX7328 or MAX7329 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 4).

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 4).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 5).

Acknowledge

The acknowledge bit is a clocked ninth bit, which the recipient uses to handshake receipt of each byte of data (Figure 6). Thus, each byte transferred effectively requires 9 bits. The master generates the ninth clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7328 or MAX7329, the MAX7328 or MAX7329 generates the acknowledge bit because the MAX7328 or MAX7329 is the recipient. When the MAX7328 or MAX7329 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX7328/MAX7329 have a 7-bit long slave address (Figure 7). The eighth bit, following the 7-bit slave address, is the R/$\overline{W}$ bit. It is low for a write command, high for a read command.

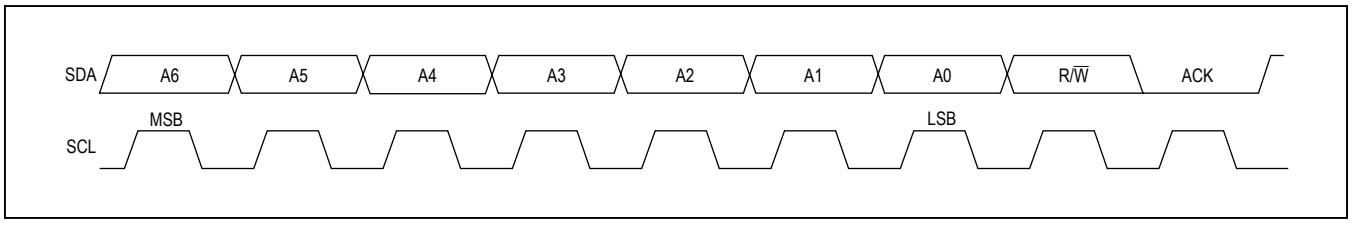


Figure 7. Slave Address

The first (A6), second (A5), third (A4), and fourth (A3) bits of the MAX7328 slave address are always 0, 1, 0, and 0. Slave address bits A2, A1, and A0 are selected by the address inputs AD2, AD1, and AD0. These pins can be connected to GND or V+. The MAX7328 has eight possible slave addresses (Table 1), and therefore, a maximum of eight MAX7328 devices can be controlled independently from the same interface.

The first (A6), second (A5), third (A4), and fourth (A3) bits of the MAX7329 slave address are always 0, 1, 1, and 1. Slave address bits A2, A1, and A0 are selected by the address inputs AD2, AD1, and AD0. These pins can be connected to GND or V+. The MAX7329 has eight possible slave addresses (Table 2), and therefore, a maximum of eight MAX7329 devices can be controlled independently from the same interface.

Because the MAX7328 has a different range of slave address selections than the MAX7329, a total of eight MAX7328 devices and eight MAX7329 devices can be connected to the same bus and independently controlled.

Reading and Writing the MAX7328 and MAX7329

I2C interface access to the MAX7328/MAX7329 is as follows:

A **single-byte read** from the MAX7328 or MAX7329 returns the status of the eight ports (with output ports read back as inputs), and clears the $\overline{INT}$ output.

A **2-byte read** from the MAX7328 or MAX7329 returns the status of the eight ports (with output ports read back as inputs) and clears the $\overline{INT}$ output.

A **multibyte read** repeatedly returns the input port data.

Input port data is sampled during the preceding I2C acknowledge bit, which is the acknowledge bit for the I2C slave address in the case of a single-byte or 2-byte read.

A **single-byte write** to the MAX7328 or MAX7329 sets the eight ports to high or low, depending on the data byte content. Bit locations of a write byte, corresponding to ports intended for input usage, contain high values.

A **multibyte write** to the MAX7328 or MAX7329 repeatedly sets the logic state of all eight I/O ports.

Reading from the MAX7328 and MAX7329

A read from the MAX7328 or MAX7329 starts with the master transmitting the MAX7328's or MAX7329's slave address with the R/$\overline{W}$ bit set high. The MAX7328 or MAX7329 acknowledges the slave address, and samples the input ports (takes a snapshot) during acknowledge.

Typically, the master reads 1 or 2 bytes from the MAX7328 or MAX7329, each byte being acknowledged by the master on reception, with exception of the last byte.

The master can read 1 byte from the MAX7328 or MAX7329 and then issue a STOP condition (Figure 8). In this case, the MAX7328 or MAX7329 transmits the current port data, and restarts the transition detection. $\overline{INT}$ goes high (high impedance if an external pullup resistor is not fitted) during the port data-byte acknowledge. The new snapshot data is the current port data transmitted to the master, and therefore, any port changes that occur during the transmission are detected. $\overline{INT}$ always remains high until a STOP condition.

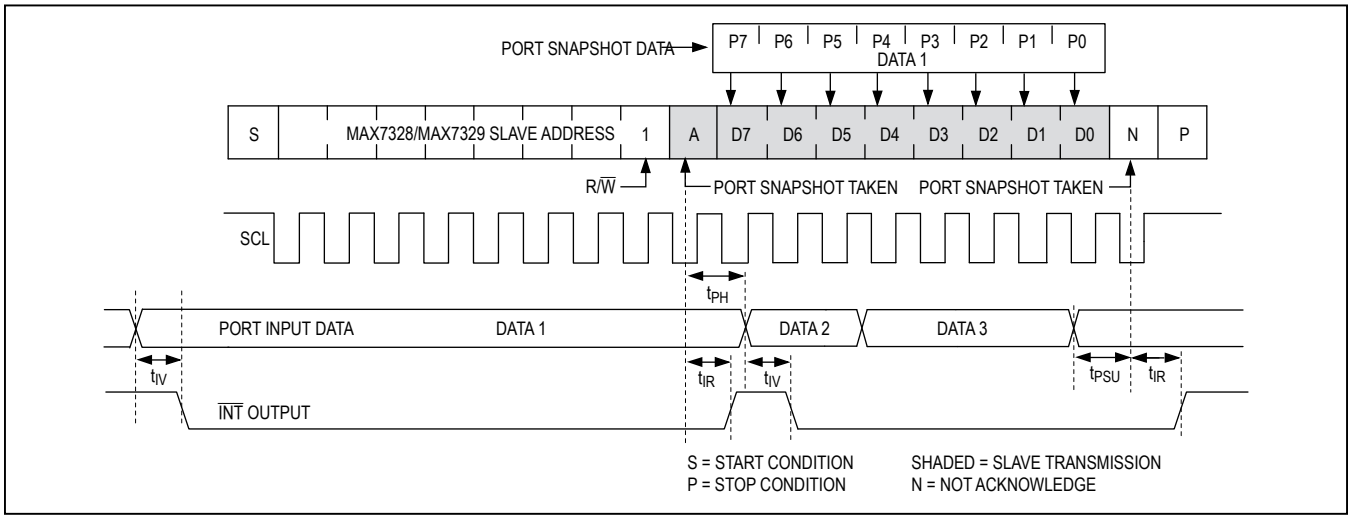


Figure 8. Reading from the MAX7328/MAX7329 (1 Data Byte)

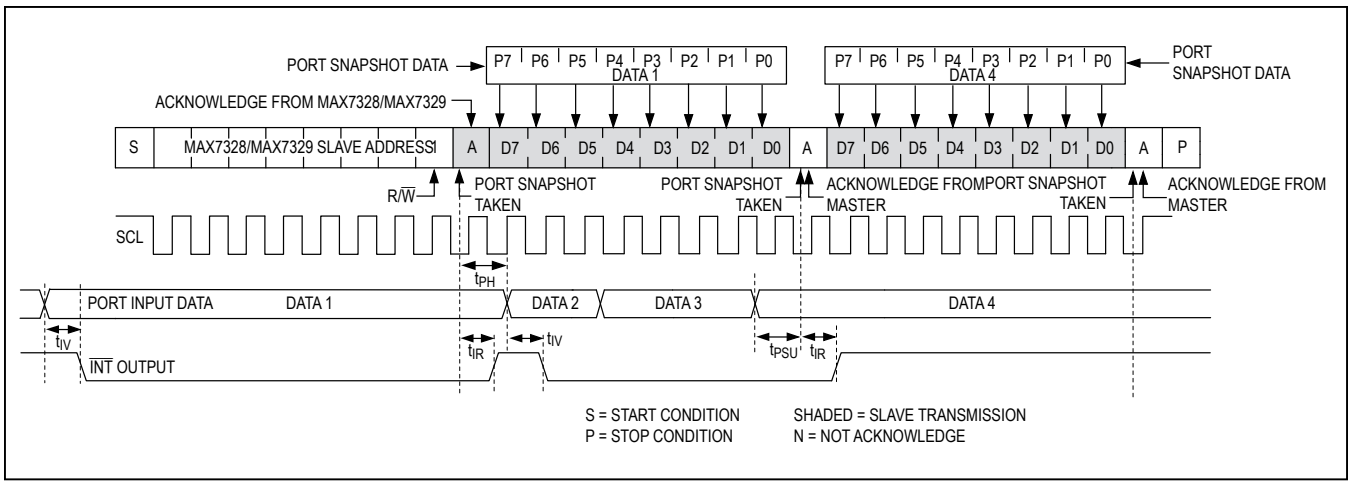


Figure 9. Reading from the MAX7328/MAX7329 (2 Data Bytes)

The master can read 2 bytes from the MAX7328 or MAX7329 and then issues the STOP condition (Figure 9). In this case, the MAX7328 or MAX7329 transmits the current port data repeatedly. $\overline{INT}$ goes high during the port data-byte acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, any port transitions that occur during the transmission are detected. $\overline{INT}$ remains high until the STOP condition.

Writing to the MAX7328/MAX7329

A data write to the MAX7328 or MAX7329 comprises the transmission of the MAX7328's or MAX7329's slave address with the R/$\overline{W}$ bit set to zero, followed by one or more bytes of data. The MAX7328 or MAX7329 acknowledges the slave address and any subsequent bytes of data until the master issues a STOP condition (Figure 10).

Applications Information

Hot Insertion

The MAX7328/MAX7329's SDA, SCL, AD0, AD1, AD2, $\overline{RST}$, and P0–P7 I/Os remain high impedance with up to +6V asserted on them when the MAX7328 or MAX7329 is powered down (V+ = 0V). The MAX7328/MAX7329 can therefore be used in hot-swap applications.

Each of the I/O ports P0–P7 has protection diodes to V+ and GND. When a port output is back driven to a voltage higher than V+ or lower than GND, the appropriate protection diode clamps the output to a diode drop above V+ or below GND. When a MAX7328 or MAX7329 is powered down (V+ = 0V), each output port's protection diodes to V+ and GND continue to appear as a diode clamp from each output to GND (Figure 1).

Power-Supply Considerations

The MAX7328/MAX7329 operate with a 2.5V to 5.5V power-supply voltage over the -40°C to +125°C temperature range. Bypass the power supply to GND with a ceramic capacitor of at least 0.047µF as close to the device as possible.

Chip Information

PROCESS: BiCMOS

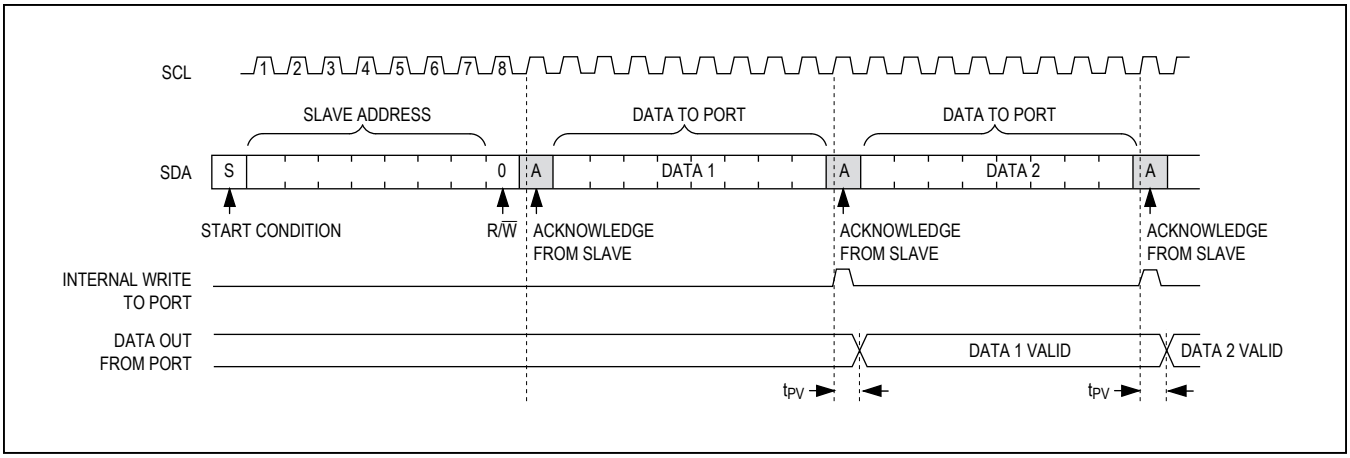
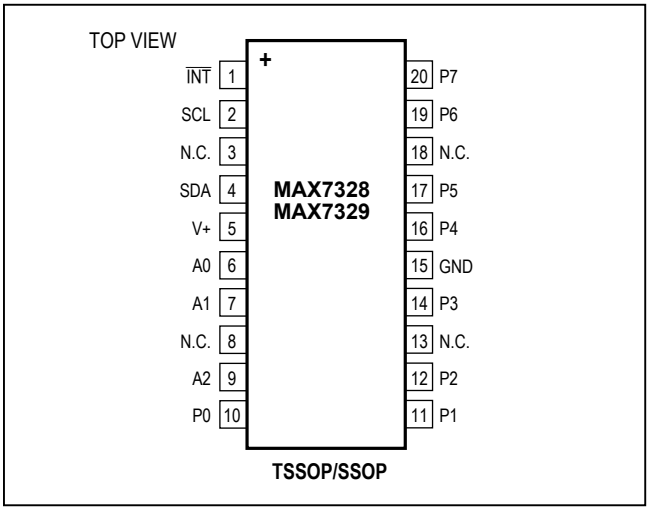


Figure 10. Writing to the MAX7328/MAX7329

Selector Guide

PART	I²C BUS RST	INPUTS	LATCHING INTERRUPT	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	SECOND SOURCE
MAX7319	Yes	8	Yes	—	—	—
MAX7320	Yes	—	Yes	—	8	—
MAX7321	Yes	Up to 8	Yes	Up to 8	—	—
MAX7322	Yes	4	Yes	—	4	—
MAX7323	Yes	Up to 4	Yes	Up to 4	4	—
MAX7328	—	Up to 8	—	Up to 8	—	PCF8574
MAX7329	—	Up to 8	—	Up to 8	—	PCF8574A

Pin Configurations (continued)



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SO	W16-1	21-0042	90-0107
20 SSOP	A20-5	21-0056	90-0094
20 TSSOP	—	21-0066	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/05	Initial release	—
1	5/14	Updated *Applications*	1

