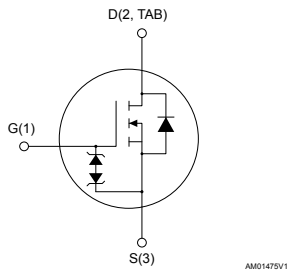
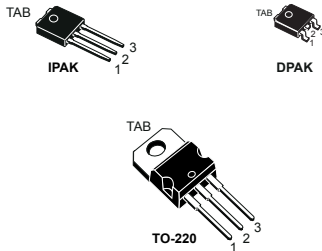


N-channel 900 V, 5 Ω typ., 2.1 A SuperMESH™ Power MOSFETs in IPAK, DPAK and TO-220 packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STD2NK90Z-1	900 V	6.5 Ω	2.1 A	IPAK
STD2NK90ZT4				DPAK
STP2NK90Z				TO-220

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STD2NK90Z-1](#)
[STD2NK90ZT4](#)
[STP2NK90Z](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	900	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.1	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	8.4	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 k Ω)	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_j	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 2.1\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	IPAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	1.78			$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50			
$R_{thj-amb}$	Thermal resistance junction-ambient		100	62.5	

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AS}^{(1)}$	Single-pulse avalanche current	2.1	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	150	mJ

1. Pulse width limited by T_{jmax} .
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	900			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 900\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 900\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.05\text{ A}$		5	6.5	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	485		μF
C_{oss}	Output capacitance			50		
C_{rSS}	Reverse transfer capacitance			10		
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 720\text{ V}$	-	24		μF
Q_g	Total gate charge	$V_{DD} = 720\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	19.5	27	nC
Q_{gs}	Gate-source charge			3.4		
Q_{gd}	Gate-drain charge			10.8		

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	21	-	ns
t_r	Rise time			11		
$t_{d(off)}$	Turn-off delay time			43		
t_f	Fall time			40		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8.4	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.1 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	415		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 50 \text{ V}$	-	1.5		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	515		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 50 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	1.9		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.5		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.
2. Pulse width is limited by safe operating area.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

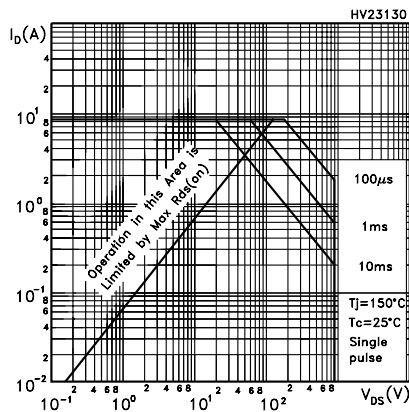
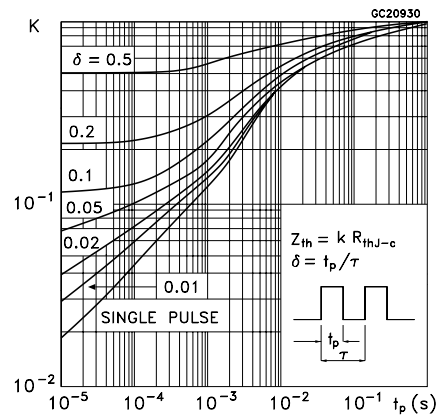
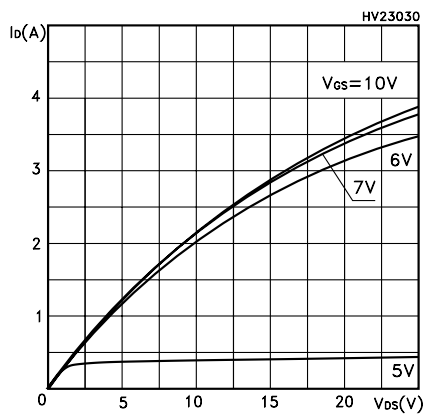
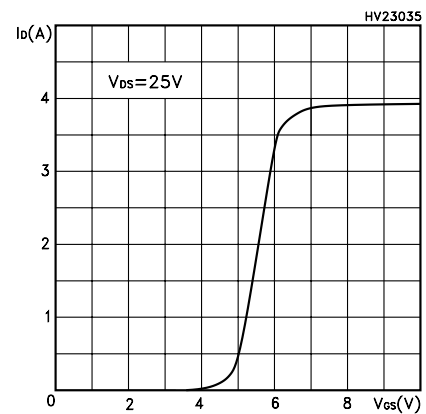
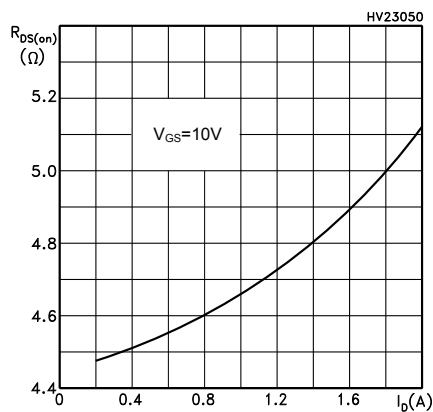
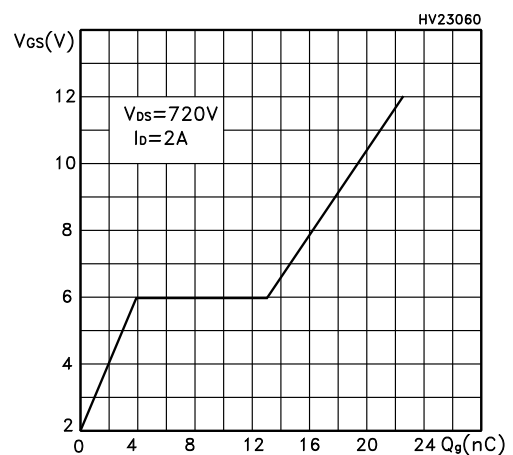
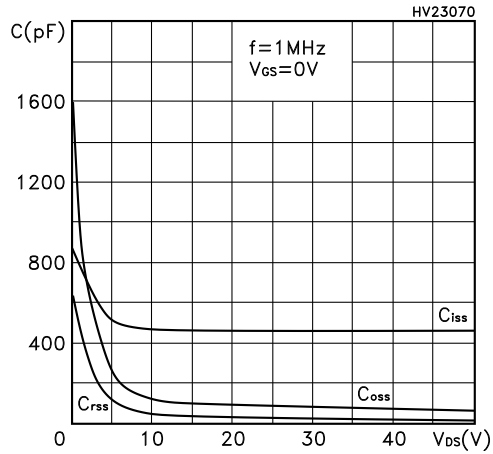
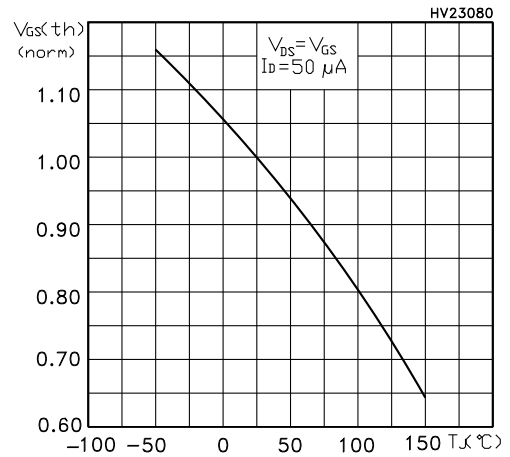
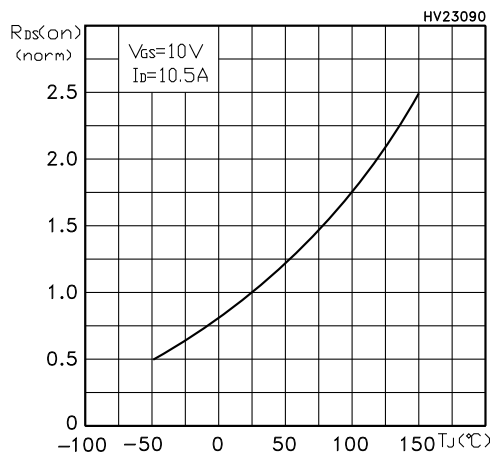
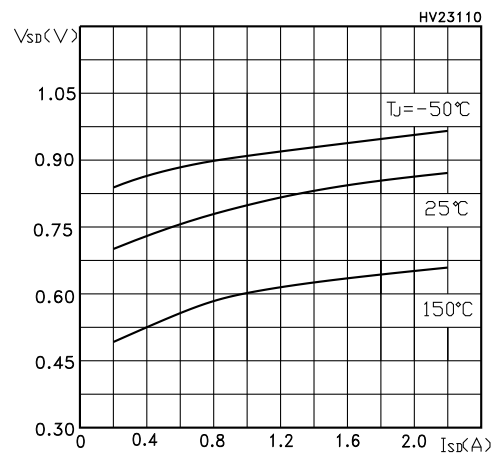
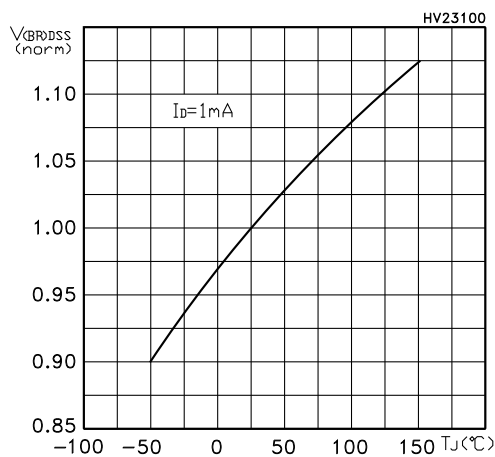
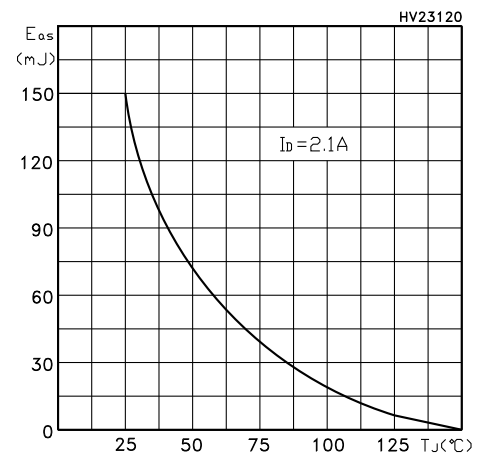
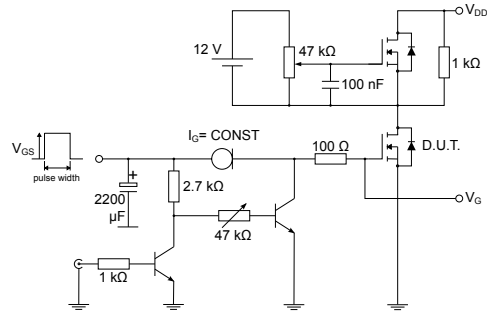
2.1 Electrical characteristics (curves)
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Static drain-source on resistance

Figure 6. Gate charge vs gate-source voltage


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on resistance vs temperature

Figure 10. Source-drain diode forward characteristics

Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

Figure 12. Maximum avalanche energy vs temperature


3 Test circuits

Figure 13. Test circuit for resistive load switching times


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Figure 14. Test circuit for gate charge behavior


AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times

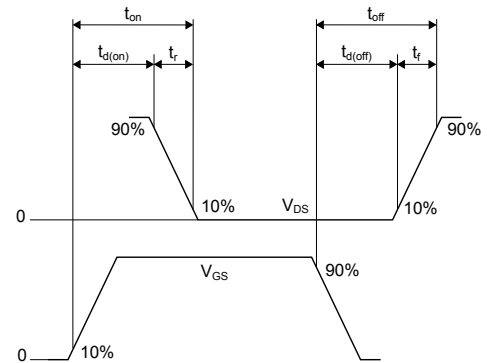

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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


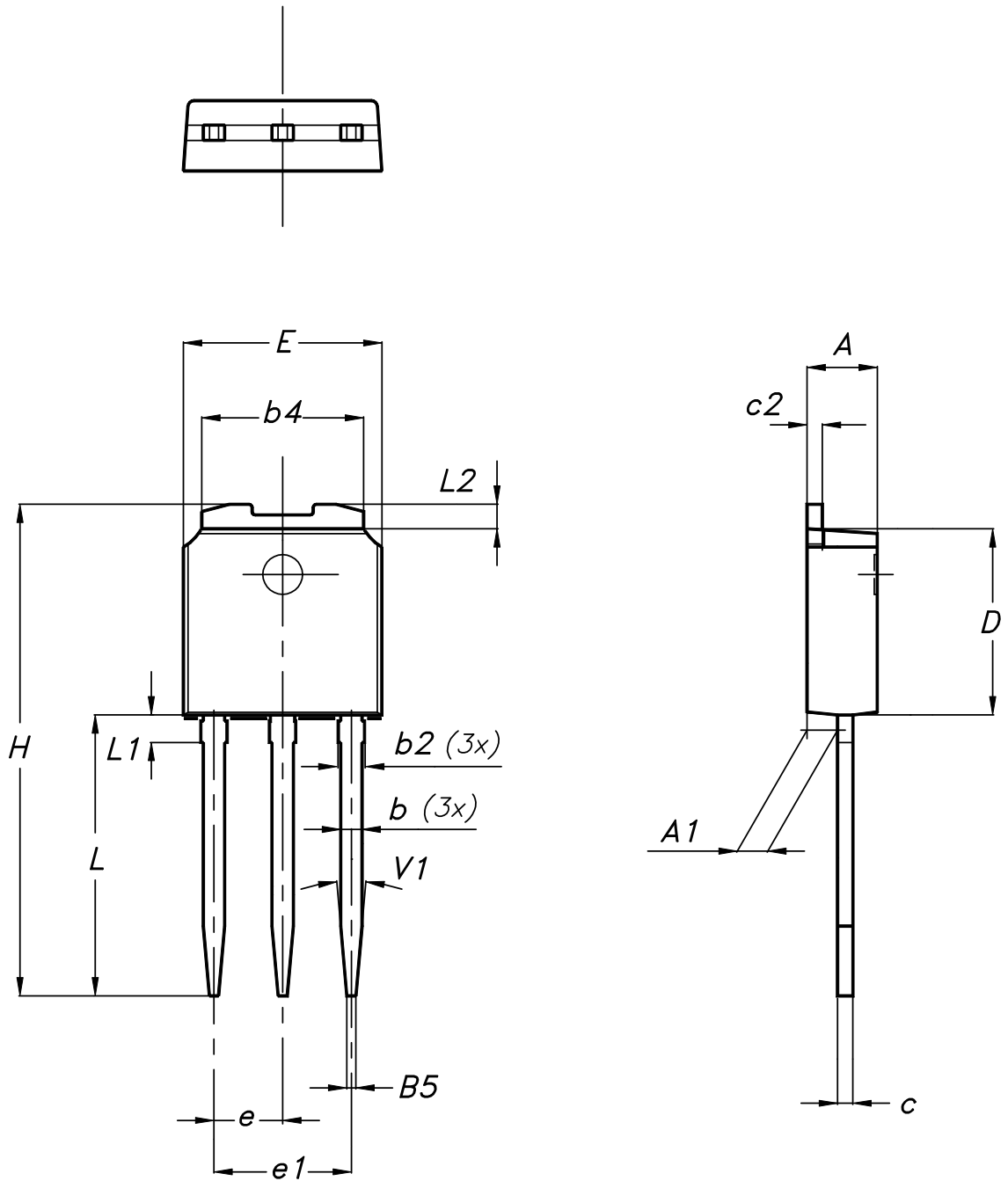
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 IPAk (TO-251) type A package information

Figure 19. IPAk (TO-251) type A package outline



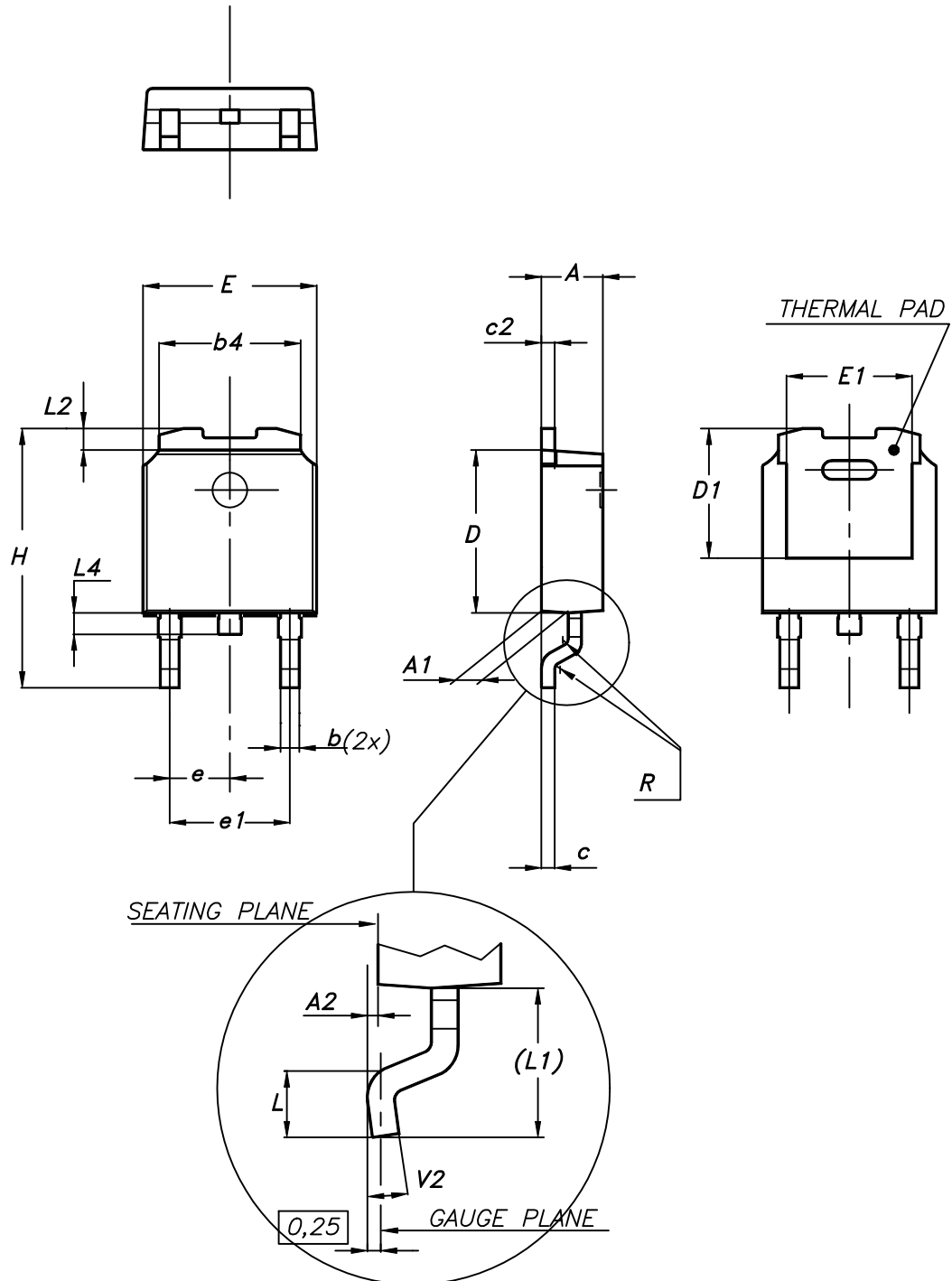
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Table 9. IPAK (TO-251) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.2 DPAK (TO-252) type A2 package information

Figure 20. DPAK (TO-252) type A2 package outline



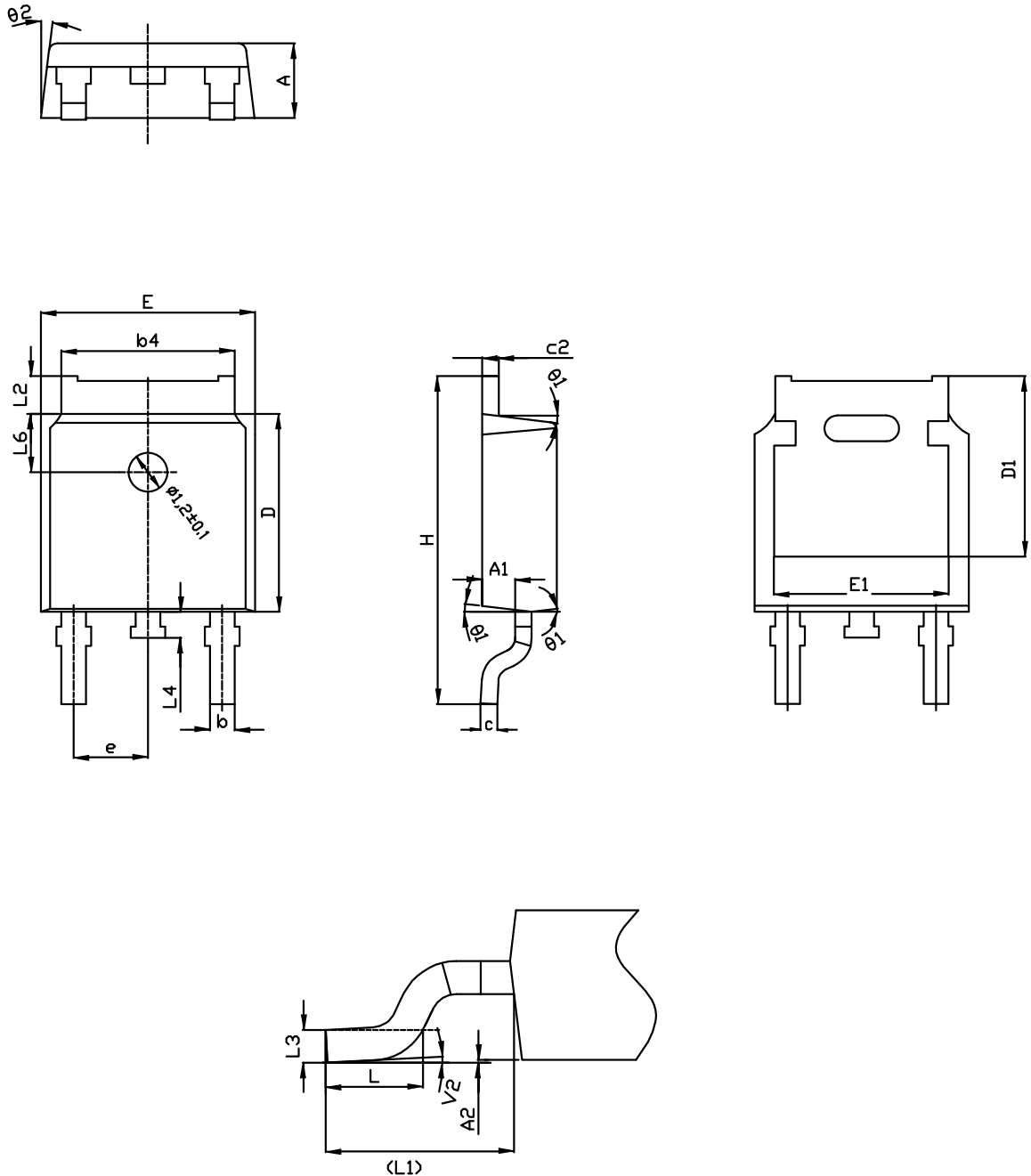
0068772_type-A2_rev25

Table 10. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.3 DPAK (TO-252) type C2 package information

Figure 21. DPAK (TO-252) type C2 package outline



0068772_C2_25

Table 11. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

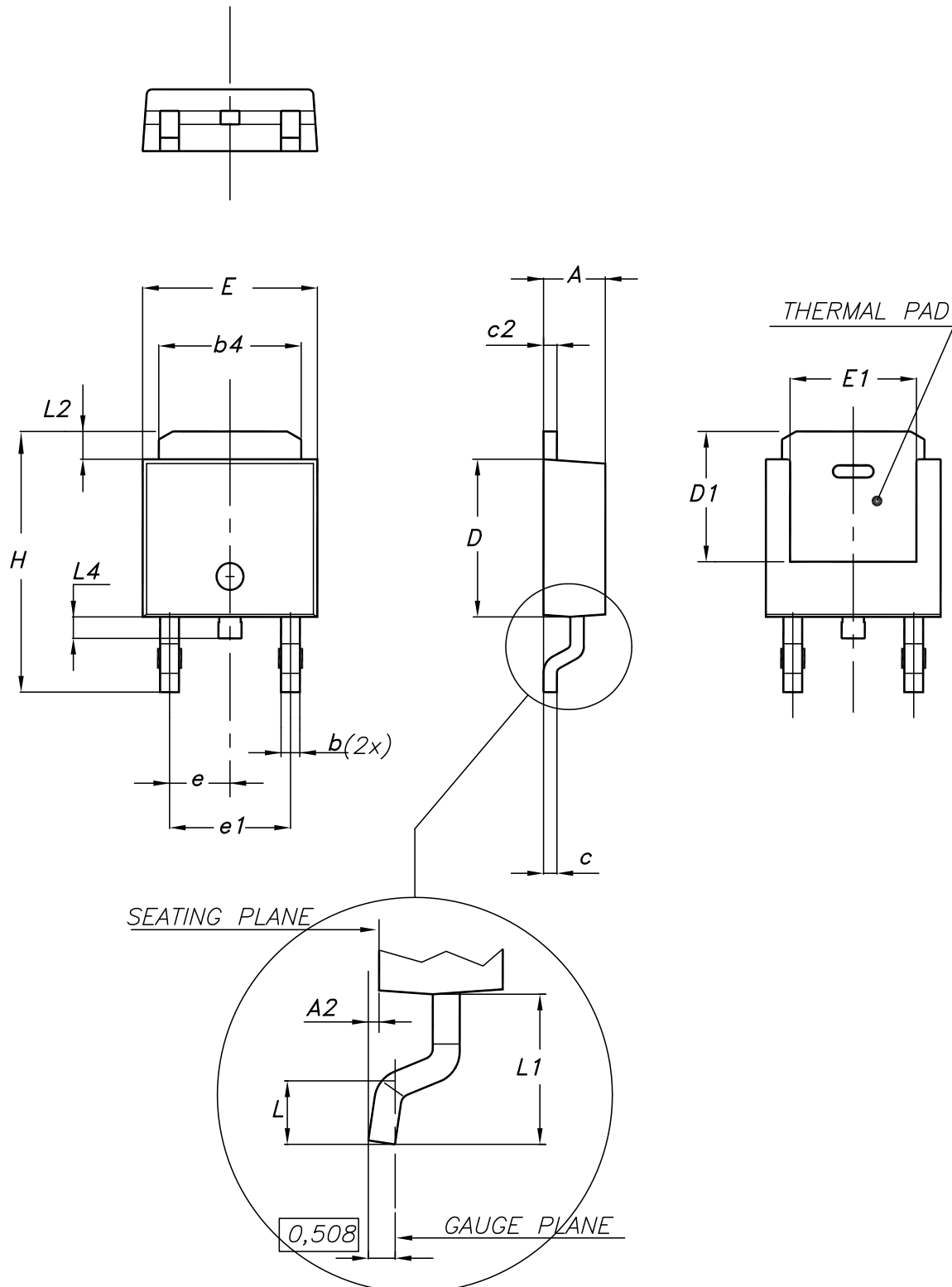
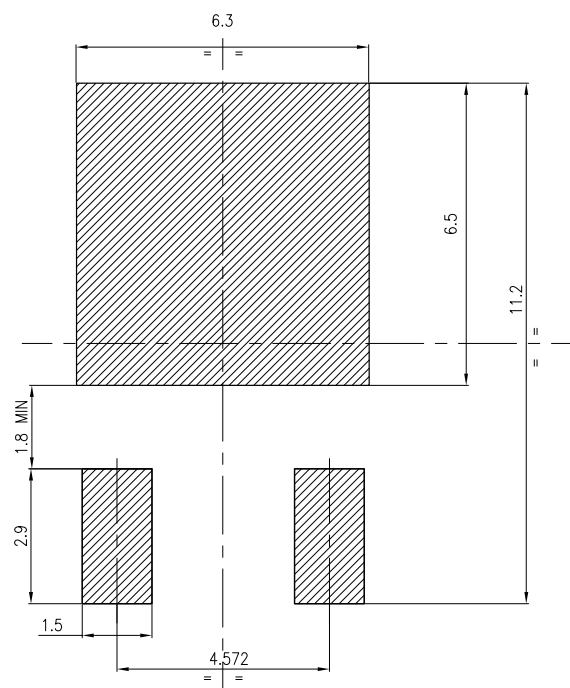
4.4 DPAK (TO-252) type E package information
Figure 22. DPAK (TO-252) type E package outline


Table 12. DPAK (TO-252) type E mechanical data

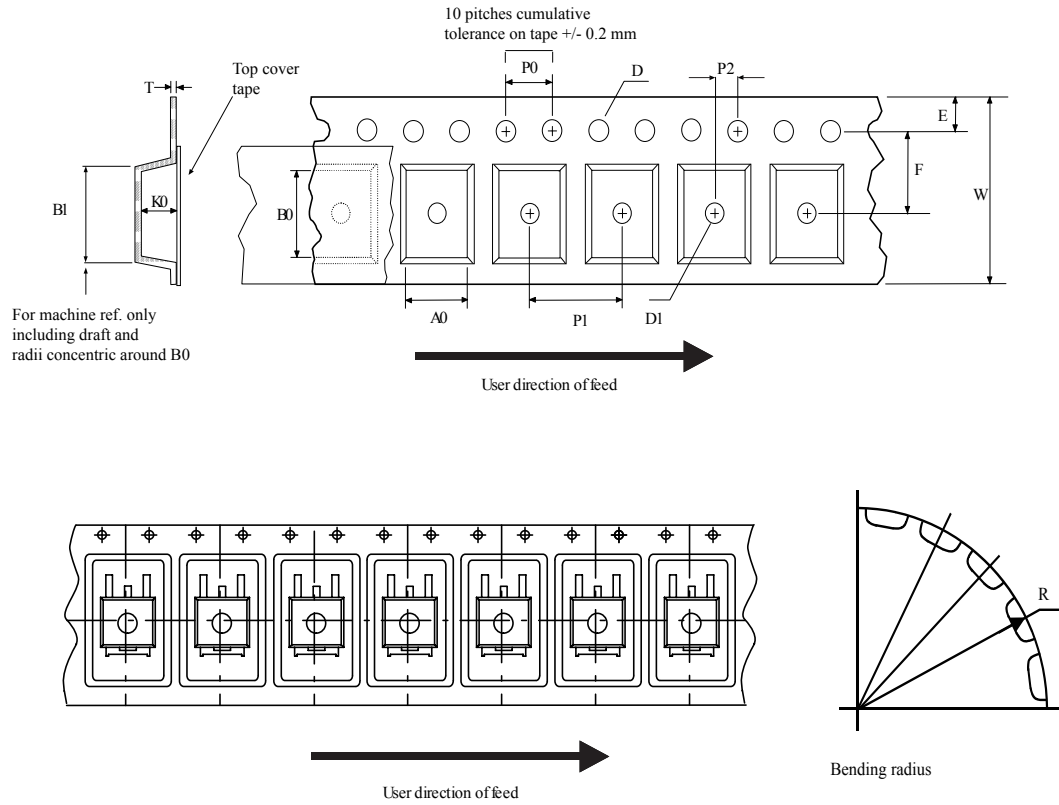
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)


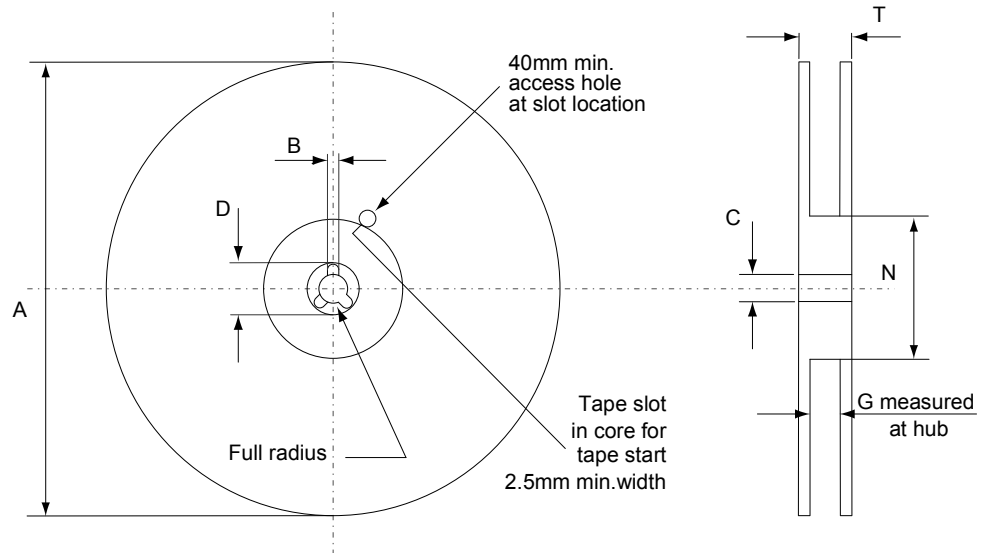
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4.5 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



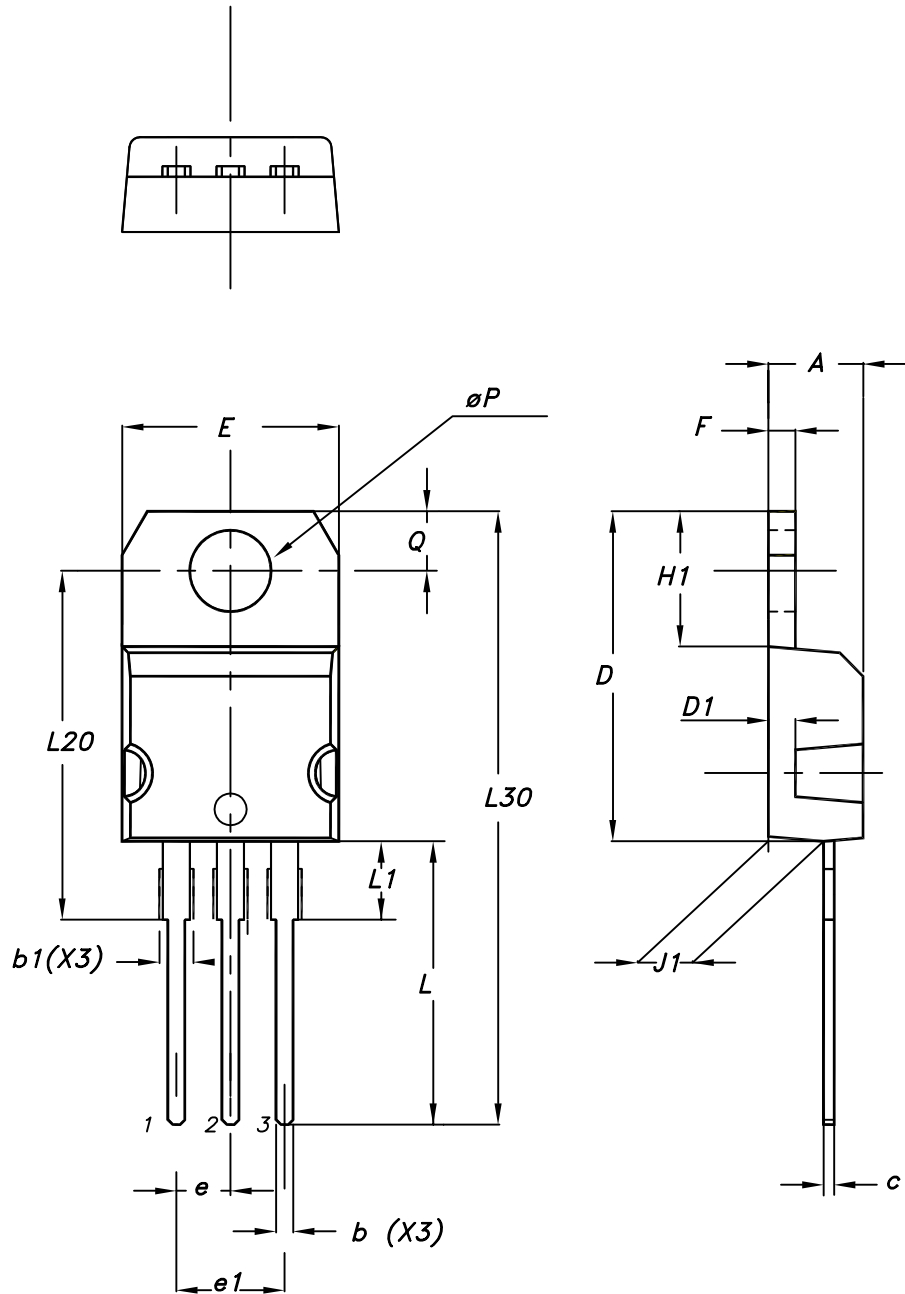
AM08852v1

Figure 25. DPAK (TO-252) reel outline


AM06038v1

Table 13. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.6 TO-220 type A package information
Figure 26. TO-220 type A package outline


0015988_typeA_Rev_21

Table 14. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Ordering information

Table 15. Order codes

Order code	Marking	Package	Packing
STD2NK90Z-1	D2NK90Z	IPAK	Tube
STD2NK90ZT4		DPAK	Tape and reel
STP2NK90Z	P2NK90Z	TO-220	Tube

Revision history

Table 16. Document revision history

Date	Version	Changes
06-Oct-2004	1	First version
08-Sep-2005	2	Complete version
05-Mar-2006	3	Inserted Ecopack indication
27-Jul-2006	4	New template, no content change
28-Jun-2018	5	Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, Section 1 Electrical ratings , Section 2 Electrical characteristics and Section 4 Package information . Minor text changes.

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