

Rail-to-Rail Input, Push-Pull Output Low power CMOS Comparators

FEATURES ($V^+ = 3V, V^- = 0V, T_a = 25^\circ C$)

- Rail-to-Rail Input
- Push Pull Output
- Supply Current 6 μA /ch typ.
- Propagation Delay 780ns typ.
- Operating Voltage 1.8 to 5.5V
- Input Offset Voltage 6mV max.
- Operating Temperature -40 to 125 $^\circ C$
- Integrated EMI filter
- Package

NJU77230	SOT-23-5, SC88A
NJU77231	SOT-23-5, SC88A, DFN6-G1(ESON6-G1)
NJU77232	MSOP8(TVSP8)*

*meet JEDEC MO-187-DA / thin type,
DFN8-U1(ESON8-U1)

GENERAL DESCRIPTION

The NJU77230/NJU77231/NJU77232 are Rail-to-Rail Input CMOS comparators featuring Low-power and Push-Pull output.

These comparators operate from 1.8V to 5.5V and low supply current of 6 μA /ch.typ. This feature is suitable for battery powered application.

The NJU77231/NJU77232 are available in small size Package, DFN6-G1(1616), DFN8-U1(2020), significantly reducing the required portable application's board area.

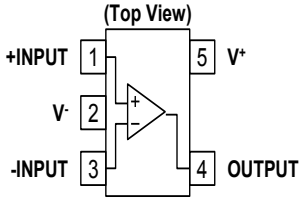
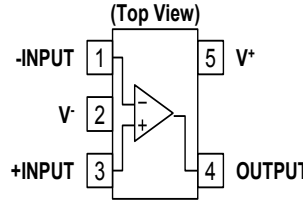
APPLICATION

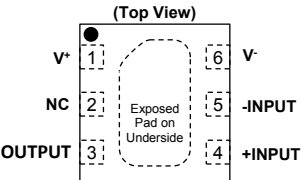
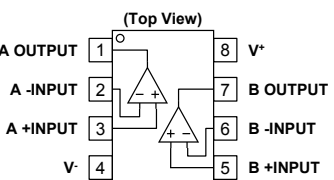
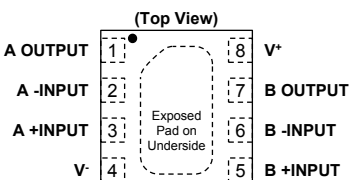
- Portable and Battery-Powered Applications
- Alarm and Surveillance Circuits
- Industrial Instruments
- Sensor Applications

RELATED PRODUCTS

Features	Single	Dual
Rail-to-Rail Input Open-Drain Output Low power CMOS Comparators	NJU77240 NJU77241	NJU77242

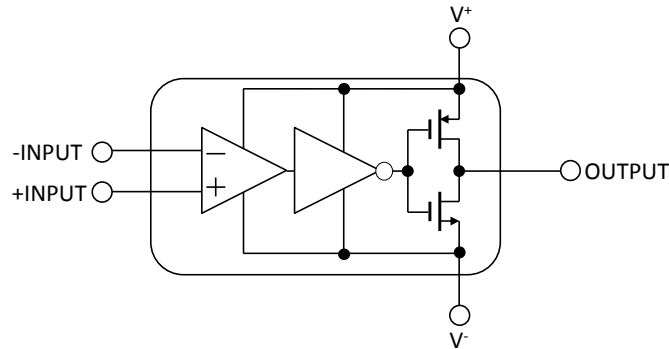
PIN CONFIGURATION

Parts Number	NJU77230F	NJU77230F3	NJU77231F	NJU77231F3
Package Outline	SOT-23-5	SC-88A	SOT-23-5	SC-88A
Pin Function				

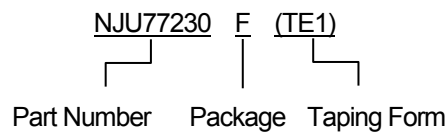
Parts Number	NJU77231KG1	NJU77232RB1	NJU77232KU1
Package Outline	DFN6-G1(ESON6-G1)(*)	MSOP8(TVSP8)	DFN8-U1(ESON8-U1) (*)
Pin Function			

(*)Connect to exposed pad to V^-

■BLOCK DIAGRAM



■PRODUCT NAME INFORMATION



■ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJU77230F	SOT-23-5	yes	yes	Sn2Bi	1H	15	3,000
NJU77230F3	SC-88A	yes	yes	Sn2Bi	F1	7.5	3,000
NJU77231F	SOT-23-5	yes	yes	Sn2Bi	1J	15	3,000
NJU77231F3	SC-88A	yes	yes	Sn2Bi	F2	7.5	3,000
NJU77231KG1	DFN6-G1	yes	yes	Sn2Bi	77231	3.5	3,000
NJU77232RB1	MSOP8(TVSP8)	yes	yes	Sn2Bi	77232	18	2,000
NJU77232KU1	DFN8-U1	yes	yes	Sn2Bi	77232	5.3	3,000

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+ - V^-$	7	V
Input Voltage ^(1,2)	V_{IN}	$V^- - 0.3$ to $V^+ + 0.3$	V
Input Current ⁽²⁾	I_{IN}	10	mA
Differential Input Voltage ⁽³⁾	V_{ID}	± 7	V
Output Terminal Input Voltage ⁽¹⁾	V_o	$V^- - 0.3$ to $V^+ + 0.3$	V
Power Dissipation($T_a=25^\circ\text{C}$)	P_D	(2-layer / 4-layer)	mW
SOT-23-5 ⁽⁴⁾		480 / 650	
SC-88A ⁽⁴⁾		360 / 490	
DFN6-G1 ⁽⁵⁾		330 / 1200	
MSOP8(TVSP8) ⁽⁴⁾		510 / 680	
DFN8-U1 ⁽⁵⁾	450 / 1200		
Junction Temperature	T_{jmax}	+150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to +150	$^\circ\text{C}$

(1) Voltage values are limited at 7V.

(2) Input voltages outside the supply voltage will be clamped by ESD protection diodes. If the input voltage exceeds the supply voltage, the input current must be limited 10mA or less by using a restriction resistance.

(3) Differential voltage is the voltage difference between +INPUT and - INPUT.

For supply voltage less than +7V, the absolute maximum rating is equal to the supply voltage.

(4) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers FR4)

Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers FR4), internal Cu area: 74.2 x 74.2mm

(5) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

*For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance	θ_{ja}	(2-layer / 4-layer)	$^{\circ}\text{C/W}$
SOT-23-5 ⁽⁶⁾		259 / 193	
SC-88A ⁽⁶⁾		352 / 256	
DFN6-G1 ⁽⁷⁾		381 / 106	
MSOP8(TVSP8) ⁽⁶⁾		244 / 185	
DFN8-U1 ⁽⁷⁾	278 / 107		
Junction-to-Top of package characterization parameter	ψ_{jt}	(2-layer/ 4-layer)	$^{\circ}\text{C/W}$
SOT-23-5 ⁽⁶⁾		67 / 58	
SC-88A ⁽⁶⁾		91 / 73	
DFN6-G1 ⁽⁷⁾		64 / 26	
MSOP8(TVSP8) ⁽⁶⁾		51 / 45	
DFN8-U1 ⁽⁷⁾	42 / 25		

(6) Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers FR4)

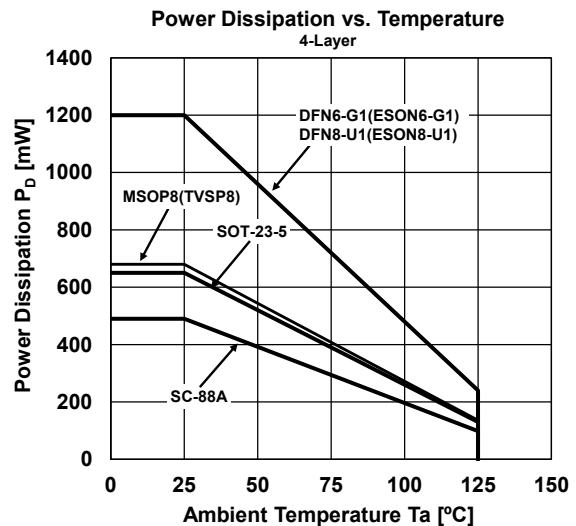
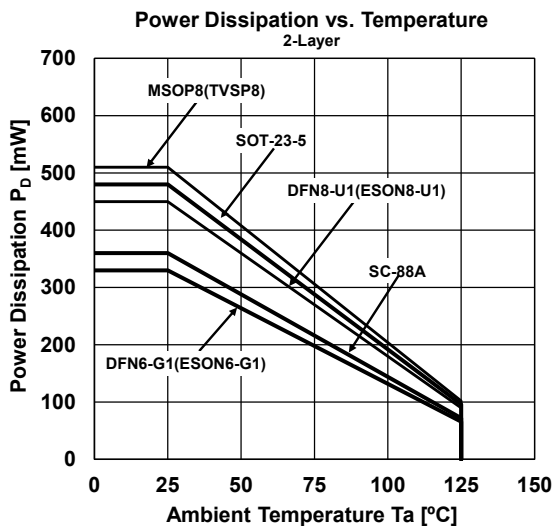
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Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)

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■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage			
Single Supply	$V^+ - V^-$	+1.8 to +5.5	V
Dual Supply	V^+ / V^-	±0.9 to ±2.75	
Operating Ambient Temperature	T_{opr}	- 40 to +125	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS

(Unless otherwise specified, $V_+=3V$, $V_-=0V$, $R_L=OPEN$, $T_a=25^\circ C$)

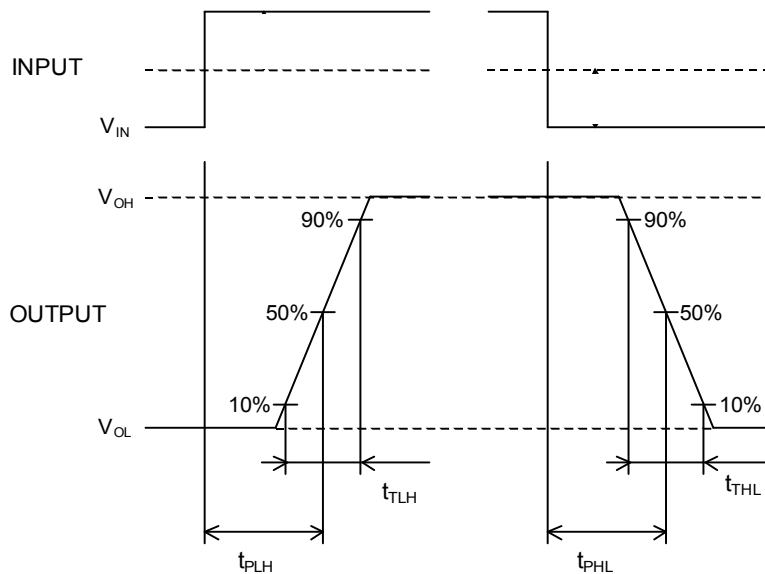
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current (per comparator)	I_{SUPPLY}	$V_{ID}=100mV, V_{com}=0V$	—	6	10	μA
		$V_{ID}=100mV, V_{com}=3V$	—	9	14	μA
Input Offset Voltage	V_{IO}	$V_{COM}=0V$	—	1	6	mV
		$V_{COM}=3V$	—	1	7	mV
Input Offset Current	I_{IO}		—	1	—	μA
Input Bias Current	I_B		—	1	—	μA
Common Mode Input Voltage Range	V_{ICM}	$CMR \geq 50dB$	0	—	3	V
Open-Loop Voltage Gain	A_v	$R_L=5.1k\Omega$	—	100	—	dB
Common Mode Rejection Ratio	CMR	$V_{ICM}=0$ to $3V$	50	70	—	dB
Supply Voltage Rejection Ratio	SVR	$V_{COM}=0V$, $V^+=1.8$ to $5.5V$	65	85	—	dB
High-level Output Voltage	V_{OH}	$I_{SOURCE}=3mA$	2.7	2.8	—	V
Low-level Output Voltage	V_{OL}	$I_{SINK}=3mA$	—	0.2	0.3	V

● SWITCHING CHARACTERISTICS

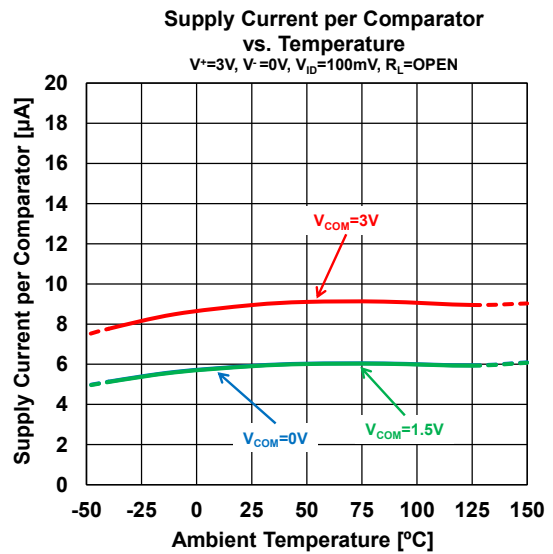
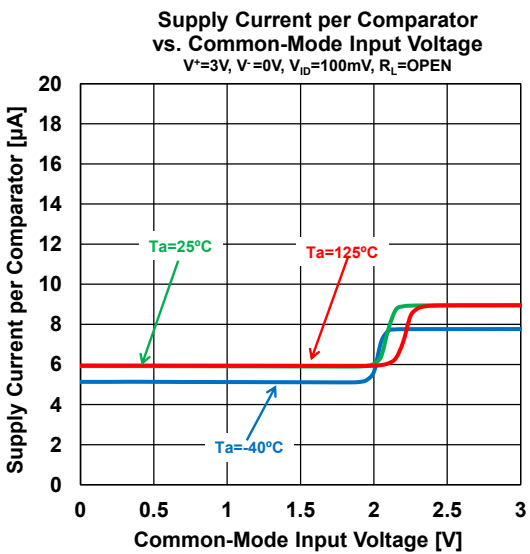
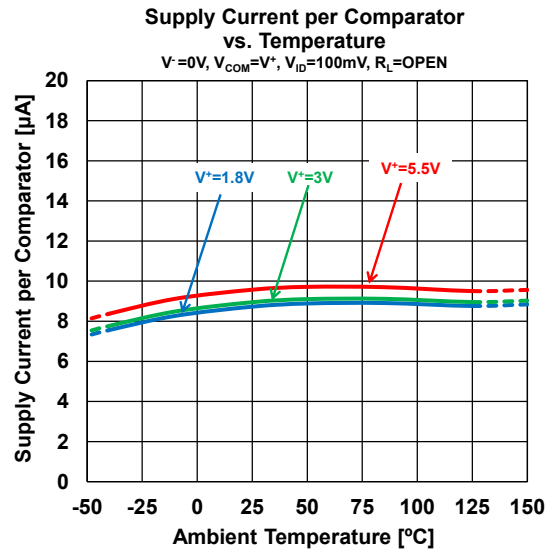
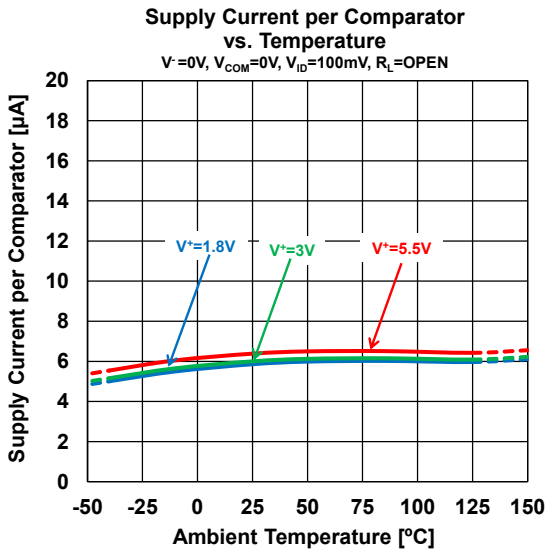
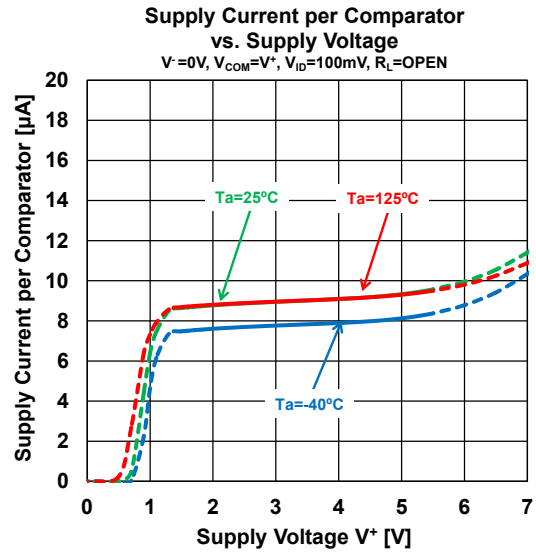
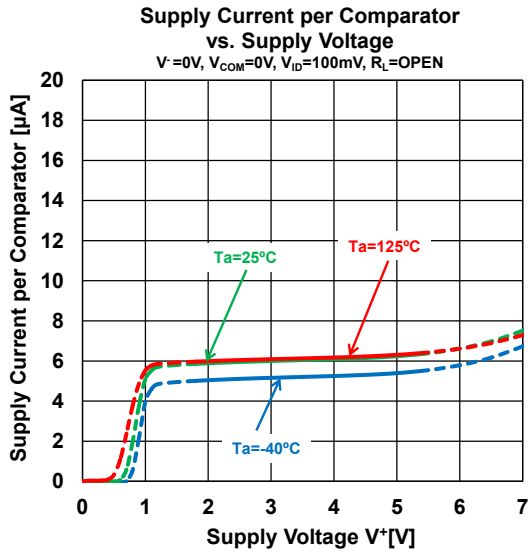
(Unless otherwise specified, $V^+=+3V$, $V_-=0V$, $T_a=25^\circ C$, $C_L=15pF$, $R_L=5.1k\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Low to High	t_{PLH}	Overdrive= $100mV$	—	780	—	ns
Propagation Delay High to Low	t_{PHL}	Overdrive= $100mV$	—	480	—	ns
Output Signal Rising Time	t_{TLH}	Overdrive= $100mV$	—	20	—	ns
Output Signal Falling Time	t_{THL}	Overdrive= $100mV$	—	11	—	ns

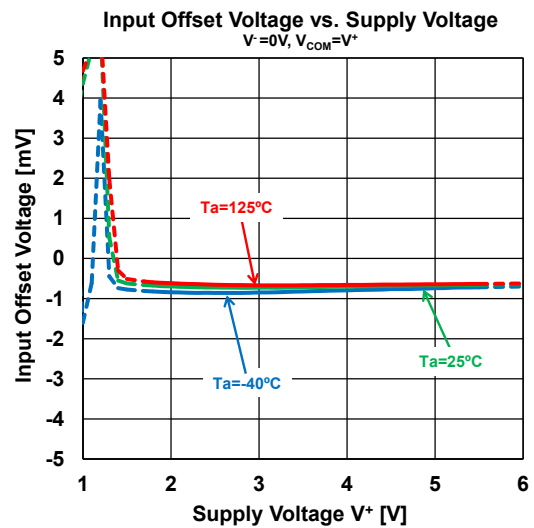
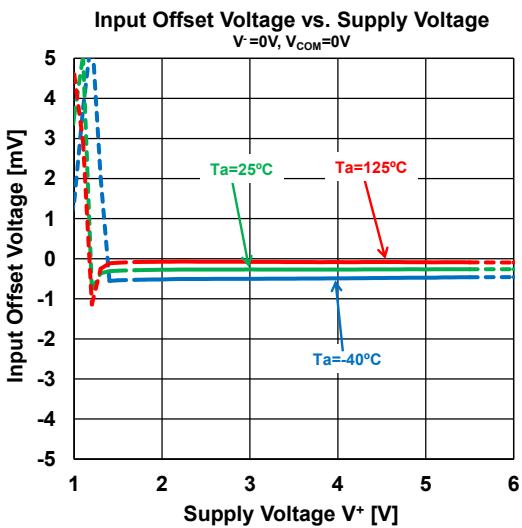
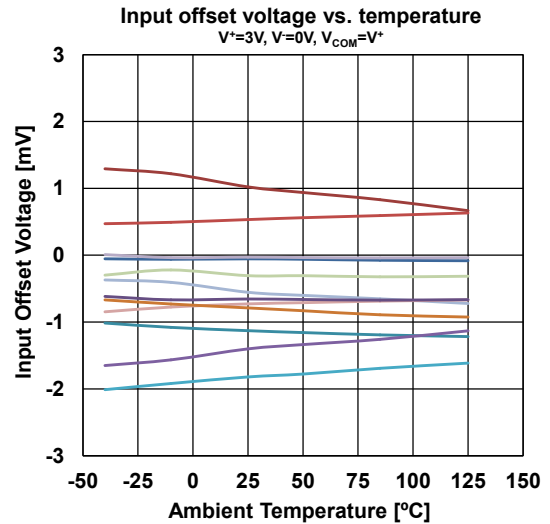
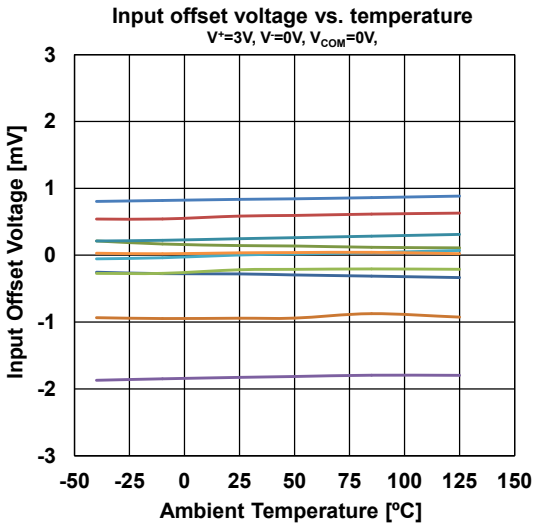
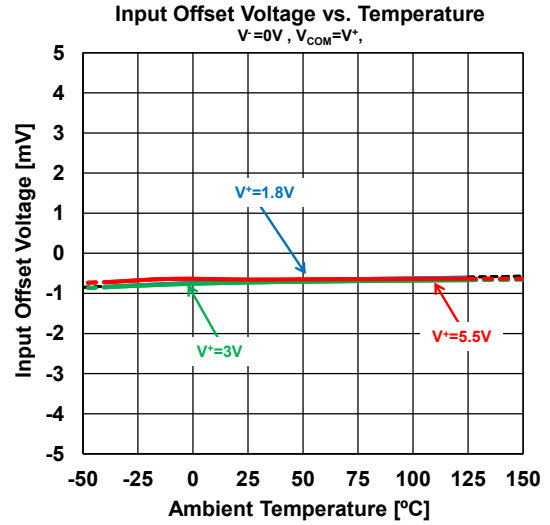
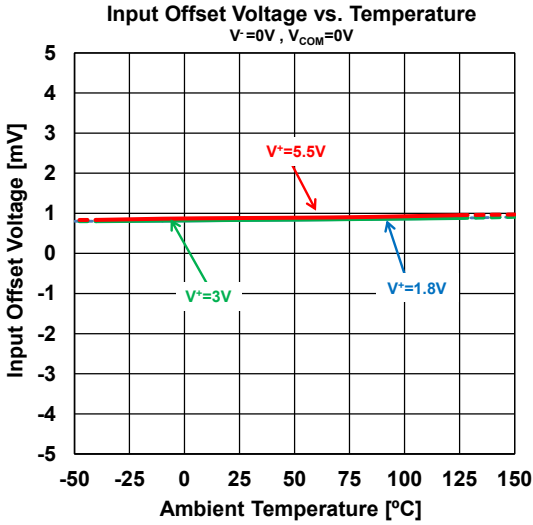
■ TIMING WAVEFORM



■ TYPICAL CHARACTERISTICS

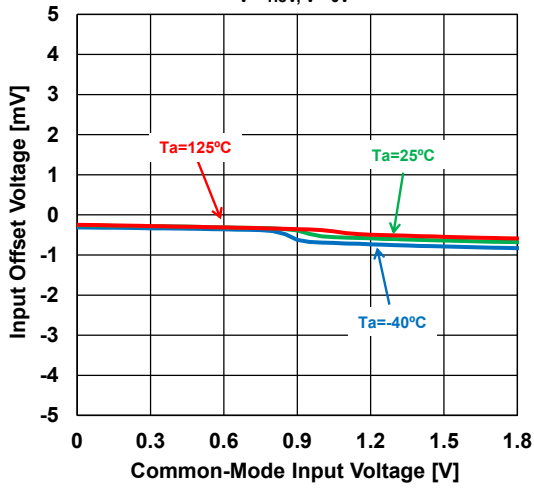


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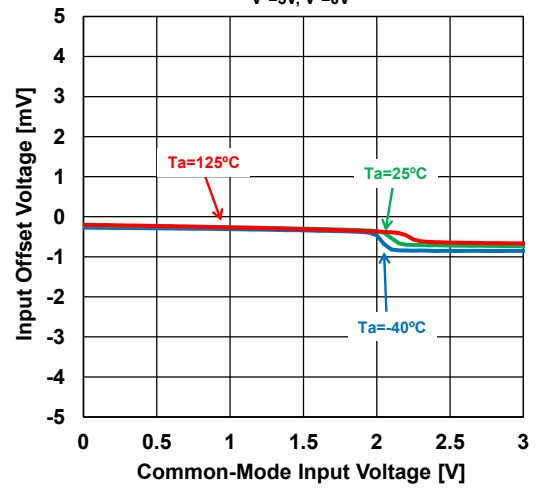


■ TYPICAL CHARACTERISTICS

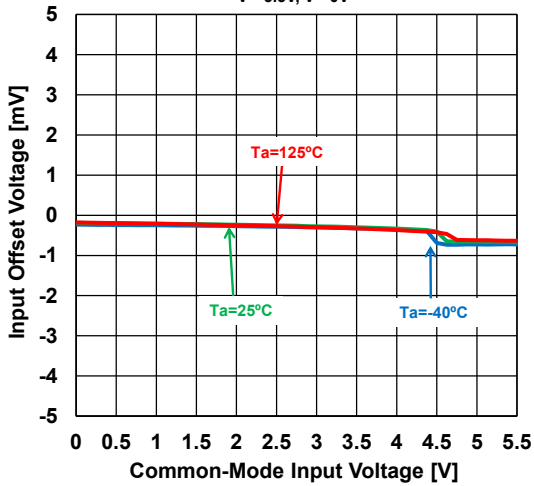
Input Offset Voltage
vs. Common-Mode Input Voltage
 $V^+=1.8V, V^-=0V$



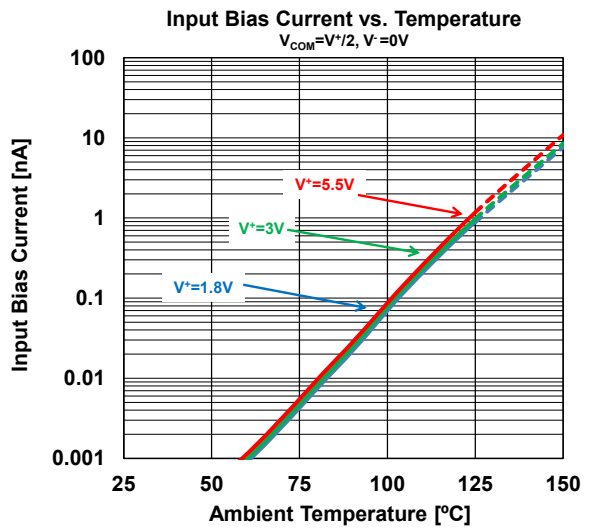
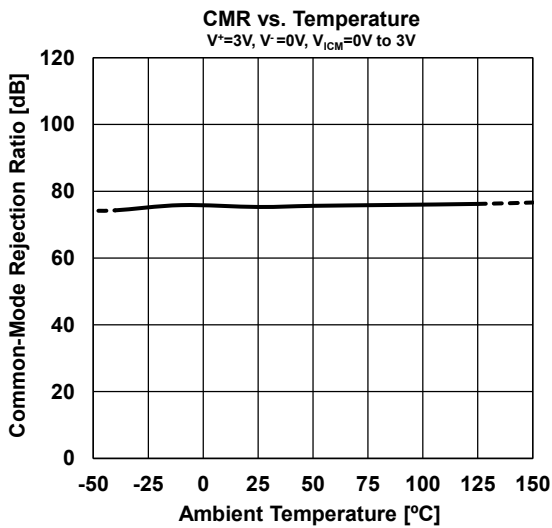
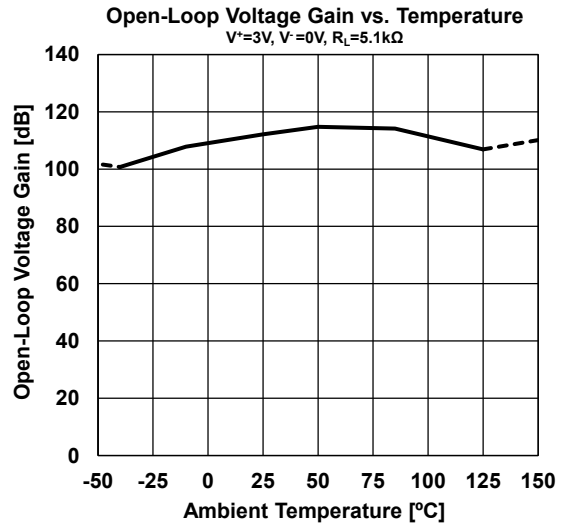
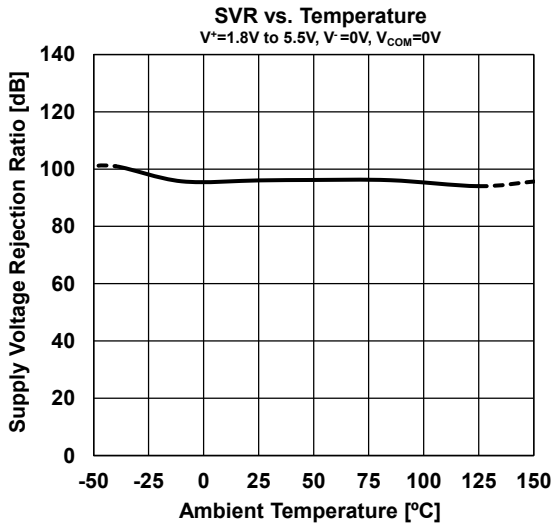
Input Offset Voltage
vs. Common-Mode Input Voltage
 $V^+=3V, V^-=0V$



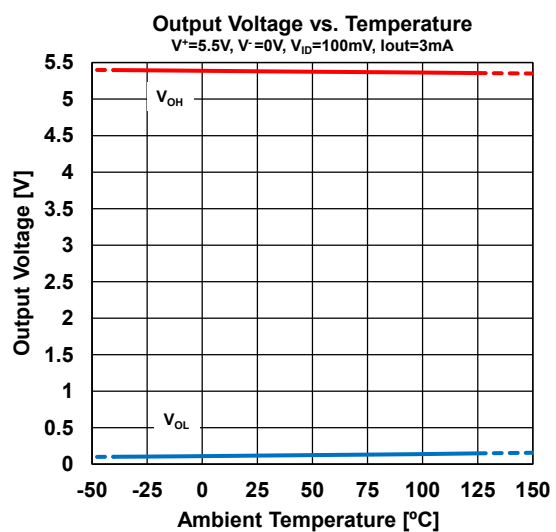
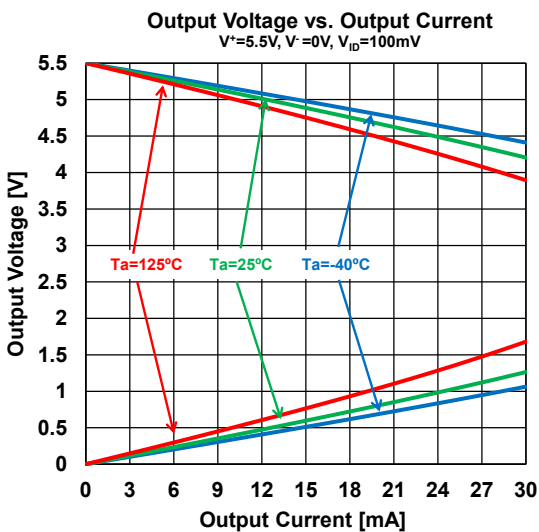
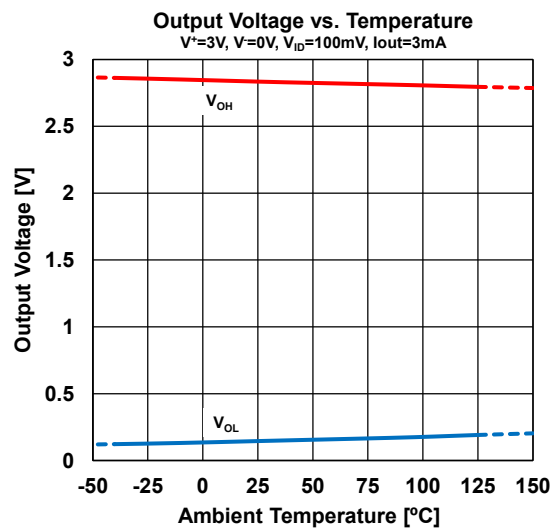
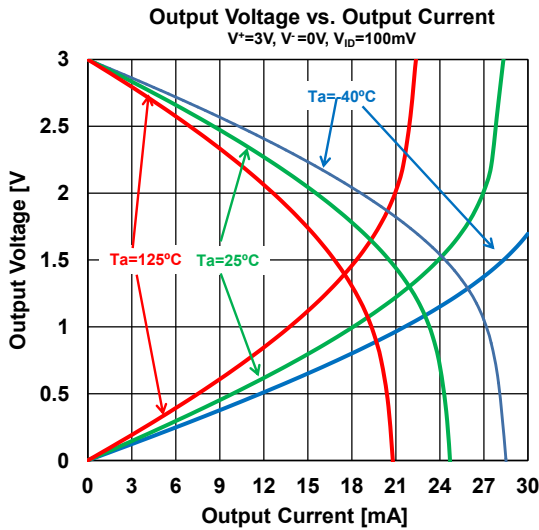
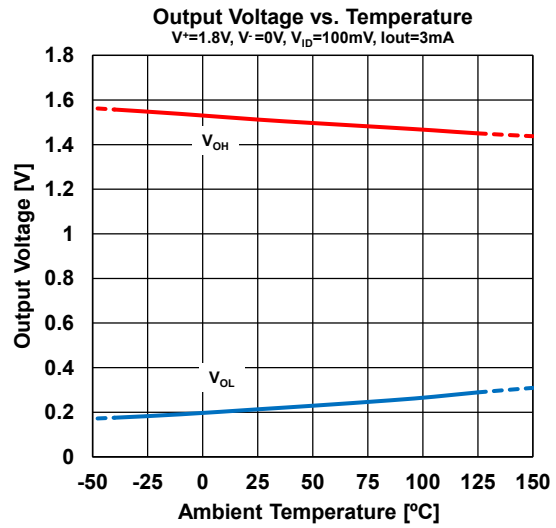
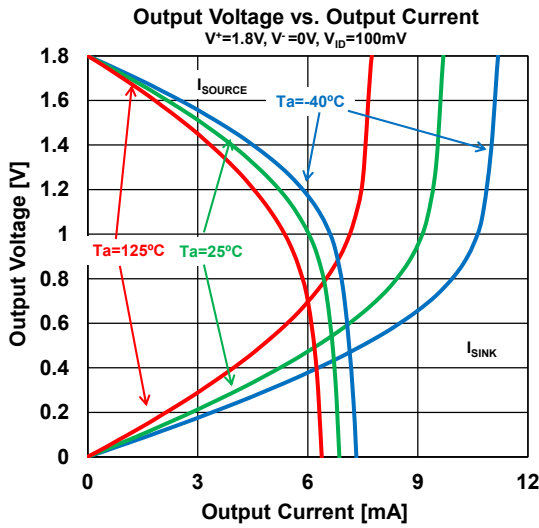
Input Offset Voltage
vs. Common-Mode Input Voltage
 $V^+=5.5V, V^-=0V$



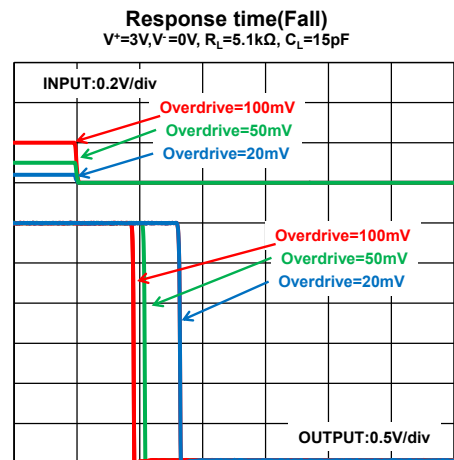
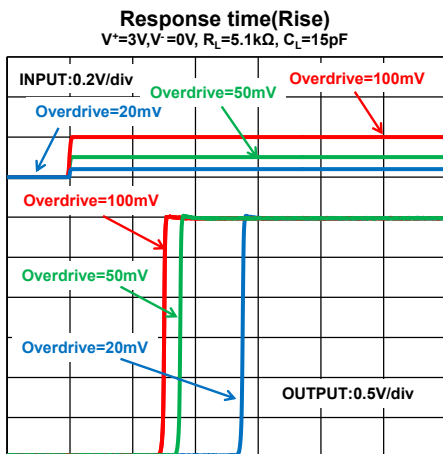
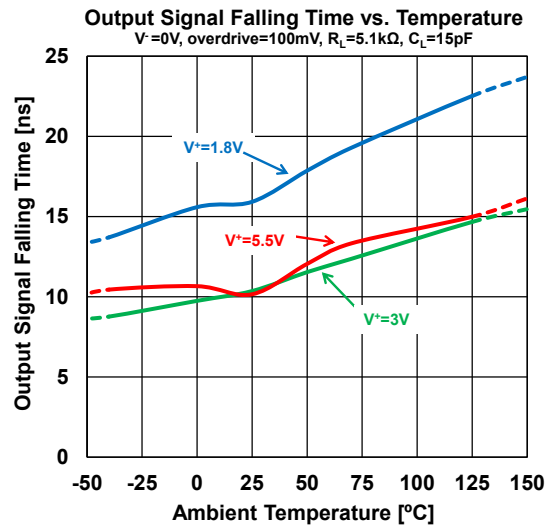
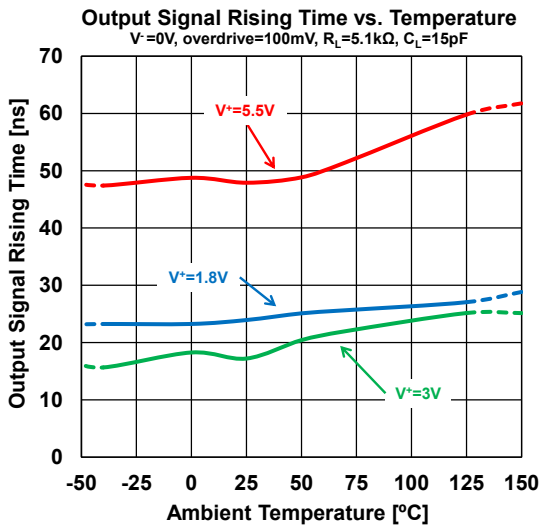
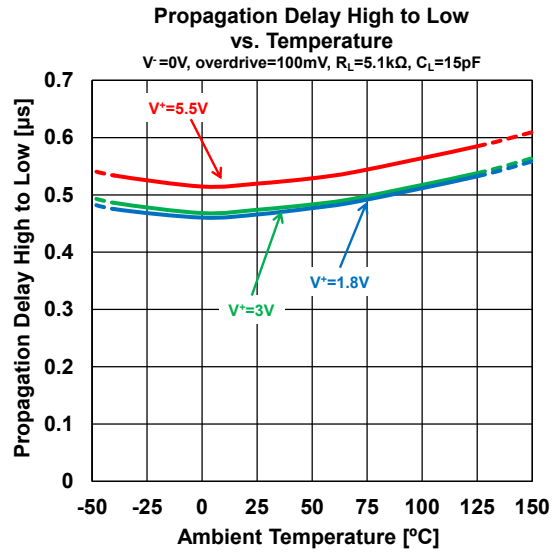
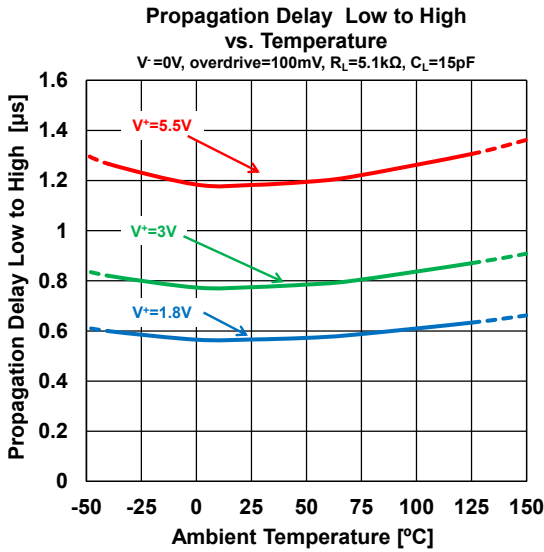
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS



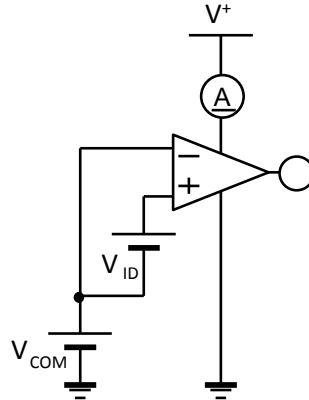
■ TYPICAL CHARACTERISTICS



■ TYPICAL TEST CIRCUIT

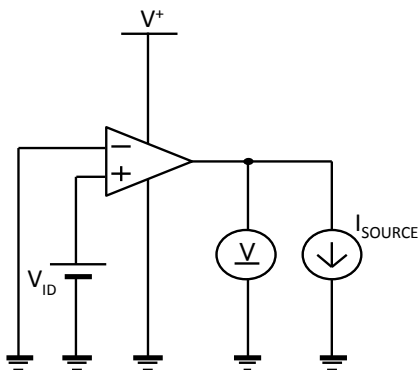
● Supply Current (I_{SUPPLY})

- $V^+ = 3V, V^- = 0V, V_{COM} = 0V, V_{ID} = 100mV$
- $V^+ = 3V, V^- = 0V, V_{COM} = 3V, V_{ID} = 100mV$



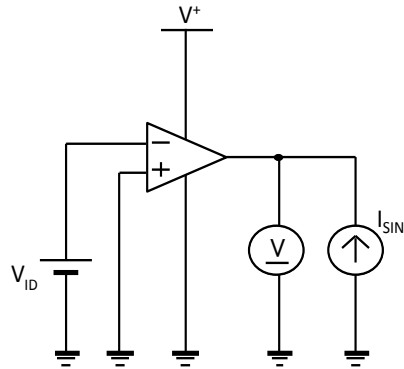
● High-level Output Voltage (V_{OH})

- $V^+ = 3V, V^- = 0V, I_{SOURCE} = 3mA, V_{ID} = 100mV$



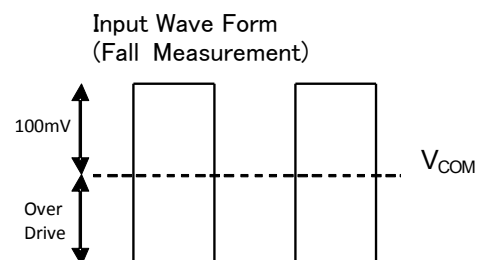
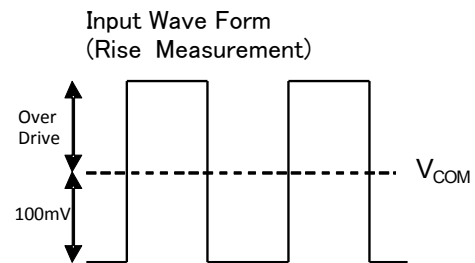
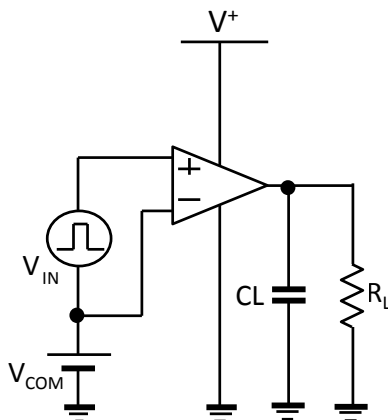
● Low-level Output Voltage (V_{OL})

- $V^+ = 3V, V^- = 0V, I_{SINK} = 3mA, V_{ID} = 100mV$



● Propagation Delay (t_{PLH}, t_{PHL}), Output Signal Rising Time (t_{RLH}), Output Signal Falling Time (t_{RTL})

- $V^+ = 3V, V^- = 0V, V_{COM} = 0V, R_L = 5.1k\Omega, C_L = 15pF, \text{Over drive} = 100mV$



APPLICATION NOTE

Input Voltage Exceeding the Supply Voltage

Inputs of the NJU77230/ NJU77231/ NJU77232 are protected by ESD diodes (shown in Figure1) that will conduct if the input voltages exceed the power supplies by more than approximately 300mV. Momentary voltages greater than 300mV beyond the power supply, inputs can be tolerated if the current is limited to 10mA. Figure2 is easily accomplished with an input resistor. If the input voltage exceeds the supply voltage, the input current must be limited 10mA or less by using a restriction resistance (R_{LIMIT}) as shown in figure2.

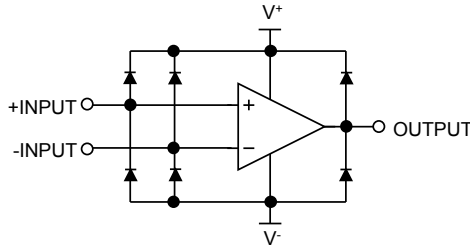


Figure1. Simplified Schematic

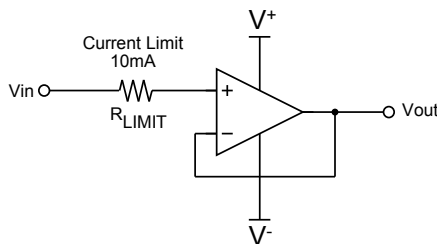


Figure2. Input Current Protection for Voltages exceeding the Supply Voltage.

Bypass Capacitor

It is advised to add a bypass capacitor between the supply voltage and ground as close as possible to device.

• EMIRR(EMI Rejection Ratio) Definition

EMIRR is a parameter indicating the EMI robustness of an OP-Amp. The definition of EMIRR is given by the following formula (1). We can grasp the tolerance of the RF signal by measuring an RF signal and offset voltage shift quantity.

$$EMIRR = 20 \cdot \log \left(\frac{V_{RF_PEAK}}{|\Delta V_{IO}|} \right) \quad \dots(1)$$

V_{RF_PEAK} : RF Signal Amplitude [V_P]

ΔV_{IO} : Input offset voltage shift quantity [V]

Offset voltage shift is small so that a value of EMIRR is big. And it understands that the tolerance for the RF signal is high. In addition, about the input offset voltage shift with the RF signal, there is the thinking that influence applied to the input terminal is dominant. Therefore, generally the EMIRR becomes value that applied an RF signal to +INPUT terminal.

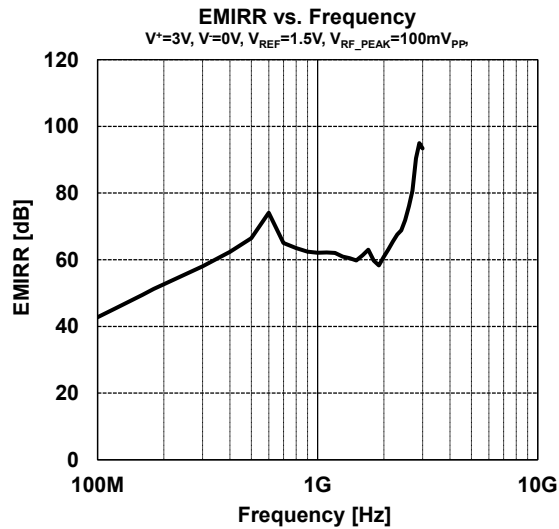
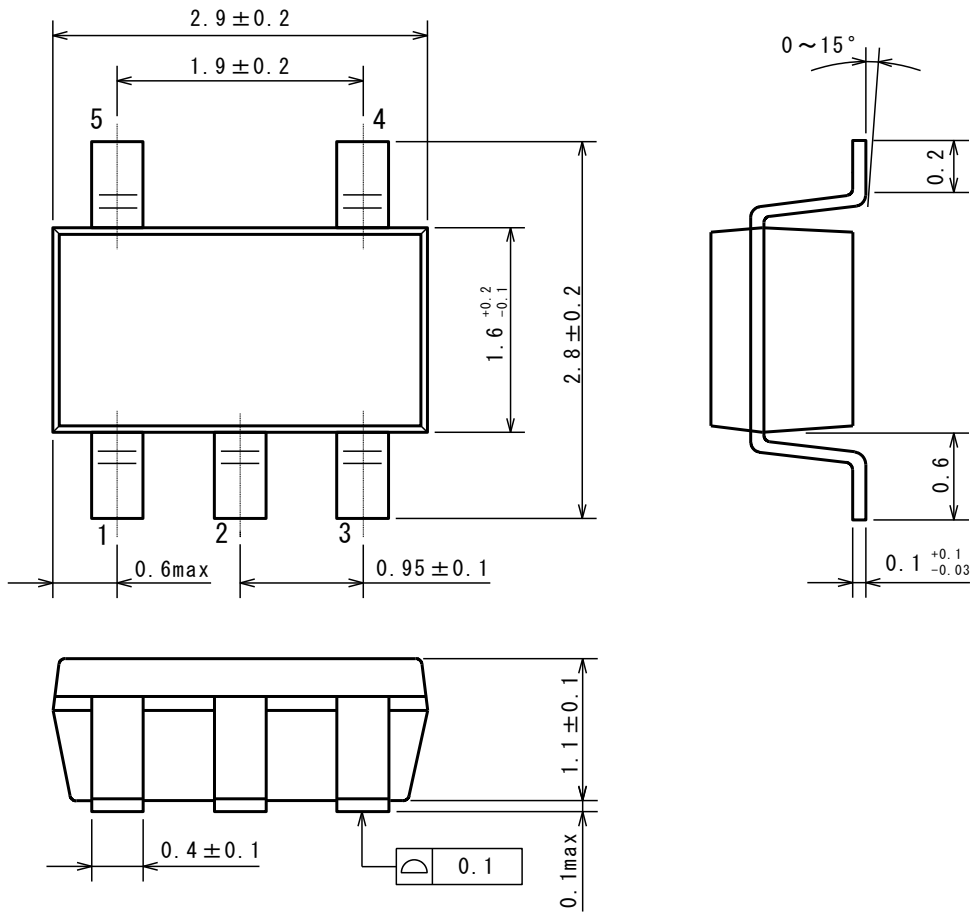


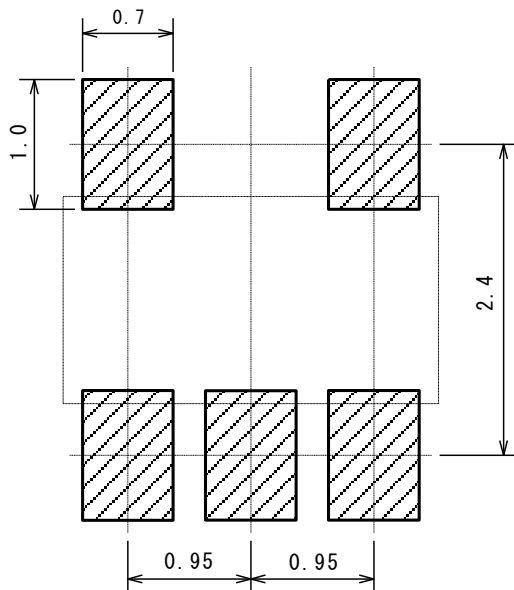
Figure3. EMIRR vs. Frequency

*For details, refer to " Application Note for EMI Immunity" in our HP: <http://www.njr.com/>

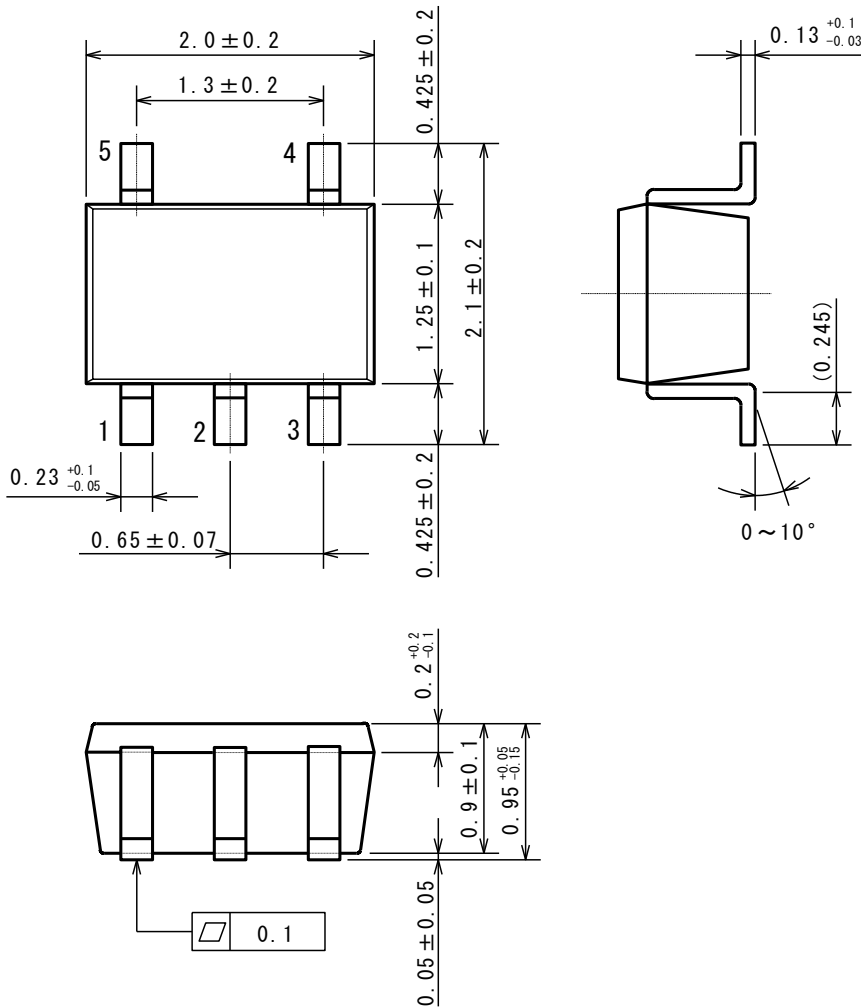
PACKAGE DIMENSIONS



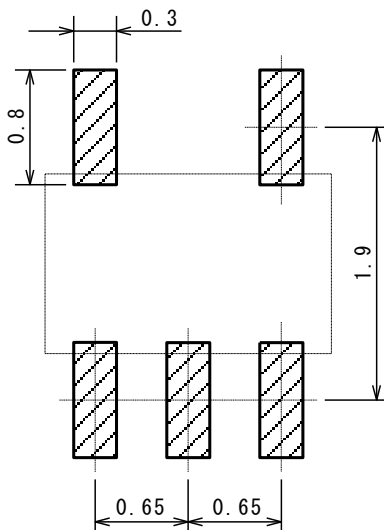
EXAMPLE OF SOLDER PADS DIMENSIONS



PACKAGE DIMENSIONS

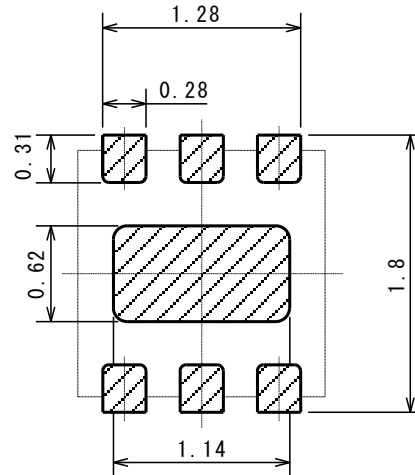
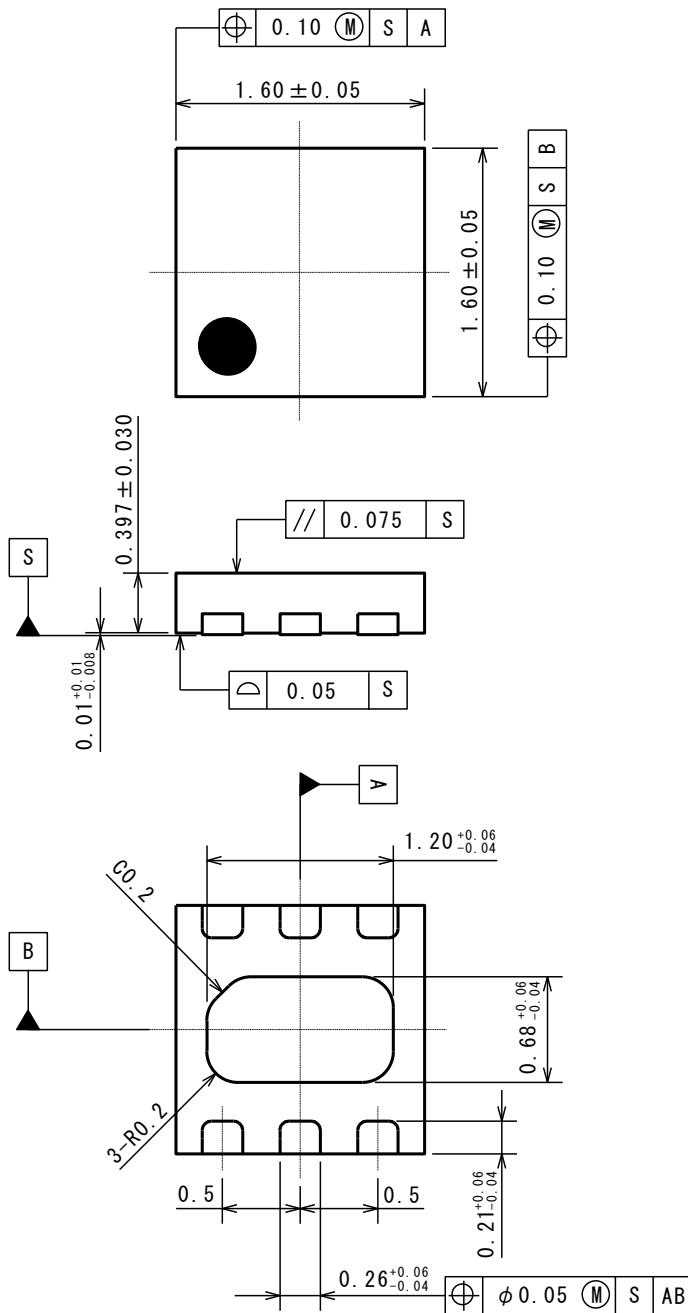


EXAMPLE OF SOLDER PADS DIMENSIONS

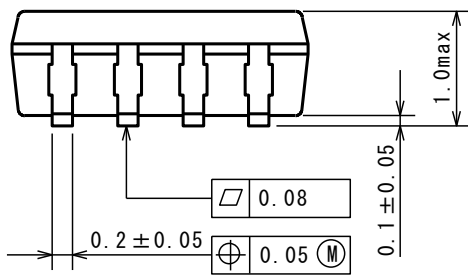
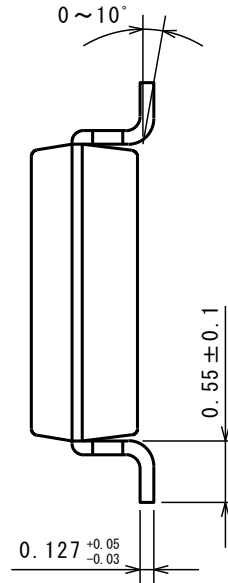
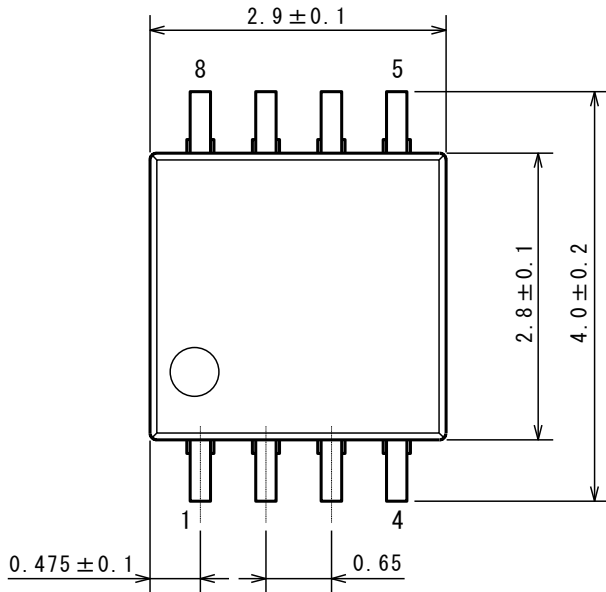


PACKAGE DIMENSIONS

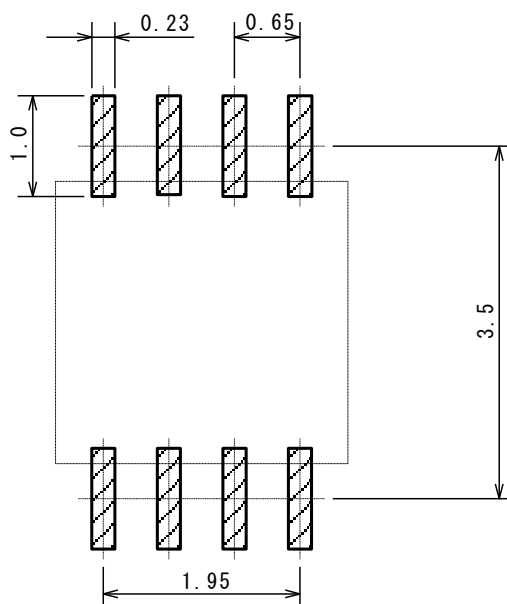
EXAMPLE OF SOLDER PADS DIMENSIONS



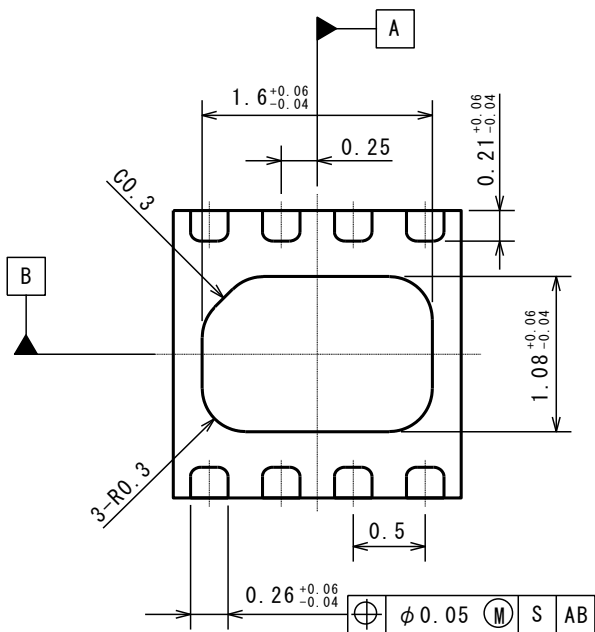
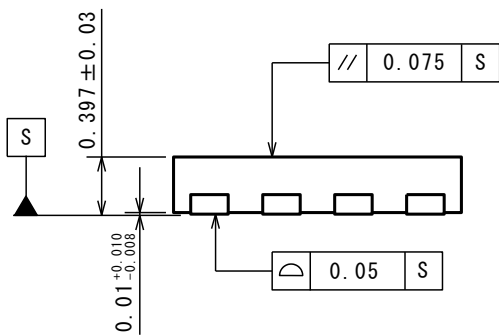
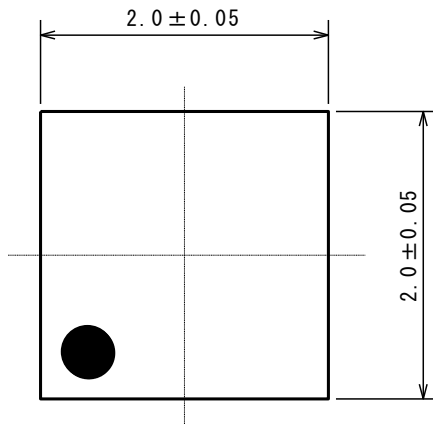
PACKAGE DIMENSIONS



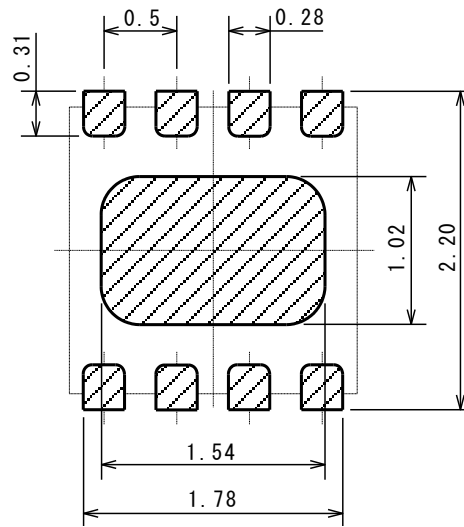
EXAMPLE OF SOLDER PADS DIMENSIONS



PACKAGE DIMENSIONS

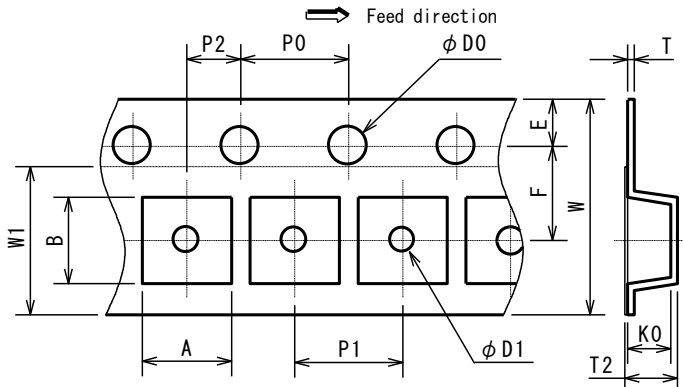


EXAMPLE OF SOLDER PADS DIMENSIONS



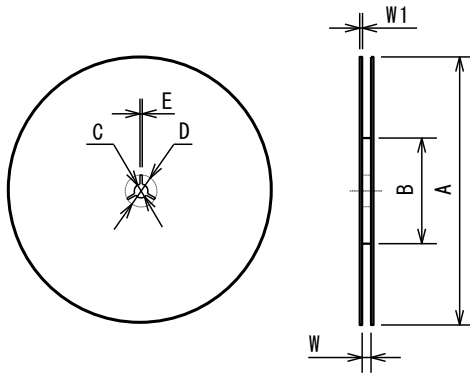
PACKING SPEC

TAPING DIMENSIONS



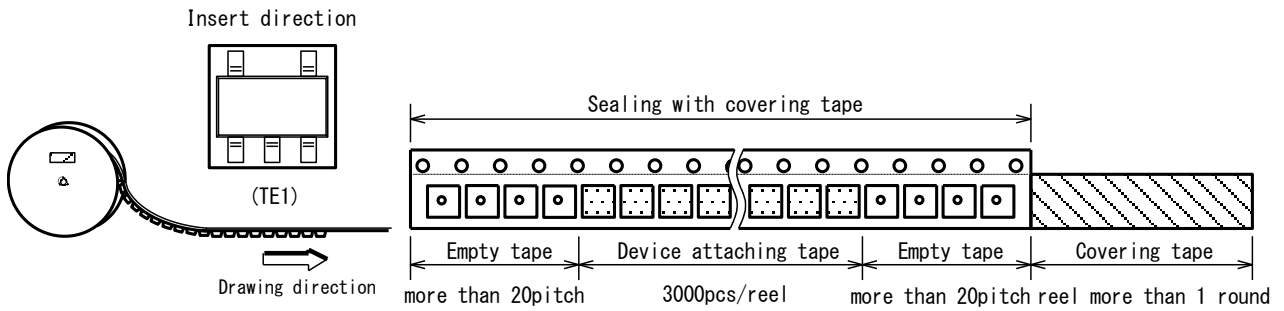
SYMBOL	DIMENSION	REMARKS
A	3.3±0.1	BOTTOM DIMENSION
B	3.2±0.1	BOTTOM DIMENSION
D0	1.55	
D1	1.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.82	
K0	1.5±0.1	
W	8.0±0.3	
W1	5.5	THICKNESS 0.1MAX

REEL DIMENSIONS

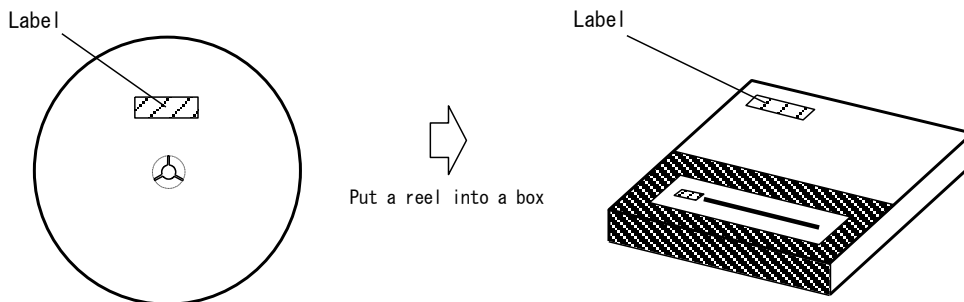


SYMBOL	DIMENSION
A	φ 180±1
B	φ 60±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9±0.5
W1	1.2±0.2

TAPING STATE

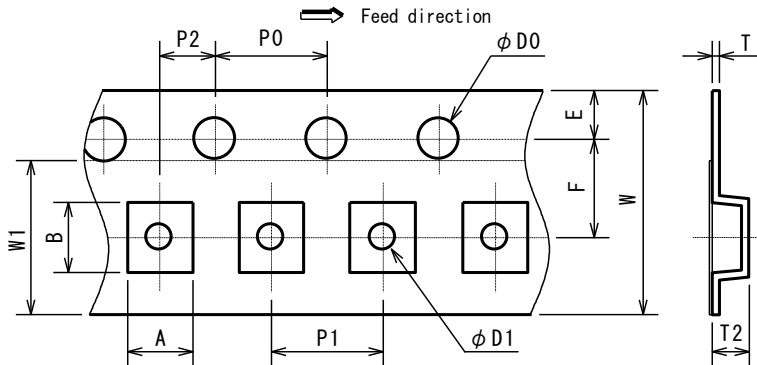


PACKING STATE



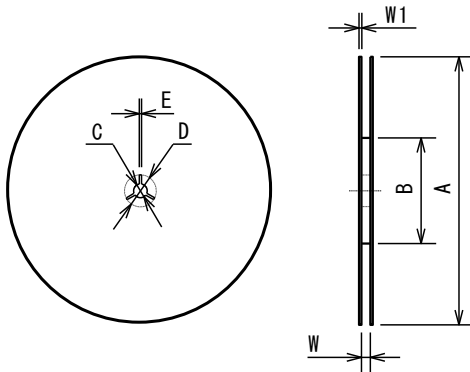
PACKING SPEC

TAPING DIMENSIONS



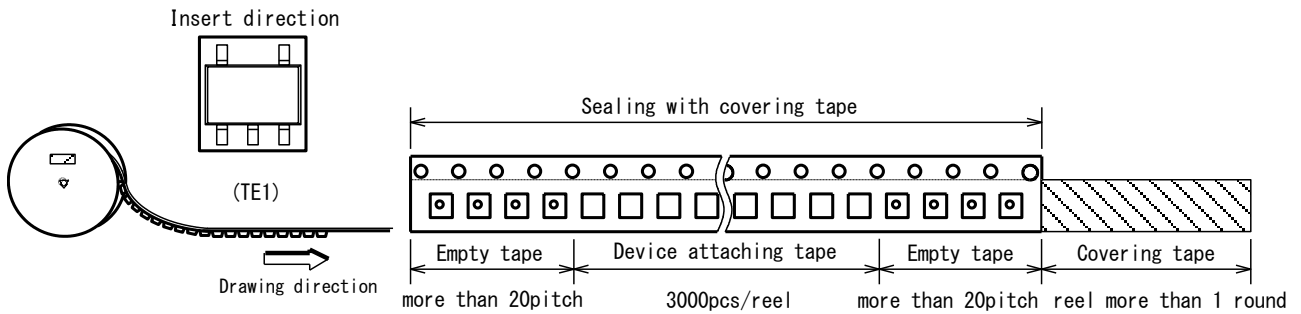
SYMBOL	DIMENSION	REMARKS
A	2.3±0.1	BOTTOM DIMENSION
B	2.5±0.1	BOTTOM DIMENSION
D0	1.55±0.05	
D1	1.05±0.05	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.3±0.1	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

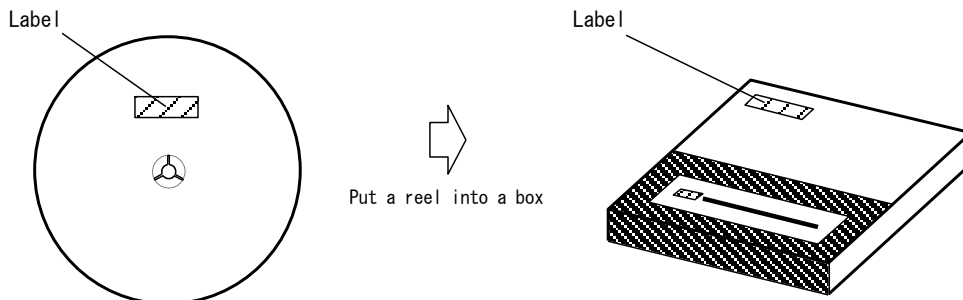


SYMBOL	DIMENSION
A	φ 180±1
B	φ 60±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9±0.5
W1	1.2±0.2

TAPING STATE

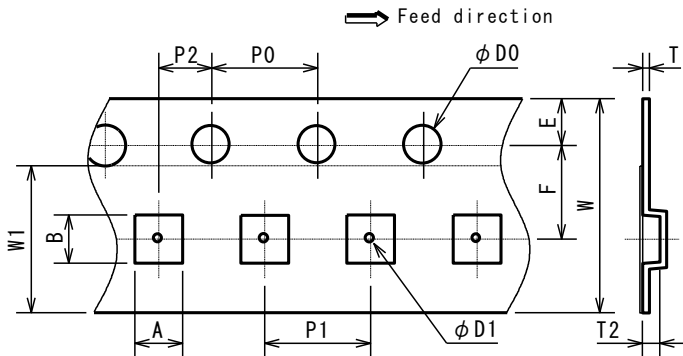


PACKING STATE



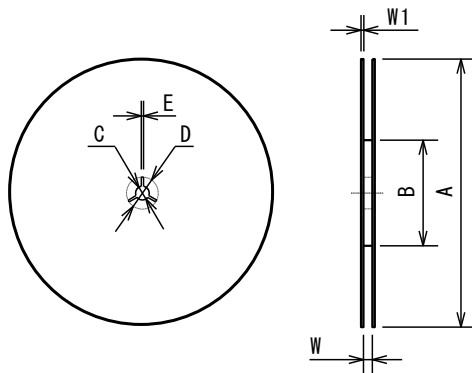
PACKING SPEC

TAPING DIMENSIONS



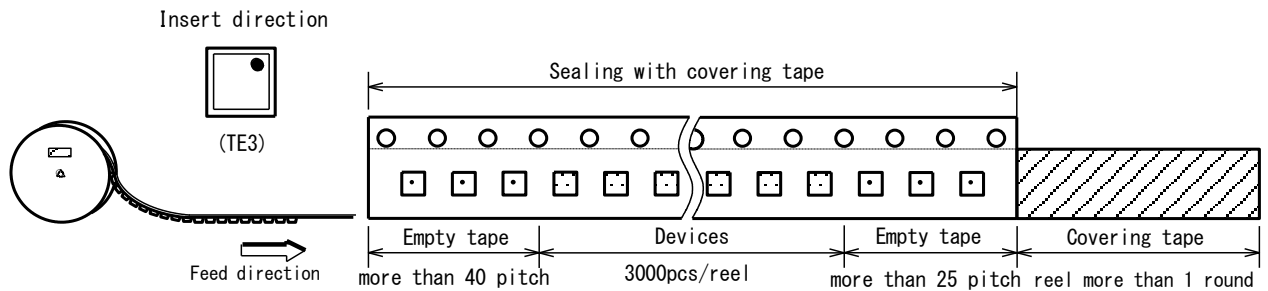
SYMBOL	DIMENSION	REMARKS
A	1.85±0.05	BOTTOM DIMENSION
B	1.85±0.05	BOTTOM DIMENSION
D0	1.5 ^{+0.1} ₀	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

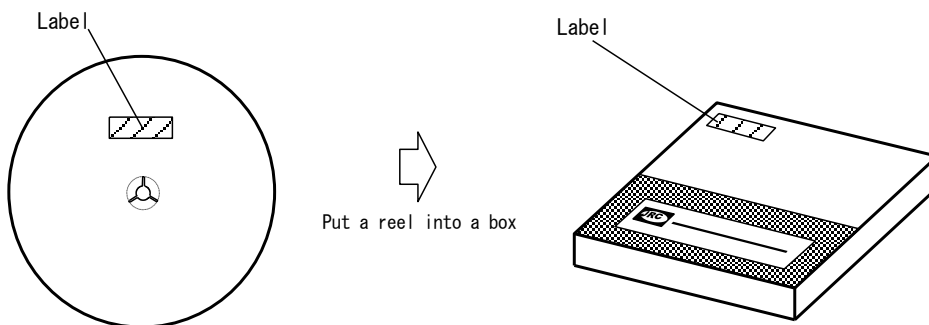


SYMBOL	DIMENSION
A	φ 180 ⁰ _{-1.5}
B	φ 60 ⁺¹ ₀
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9 ^{+0.3} ₀
W1	1.2

TAPING STATE

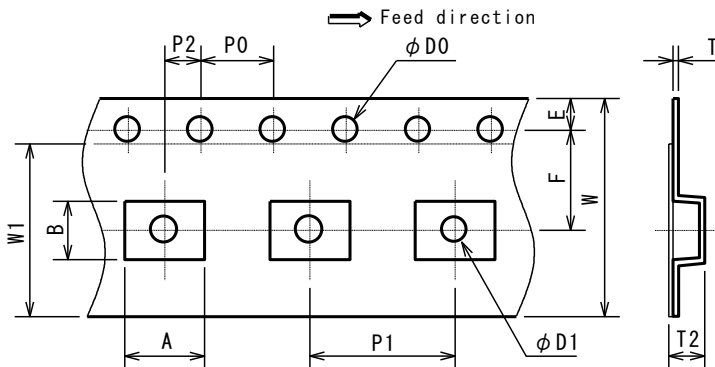


PACKING STATE



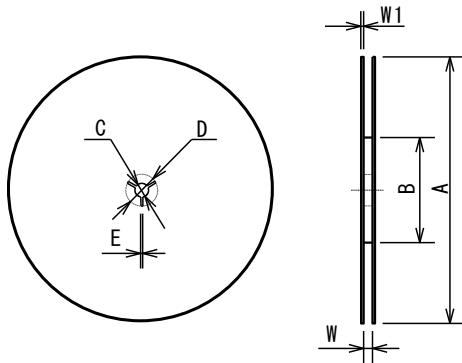
PACKING SPEC

TAPING DIMENSIONS



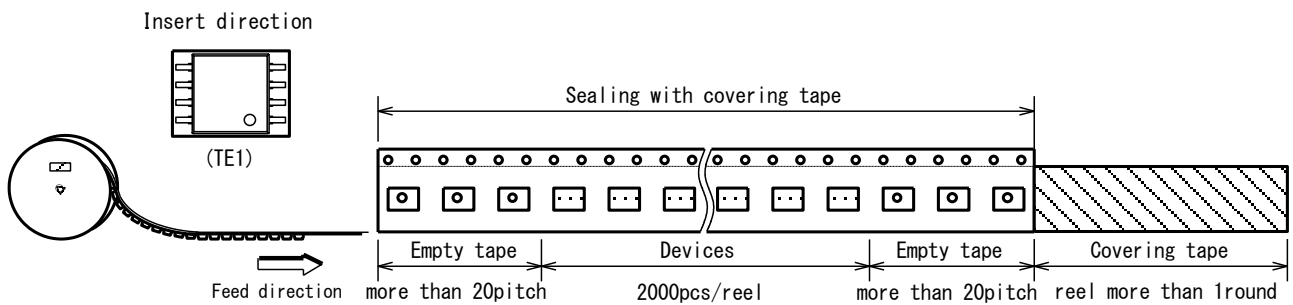
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	1.5 ^{+0.1} ₀	
D1	1.5 ^{+0.1} ₀	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.30±0.05	
T2	1.75 (MAX.)	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

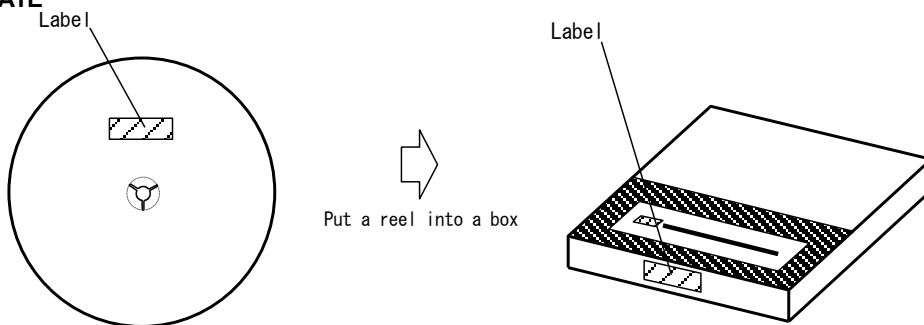


SYMBOL	DIMENSION
A	φ254±2
B	φ100±1
C	φ13±0.2
D	φ21±0.8
E	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE

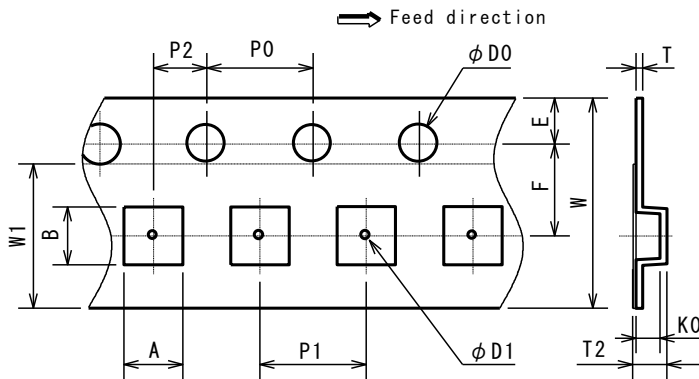


PACKING STATE



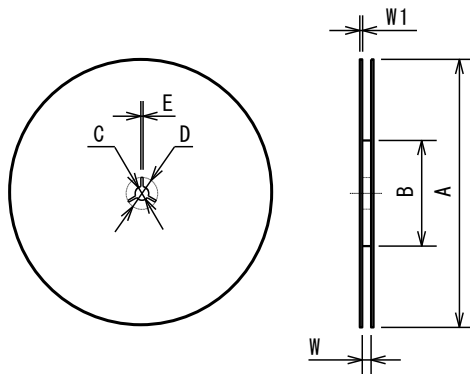
PACKING SPEC

TAPING DIMENSIONS



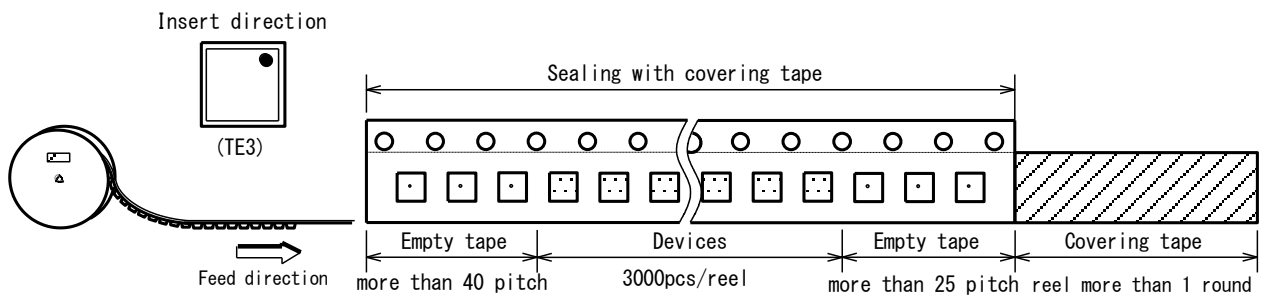
SYMBOL	DIMENSION	REMARKS
A	2.25±0.05	BOTTOM DIMENSION
B	2.25±0.05	BOTTOM DIMENSION
D0	1.5 ^{+0.1} / ₀	
D1	0.5±0.1	
E	1.75±0.1	
F	3.5±0.05	
P0	4.0±0.1	
P1	4.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.00±0.07	
K0	0.65±0.05	
W	8.0±0.2	
W1	5.5	THICKNESS 0.1max

REEL DIMENSIONS

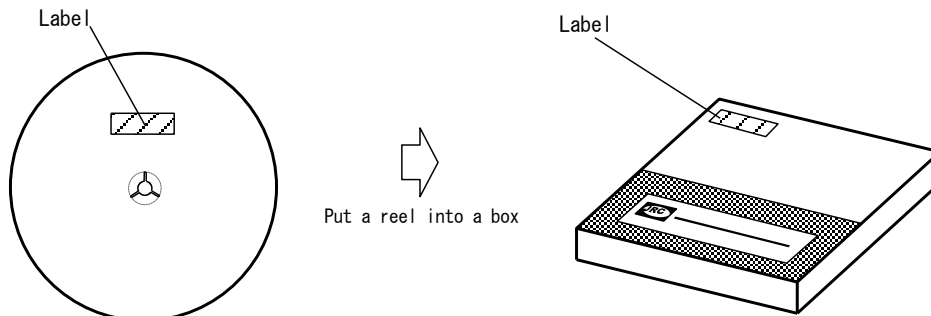


SYMBOL	DIMENSION
A	φ 180 ⁰ / _{-1.5}
B	φ 60 ⁺¹ / ₀
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	9 ^{+0.3} / ₀
W1	1.2

TAPING STATE

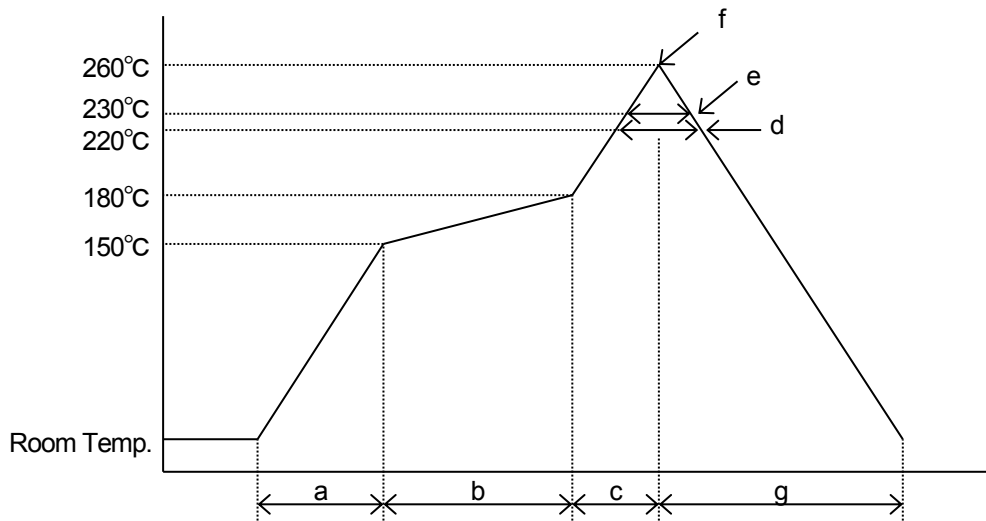


PACKING STATE



RECOMMENDED MOUNTING METHOD

*Recommended reflow soldering procedure



- a: Temperature ramping rate : 1 to 4°C/s
- b: Pre-heating temperature : 150 to 180°C
time : 60 to 120s
- c: Temperature ramp rate : 1 to 4°C/s
- d: 220°C or higher time : Shorter than 60s
- e: 230°C or higher time : Shorter than 40s
- f: Peak temperature : Lower than 260°C
- g: Temperature ramping rate : 1 to 6°C/s

*The temperature indicates at the surface of mold package.

REVISION HISTORY

Date	Revision	Changes
2016/11/30	Ver.0	First edition
2017/5/24	Ver.1	Added information of NJU77232.
2017/10/12	Ver.2	Changed GENERAL DESCRIPTION and APPLICATION
2017/11/10	Ver.3	Corrected ELECTRICAL CHARACTERISTICS

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