

# 4-Channel PMBus Power System Manager Featuring Accurate Input Current and Energy Measurement

## FEATURES

- Sequence, Trim, Margin and Supervise Four Power Supplies
- Manage Faults, Monitor Telemetry and Create Fault Logs
- PMBus™ Compliant Command Set
- Supported by LTpowerPlay® GUI
- Margin or Trim Supplies to Within 0.25% of Target
- Monitor Input Current ( $\pm 1\%$ ) and Accumulate Energy
- Fast OV/UV and OC Supervisors Per Channel
- Coordinate Sequencing and Fault Management Across Multiple ADI PSM Devices
- Automatic Fault Logging to Internal EEPROM
- Operate Autonomously Without Additional Software
- External Temperature and Input Voltage Supervisors
- Accurate Monitoring of Four Output Voltages, Four Output Currents, Four External Temperatures, Input Voltage and Current, and Internal Die Temperature
- Can Be Powered from 3.3V, or 4.5V to 15V
- Pin-Compatible to the LTC2974
- Available in 64-Lead 9mm × 9mm QFN Package and in 63-Lead 6.25mm × 7.5mm BGA Package
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Video and Medical Imaging

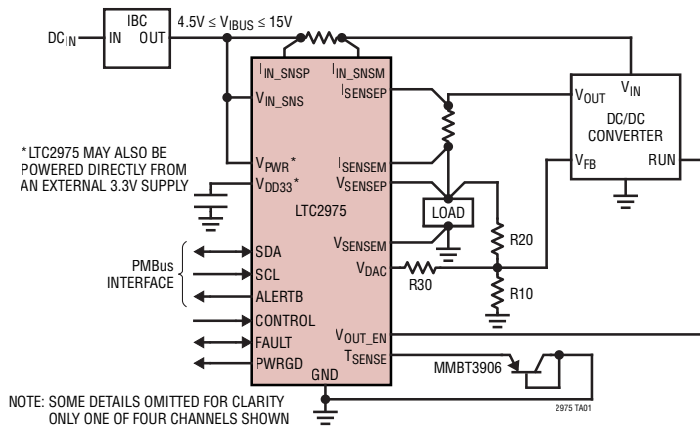
## DESCRIPTION

The **LTC®2975** is a 4-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include over and under current, voltage and temperature threshold limits for four power supply output channels as well as over and under voltage threshold limits for a single power supply input channel. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors four output voltages, four output currents, four external temperatures, input voltage and current, and die temperature. Input power, energy, and output power is also calculated. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple ADI Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

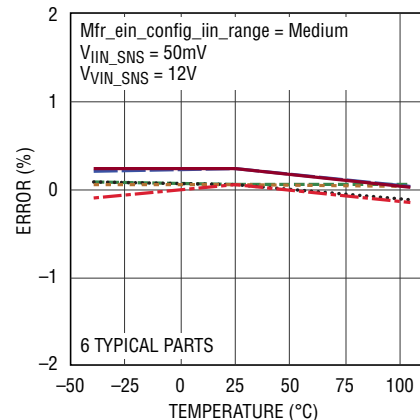
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## TYPICAL APPLICATION

4-Channel PMBus Power System Manager with Input Energy Metering



Power Measurement Error



## TABLE OF CONTENTS

<b>Features</b> .....	1	Input Voltage Commands and Limits .....	48
<b>Applications</b> .....	1	VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT and VIN_UV_FAULT_LIMIT .....	48
<b>Typical Application</b> .....	1	Input Current and Energy .....	49
<b>Description</b> .....	1	Energy Measurement and Reporting .....	49
<b>Absolute Maximum Ratings</b> .....	4	MFR_EIN .....	49
<b>Pin Configuration</b> .....	4	MFR_EIN_CONFIG .....	50
<b>Order Information</b> .....	5	MFR_IIN_CAL_GAIN .....	50
<b>Electrical Characteristics</b> .....	5	MFR_IIN_CAL_GAIN_TC .....	51
<b>PMBus Timing Diagram</b> .....	11	MFR_CLEAR_ENERGY .....	51
<b>Typical Performance Characteristics</b> .....	12	Output Voltage Commands and Limits .....	51
<b>Pin Functions</b> .....	16	VOUT_MODE .....	52
<b>Block Diagram</b> .....	18	VOUT_COMMAND, VOUT_MAX, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_OV_FAULT_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, POWER_GOOD_ON and POWER_GOOD_OFF .....	52
<b>Operation</b> .....	19	MFR_VOUT_DISCHARGE_THRESHOLD .....	52
LTC2975 Operation Overview .....	19	MFR_DAC .....	52
EEPROM .....	20	Output Current Commands and Limits .....	53
AUXFAULTB .....	20	IOUT_CAL_GAIN .....	53
RESETB .....	21	IOUT_OC_FAULT_LIMIT, IOUT_OC_WARN_LIMIT and IOUT_UC_FAULT_LIMIT .....	53
PMBus Serial Digital Interface .....	21	MFR_IOUT_CAL_GAIN_TC .....	53
PMBus .....	21	External Temperature Commands and Limits .....	54
Device Address .....	21	OT_FAULT_LIMIT, OT_WARN_LIMIT, UT_WARN_LIMIT and UT_FAULT_LIMIT .....	55
Processing Commands .....	22	MFR_TEMP_1_GAIN and MFR_TEMP_1_OFFSET .....	55
<b>PMBUS Command Summary</b> .....	25	MFR_T_SELF_HEAT, MFR_IOUT_CAL_GAIN_TAU_INV and MFR_IOUT_CAL_GAIN_THETA .....	55
<b>PMBus Command Description</b> .....	31	Sequencing Timing Limits and Clock Sharing .....	57
Addressing and Write Protect .....	31	TON_DELAY, TON_RISE, TON_MAX_FAULT_LIMIT and TOFF_DELAY .....	57
PAGE .....	31	Watchdog Timer and Power Good .....	58
WRITE_PROTECT .....	32	MFR_PWRGD_EN .....	58
Write Protect Pin .....	32	MFR_RESTART_DELAY .....	58
MFR_PAGE_FF_MASK .....	32	Clock Sharing .....	58
MFR_I2C_BASE_ADDRESS .....	33	MFR_POWERGOOD_ASSERTION_DELAY .....	59
MFR_COMMAND_PLUS .....	33	Watchdog Operation .....	59
MFR_DATA_PLUS0 and MFR_DATA_PLUS1 .....	33	MFR_WATCHDOG_T_FIRST and MFR_WATCHDOG_T .....	59
MFR_STATUS_PLUS0, and MFR_STATUS_PLUS1 .....	33	Fault Responses .....	60
Reading Fault Log Using Command Plus and Mfr_data_plus0 ...	34	Clearing Latched Faults .....	60
Reading Energy Using MFR_COMMAND_PLUS and MFR_DATA_PLUS0 .....	35	VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE .....	60
Peek Operation Using Mfr_data_plus0 .....	35	IOUT_OC_FAULT_RESPONSE and IOUT_UC_FAULT_RESPONSE .....	61
Enabling and Disabling Poke Operations .....	35	OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE and VIN_UV_FAULT_RESPONSE .....	62
Poke Operation Using Mfr_data_plus0 .....	35	TON_MAX_FAULT_RESPONSE .....	63
Command Plus Operations Using Mfr_data_plus1 .....	36	MFR_RETRY_DELAY .....	63
On/Off Control, Margining and Configuration .....	36	MFR_RETRY_COUNT .....	63
OPERATION .....	36	Shared External Faults .....	64
ON_OFF_CONFIG .....	37	MFR_FAULTB0_PROPAGATE and MFR_FAULTB1_PROPAGATE .....	64
MFR_CONFIG_LTC2975 .....	38		
Cascade Sequence ON with Time-Based Sequence OFF .....	39		
MFR_CONFIG2_LTC2975 .....	40		
MFR_CONFIG3_LTC2975 .....	41		
Tracking Supplies On and Off .....	42		
Tracking Implementation .....	44		
MFR_CONFIG_ALL_LTC2975 .....	44		
Programming User EEPROM Space .....	46		
STORE_USER_ALL and RESTORE_USER_ALL .....	46		
Bulk Programming the User EEPROM Space .....	46		
MFR_EE_UNLOCK .....	47		
MFR_EE_ERASE .....	47		
MFR_EE_DATA .....	47		
Response When Part Is Busy .....	48		
MFR_EE Erase and Write Programming Time .....	48		

# TABLE OF CONTENTS

MFR_FAULTB0_RESPONSE and MFR_FAULTB1_RESPONSE.....	64	<b>Applications Information .....</b>	<b>85</b>
Fault Warning and Status .....	65	Overview .....	85
CLEAR_FAULTS .....	65	Powering the LTC2975.....	85
STATUS_BYTE.....	66	Setting Command Register Values.....	85
STATUS_WORD.....	66	Measuring Input Current.....	85
STATUS_VOUT.....	67	Measuring Input Voltage.....	87
STATUS_IOUT.....	67	Measuring Input Power.....	87
STATUS_INPUT.....	67	Measuring Input Energy .....	87
STATUS_TEMPERATURE.....	68	Sequence, Servo, Margin and Restart Operations .....	87
STATUS_CML.....	68	Command Units On or Off.....	87
STATUS_MFR_SPECIFIC.....	68	On Sequencing.....	88
MFR_PADS.....	69	On State Operation.....	88
MFR_COMMON.....	70	Servo Modes.....	88
Telemetry.....	71	DAC Modes.....	88
READ_VIN.....	71	Margining.....	89
READ_IIN.....	71	Off Sequencing.....	89
READ_PIN.....	71	V <sub>OUT</sub> Off Threshold Voltage .....	89
READ_VOUT.....	71	Automatic Restart via MFR_RESTART_DELAY Command and CONTROL Pin.....	89
READ_IOUT.....	72	Fault Management.....	90
MFR_IIN_PEAK.....	72	Output Overvoltage, Undervoltage, Overcurrent and Undercurrent Faults.....	90
MFR_IIN_MIN.....	72	Output Overvoltage, Undervoltage, and Overcurrent Warnings.....	90
MFR_PIN_PEAK.....	72	Configuring the AUXFAULTB Output.....	90
MFR_PIN_MIN.....	72	Multi-Channel Fault Management .....	90
READ_TEMPERATURE_1.....	72	Interconnect Between Multiple ADI Power Managers.....	92
READ_TEMPERATURE_2.....	72	Application Circuits.....	93
READ_POUT.....	73	Trimming and Margining DC/DC Converters with External Feedback Resistors .....	93
MFR_READ_IOUT.....	73	Four-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors .....	94
MFR_IOUT_SENSE_VOLTAGE.....	74	Trimming and Margining DC/DC Converters with a TRIM Pin.....	94
MFR_VIN_PEAK.....	74	Two-Step Resistor and DAC Full-Scale Voltage Selection Procedure for DC/DC Converters with a TRIM Pin .....	95
MFR_VOUT_PEAK.....	74	Measuring Output with a Sense Resistor.....	95
MFR_IOUT_PEAK.....	74	Measuring Output with Inductor DCR.....	95
MFR_TEMPERATURE_1_PEAK.....	74	Single Phase Design Example.....	96
MFR_VIN_MIN.....	74	Measuring Multiphase Currents.....	96
MFR_VOUT_MIN.....	74	Multiphase Design Example.....	96
MFR_IOUT_MIN.....	75	Anti-aliasing Filter Considerations.....	96
MFR_TEMPERATURE_1_MIN.....	75	Sensing Negative Voltages.....	97
Fault Logging.....	75	Connecting the DC1613 USB to I <sup>2</sup> C/SMBus/PMBus Controller to the LTC2975 in System .....	97
Fault Log Operation.....	75	Accurate DCR Temperature Compensation .....	98
MFR_FAULT_LOG_STORE.....	75	LTpowerPlay: An Interactive GUI for Power Managers.....	101
MFR_FAULT_LOG_RESTORE.....	76	PCB Assembly and Layout Suggestions.....	102
MFR_FAULT_LOG_CLEAR.....	76	Bypass Capacitor Placement.....	102
MFR_FAULT_LOG_STATUS.....	76	Exposed Pad Stencil Design.....	102
MFR_FAULT_LOG.....	76	PCB Board Layout .....	102
MFR_FAULT_LOG Read Example.....	79	Unused ADC Sense Inputs .....	102
Identification/Information.....	83	Design Checklist .....	103
CAPABILITY.....	83	<b>Package Description .....</b>	<b>104</b>
User Scratchpad.....	84	<b>Revision History .....</b>	<b>107</b>
USER_DATA_00, USER_DATA_01, USER_DATA_02, USER_DATA_03, USER_DATA_04, MFR_LTC_RESERVED_1 and MFR_LTC_RESERVED_2 .....	84	<b>Typical Application .....</b>	<b>108</b>
PMBUS_REVISION.....	84	<b>Related Parts .....</b>	<b>108</b>
MFR_SPECIAL_ID.....	84		
MFR_SPECIAL_LOT.....	84		
MFR_INFO.....	84		

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

### Supply Voltages:

V <sub>PWR</sub> .....	-0.3V to 15V
V <sub>DD33</sub> .....	-0.3V to 3.6V
V <sub>DD25</sub> .....	-0.3V to 2.75V

### Digital Input/Output Voltages:

ALERTB, SDA, SCL, CONTROL0, CONTROL1, CONTROL2, CONTROL3 .....	-0.3V to 3.6V
PWRGD, SHARE_CLK, WDI/RESETB, WP, FAULTB0, FAULTB1 .....	-0.3V to 3.6V
ASELO, ASEL1 .....	-0.3V to 3.6V

### Analog Voltages:

REFP .....	-0.3V to 1.35V
REFM .....	-0.3V to 0.3V
V <sub>IN_SNS</sub> , V <sub>IN_SNS_CAP</sub> .....	-0.3V to 15V
I <sub>IN_SNSP</sub> , I <sub>IN_SNSM</sub> to V <sub>IN_SNS</sub> .....	-0.3V to 0.3V
V <sub>SENSEP</sub> [3:0] .....	-0.3V to 6V

V <sub>SENSEM</sub> [3:0].....	-0.3V to 6V
I <sub>SENSEP</sub> [3:0].....	-0.3V to 6V
I <sub>SENSEM</sub> [3:0].....	-0.3V to 6V
V <sub>OUT_EN</sub> [3:0], AUXFAULTB .....	-0.3V to 15V
V <sub>DAC</sub> [3:0] .....	-0.3V to 6V
T <sub>SENSE</sub> [3:0] .....	-0.3V to 3.6V
I <sub>IN_SNSP</sub> , I <sub>IN_SNSM</sub> .....	-0.3V to 15V

### Operating Junction Temperature Range:

LTC2975C .....	0°C to 70°C
LTC2975I .....	-40°C to 105°C

### Storage Temperature Range .....

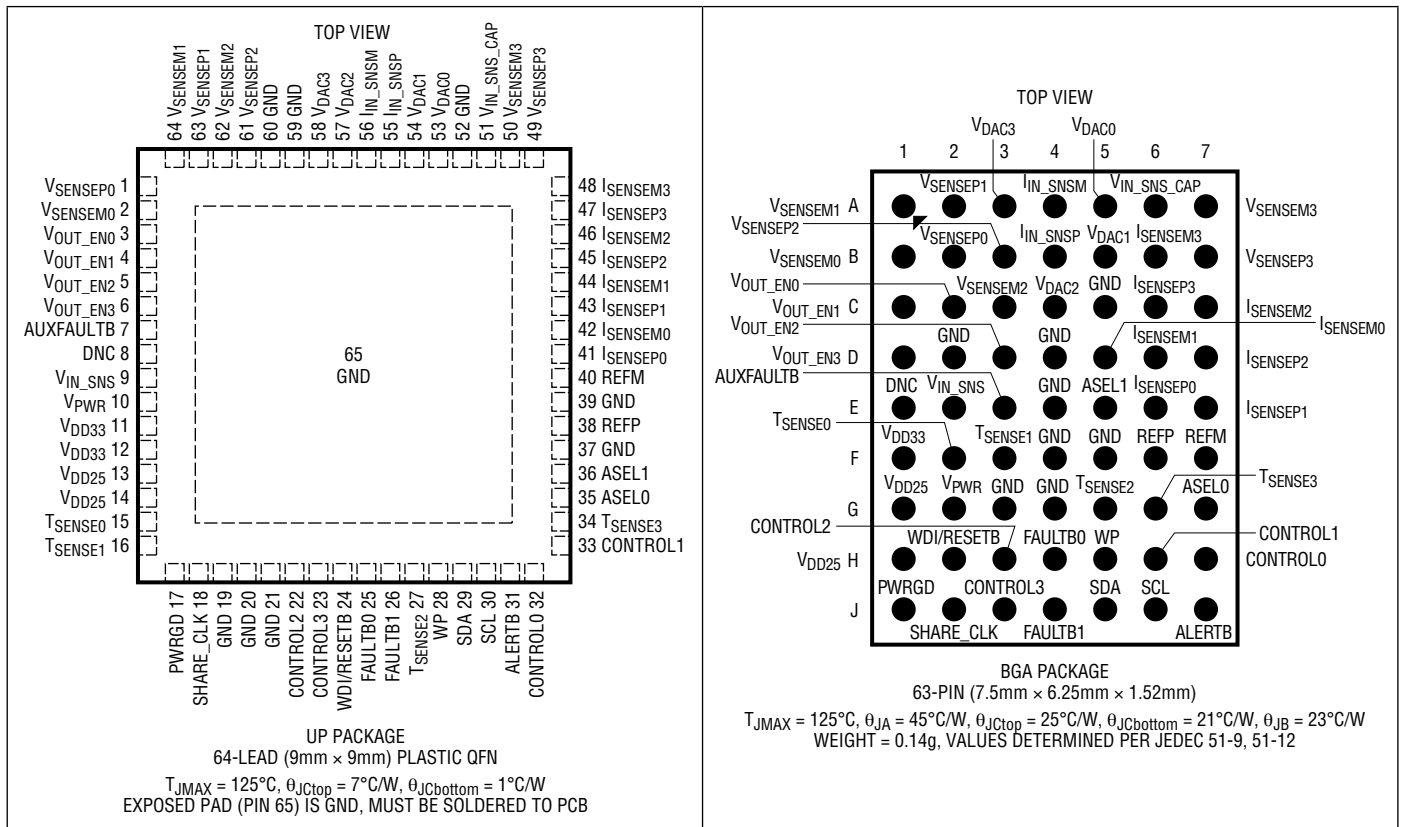
-65°C to 150°C\*

### Maximum Junction Temperature .....

125°C\*

\*See OPERATION section for detailed EEPROM derating information for junction temperatures in excess of 105°C.

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2975CUP#PBF	LTC2975CUP#TRPBF	LTC2975UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2975IUP#PBF	LTC2975IUP#TRPBF	LTC2975UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 105°C

### AUTOMOTIVE PRODUCTS\*\*

LTC2975IUP#WPBF	LTC2975IUP#WTRPBF	LTC2975UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 105°C
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Contact the factory for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

[Tape and reel specifications](#). Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

\*\*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTC2975CY#PBF	SAC305 (RoHS)	LTC2975Y	e1	BGA	3	0°C to 70°C
LTC2975IY#PBF		LTC2975Y				–40°C to 105°C

- Contact the factory for parts specified with wider operating temperature ranges. \*Pad or ball finish code is per IPC/JEDEC J-STD-609.
- [Recommended LGA and BGA PCB Assembly and Manufacturing Procedures](#)
- [LGA and BGA Package and Tray Drawings](#)

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{PWR} = V_{IN\_SNS} = 12\text{V}$ ,  $V_{DD33}$ ,  $V_{DD25}$ , REFP and REFM pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ ,  $C_{VIN\_SNS\_CAP} = 10\text{nF}$  and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Power Supply Characteristics</b>							
$V_{PWR}$	$V_{PWR}$ Supply Input Operating Range	$V_{DD33}$ Floating	● 4.5		15	V	
$I_{PWR}$	$V_{PWR}$ Supply Current	$4.5\text{V} \leq V_{PWR} \leq 15\text{V}$ , $V_{DD33}$ Floating	●	10	13	mA	
$I_{VDD33}$	$V_{DD33}$ Supply Current	$3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$ , $V_{PWR} = V_{DD33}$	●	10	13	mA	
$V_{UVLO\_VDD33}$	$V_{DD33}$ Undervoltage Lockout	$V_{DD33}$ Ramping Up, $V_{PWR} = V_{DD33}$	●	2.25	2.55	2.8	V
	$V_{DD33}$ Undervoltage Lockout Hysteresis			120			mV
$V_{DD33}$	Supply Input Operating Range	$V_{PWR} = V_{DD33}$	●	3.13		3.47	V
	Regulator Output Voltage	$4.5\text{V} \leq V_{PWR} \leq 15\text{V}$	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	$V_{PWR} = 4.5\text{V}$ , $V_{DD33} = 0\text{V}$	●	50	90	140	mA
$V_{DD25}$	Regulator Output Voltage	$3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	$V_{PWR} = V_{DD33} = 3.47\text{V}$ , $V_{DD25} = 0\text{V}$	●	30	55	80	mA
$t_{INIT}$	Initialization Time	Time from $V_{IN}$ applied until the TON_DELAY timer starts		30		ms	
<b>Voltage Reference Characteristics</b>							
$V_{REF}$	Output Voltage (Note 3)	$V_{REF} = V_{REFP} - V_{REFM}$ , $0 < I_{REFP} < 100\mu\text{A}$	●	1.220	1.232	1.244	V
	Temperature Coefficient			3			ppm/°C
	Hysteresis	(Note 4)		100			ppm

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>ADC Characteristics</b>							
$V_{IN\_ADC}$	Voltage Sense Input Range	Differential Voltage: $V_{IN\_ADC} = (V_{SENSEPN} - V_{SENSEMN})$	●	0	6	V	
		Single-Ended Voltage: $V_{SENSEMN}$	●	-0.1	0.1	V	
	Current Sense Input Range	Single-Ended Voltage: $I_{SENSEPN}$ , $I_{SENSEMN}$	●	-0.1	6	V	
		Differential Current Sense Voltage: $V_{IN\_ADC} = (I_{SENSEPN} - I_{SENSEMN})$	●	-170	170	mV	
$N\_ADC$	Voltage Sense Resolution (Note 5)	$0\text{V} \leq V_{IN\_ADC} \leq 6\text{V}$ , READ_VOUT		122		$\mu\text{V}/\text{LSB}$	
$TUE\_ADC\_VOLT\_SNS$	Total Unadjusted Error (Note 3)	Voltage Sense Inputs $V_{IN\_ADC} \geq 1\text{V}$	●		$\pm 0.25$	% of Reading	
		Voltage Sense Inputs $0 \leq V_{IN\_ADC} \leq 1\text{V}$	●		$\pm 2.5$	mV	
$TUE\_ADC\_CURR\_SNS$	Total Unadjusted Error (Note 3)	Current Sense Inputs $20\text{mV} \leq  V_{IN\_ADC}  \leq 170\text{mV}$	●		$\pm 0.3$	% of Reading	
		Current Sense Inputs $ V_{IN\_ADC}  \leq 20\text{mV}$	●		$\pm 60$	$\mu\text{V}$	
$V_{OS\_ADC}$	Offset Error	$I_{SENSEPN}$ and $I_{SENSEMN}$ Inputs, $V_{OS} \cdot I_{OUT\_CAL\_GAIN}$ , $I_{OUT\_CAL\_GAIN} = 1000\text{m}\Omega$	●		$\pm 35$	$\mu\text{V}$	
$t_{CONV\_ADC}$	Conversion Time	$V_{SENSEPN}$ , $V_{SENSEMN}$ , $V_{IN\_SNS}$ Inputs (Note 6)		6.15		ms	
		$I_{SENSEPN}$ and $I_{SENSEMN}$ Inputs (Note 6)		24.6		ms	
		Internal Temperature (READ_TEMPERATURE_2) (Note 6)		24.6		ms	
$t_{UPDATE\_ADC}$	Update Time	Mfr_ein_config_hd = 0 (Note 6)		190		ms	
		Mfr_ein_config_hd = 1 (Note 6)		500		ms	
$f_{IN\_ADC}$	Input Sampling Frequency			62.5		kHz	
<b>Sense Input Current Characteristics (Note 13)</b>							
$I_{IN\_VSENSE}$	Input Current	$V_{SENSEPN}$ and $V_{SENSEMN}$ Inputs	●		$\pm 15$	$\mu\text{A}$	
	Differential Input Current	$V_{SENSEPN}$ and $V_{SENSEMN}$ Inputs, $V_{IN\_DIFF} = 6\text{V}$	●		$\pm 30$	$\mu\text{A}$	
$I_{IN\_ISENSE}$	Input Current	$I_{SENSEPN}$ and $I_{SENSEMN}$ Inputs	●		$\pm 3$	$\mu\text{A}$	
	Differential Input Current	$I_{SENSEPN}$ and $I_{SENSEMN}$ Inputs, $ V_{IN\_DIFF}  = 170\text{mV}$	●		$\pm 5$	$\mu\text{A}$	
<b>DAC Output Characteristics</b>							
$N\_VDAC$	Resolution			10		Bits	
$V_{FS\_VDAC}$	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF	●	1.3	1.38	1.44	V
		DAC Polarity = 1	●	2.5	2.65	2.77	V
$INL\_VDAC$	Integral Nonlinearity	(Note 7)	●		$\pm 2$	LSB	
$DNL\_VDAC$	Differential Nonlinearity	(Note 7)	●		$\pm 2.4$	LSB	
$V_{OS\_VDAC}$	Offset Voltage	(Note 7)	●		$\pm 15$	mV	
$V_{DAC}$	Load Regulation	$V_{DACn} = 2.65\text{V}$ , $I_{VDACn}$ Sourcing = 2mA		100		ppm/mA	
		$V_{DACn} = 0.1\text{V}$ , $I_{VDACn}$ Sinking = 2mA		100		ppm/mA	
	PSRR	DC: $3.13\text{V} \leq V_{DD33} \leq 3.47\text{V}$ , $V_{PWR} = V_{DD33}$		60		dB	
	Leakage Current	$V_{DACn}$ Hi-Z, $0\text{V} \leq V_{DACn} \leq 6\text{V}$	●		$\pm 100$	nA	
	Short-Circuit Current Low	$V_{DACn}$ Shorted to GND	●	-12	-4	mA	
	Short-Circuit Current High	$V_{DACn}$ Shorted to $V_{DD33}$	●	4	12	mA	
$C_{OUT}$	Output Capacitance	$V_{DACn}$ Hi-Z		10		pF	
$t_{S\_VDAC}$	DAC Output Update Rate	Fast Servo Mode		250		$\mu\text{s}$	

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Voltage Supervisor Characteristics</b>							
$V_{IN\_VS}$	Input Voltage Range (Programmable)	$V_{IN\_VS} = (V_{SENSEPN} - V_{SENSEMn})$ Low Resolution Mode	●	0	6	V	
		High Resolution Mode	●	0	3.8	V	
		Single-Ended Voltage: $V_{SENSEMn}$	●	-0.1	0.1	V	
$N\_VS$	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode		4		mV/LSB	
		0V to 6V Range: Low Resolution Mode		8		mV/LSB	
$TUE\_VS$	Total Unadjusted Error	$2\text{V} \leq V_{IN\_VS} \leq 6\text{V}$ , Low Resolution Mode	●		$\pm 1.25$	% of Reading	
		$1.5\text{V} < V_{IN\_VS} \leq 3.8\text{V}$ , High Resolution Mode	●		$\pm 1.0$	% of Reading	
		$0.8\text{V} \leq V_{IN\_VS} \leq 1.5\text{V}$ , High Resolution Mode	●		$\pm 1.5$	% of Reading	
$t_{S\_VS}$	Update Period			12.21		$\mu\text{s}$	
<b>Current Supervisor Characteristics</b>							
$V_{IN\_CS}$	Current Sense Input Range	Single-Ended Voltage: $I_{SENSEPN}$ , $I_{SENSEMn}$	●	-0.1	6	V	
		Differential Voltage: $V_{IN\_CS} = (I_{SENSEPN} - I_{SENSEMn})$	●	-170	170	mV	
$N\_CS$	Current Sense Resolution	$I_{OUT\_OC\_FAULT\_LIMIT} \cdot I_{OUT\_CAL\_GAIN}$ $I_{OUT\_UC\_FAULT\_LIMIT} \cdot I_{OUT\_CAL\_GAIN}$		400		$\mu\text{V/LSB}$	
$TUE\_CS$	Total Unadjusted Error	$50\text{mV} \leq  V_{IN\_CS}  \leq 170\text{mV}$	●		$\pm 3$	% of Reading	
		$ V_{IN\_CS}  < 50\text{mV}$	●		$\pm 1.5$	mV	
$V_{OS\_CS}$	Offset Error	$V_{IN\_CS} = 0$	●		$\pm 600$	$\mu\text{V}$	
$t_{S\_CS}$	Update Period			12.21		$\mu\text{s}$	
<b><math>V_{IN\_SNS}</math> Input Characteristics</b>							
$V_{IN\_SNS}$	$V_{IN\_SNS}$ Input Voltage Range	(Note 12)	●	0	15	V	
$I_{VIN\_SNS}$	$V_{IN\_SNS}$ Input Current	$V_{VIN\_SNS} = 4.5\text{V}$	●	80	140	200	$\mu\text{A}$
		$V_{VIN\_SNS} = 12\text{V}$	●	150	250	350	$\mu\text{A}$
		$V_{VIN\_SNS} = 15\text{V}$	●	180	300	420	$\mu\text{A}$
$TUE_{VIN\_SNS}$	$V_{IN\_ON}$ , $V_{IN\_OFF}$ Threshold Total Unadjusted Error	$4.5\text{V} \leq V_{VIN\_SNS} \leq 8\text{V}$	●		$\pm 2.0$	% of Reading	
		$V_{VIN\_SNS} > 8\text{V}$	●		$\pm 1.0$	% of Reading	
$TUE_{VIN}$	READ_VIN Total Unadjusted Error	$4.5\text{V} \leq V_{VIN\_SNS} \leq 15\text{V}$ (Note 12)	●		$\pm 0.5$	% of Reading	
<b>DAC Soft-Connect Comparator Characteristics</b>							
$V_{OS\_CMP}$	Offset Voltage	$V_{DACPn} = 0.2\text{V}$	●	$\pm 1$	$\pm 18$	mV	
		$V_{DACPn} = 1.3\text{V}$	●	$\pm 2$	$\pm 26$	mV	
		$V_{DACPn} = 2.65\text{V}$	●	$\pm 3$	$\pm 52$	mV	
<b>Input Current Sense Characteristics</b>							
$V_{IIN}$	Common Mode Input Range	$V_{IIN\_SNSP} = V_{IIN\_SNSM}$ (Note 12)	●	4.5	15	V	
$I_{IIN}$	$I_{IIN\_SNSP}$ , $I_{IIN\_SNSM}$ Input Current	$V_{IIN\_SNSP} = V_{IIN\_SNSM} = V_{IIN\_SNS}$	●	0.5	2	$\mu\text{A}$	
$FS_{IIN}$	Full-Scale Input Current Sense Voltage Range	Referred to $(V_{IIN\_SNSP} - V_{IIN\_SNSM})$ High Range	●	-100	100	mV	
		Medium Range	●	-50	50	mV	
		Low Range	●	-20	20	mV	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{PWR} = V_{IN\_SNS} = 12\text{V}$ ,  $V_{DD33}$ ,  $V_{DD25}$ , REFP and REFM pins floating, unless otherwise indicated.  $C_{VDD33} = 100\text{nF}$ ,  $C_{VDD25} = 100\text{nF}$ ,  $C_{VIN\_SNS\_CAP} = 10\text{nF}$  and  $C_{REF} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
TUE_IIN	Total Unadjusted Error	$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 100\text{mV}$ , High Range	●		±0.6	% of Reading	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 50\text{mV}$ , Medium Range	●		±0.65	% of Reading	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 20\text{mV}$ , Low Range	●		±0.75	% of Reading	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 20\text{mV}$ , High Range	●		±1	% of Reading	
CMRR_IIN	DC CMRR	$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 15\text{mV}$ , Medium Range	●		±1	% of Reading	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 10\text{mV}$ , Low Range	●		±1	% of Reading	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 0\text{mV}$ , High Range	●		±100	μV	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 0\text{mV}$ , Medium Range	●		±75	μV	
tCONV_IIN	Conversion Time	$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 0\text{mV}$ , Low Range	●		±50	μV	
		$ V_{IN\_SNSP} - V_{IN\_SNSM}  = 0\text{mV}$ , Low Range BGA Only	●		±65	μV	
tUPDATE	Update Rate	$4.5\text{V} \leq V_{IN\_SNSP} = V_{IN\_SNS} \leq 15\text{V}$ $ V_{IN\_SNSP} - V_{IN\_SNSM}  = 100\text{mV}$ High Range	●	85		dB	
		$V_{IN\_SNSP} = V_{IN\_SNS} = 12\text{V} \pm 100\text{mV}$ $f = 62.5\text{kHz}$			85	dB	
tCONV_TSENSE	Conversion Time	For One Channel, (Total Latency For All Channels Is $4 \cdot 66\text{ms}$ )		66		ms	
I <sub>TSENSE_HI</sub>	T <sub>SENSE</sub> High Level Current		●	-90	-64	-40	μA
I <sub>TSENSE_LOW</sub>	T <sub>SENSE</sub> Low Level Current		●	-5.5	-4	-2.5	μA
TUE_TS	Total Unadjusted Error	Ideal Diode Assumed	●		±3	°C	
N_TS	Maximum Ideality Factor	READ_TEMPERATURE_1 = 175°C MFR_TEMP_1_GAIN = 1/N_TS			1.10		
<b>Internal Temperature Sensor Characteristics (READ_TEMPERATURE_2)</b>							
TUE_TS2	Total Unadjusted Error				±1	°C	
<b>V<sub>OUT</sub> Enable Output (V<sub>OUT_EN</sub> [3:0]) Characteristics</b>							
V <sub>VOUT_ENn</sub>	Output High Voltage	$I_{VOUT\_ENn} = -5\mu\text{A}$ , $V_{DD33} = 3.13\text{V}$	●	10	13	14.7	V
I <sub>VOUT_ENn</sub>	Output Sourcing Current	$V_{VOUT\_ENn}$ Pull-Up Enabled, $V_{VOUT\_ENn} = 1\text{V}$	●	-5	-7	-9	μA
	Output Sinking Current	Strong Pull-Down Enabled, $V_{VOUT\_ENn} = 0.4\text{V}$	●	2.5	5	8	mA
	Output Leakage Current	Weak Pull-Down Enabled, $V_{VOUT\_ENn} = 0.4\text{V}$	●	33	50	65	μA
V <sub>VOUT_VALID</sub>	Minimum $V_{DD33}$ when $V_{OUT\_ENn}$ Valid	$V_{VOUT\_ENn} \leq 0.4\text{V}$	●		1.1	V	
<b>General Purpose Output (AUXFAULTB) Characteristics</b>							
V <sub>AUXFAULTB</sub>	Output High Voltage	$I_{AUXFAULTB} = -5\mu\text{A}$ , $V_{DD33} = 3.13\text{V}$	●	10	13	14.7	V
I <sub>AUXFAULTB</sub>	Output Sourcing Current	AUXFAULTB Pull-Up Enabled, $V_{AUXFAULTB} = 1\text{V}$	●	-5	-7	-9	μA
	Output Sinking Current	Strong Pull-Down Enabled, $V_{AUXFAULTB} = 0.4\text{V}$	●	2.5	5	8	mA
	Output Leakage Current	Internal Pull-Up Disabled, $0\text{V} \leq V_{AUXFAULTB} \leq 15\text{V}$	●			±1	μA
<b>Energy Meter Characteristics</b>							
TUE_ETB	Energy Meter Time-Base Error		●		±1.5	% of Reading	
TUE_PIN	READ_PIN Total Unadjusted Error	$V_{IN\_SNSP} - V_{IN\_SNSM} = 50\text{mV}$ , Medium Range	●		±1	% of Reading	
TUE_EIN	Energy Meter Total Unadjusted Error	$V_{IN\_SNSP} - V_{IN\_SNSM} = 50\text{mV}$ , Medium Range	●		±2.5	% of Reading	



**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_J = 25^\circ\text{C}$ .  $V_{\text{PWR}} = V_{\text{IN\_SNS}} = 12\text{V}$ ,  $V_{\text{DD33}}$ ,  $V_{\text{DD25}}$ , REFP and REFM pins floating, unless otherwise indicated.  $C_{\text{VDD33}} = 100\text{nF}$ ,  $C_{\text{VDD25}} = 100\text{nF}$ ,  $C_{\text{VIN\_SNS\_CAP}} = 10\text{nF}$  and  $C_{\text{REF}} = 100\text{nF}$ . (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>EEPROM Characteristics</b>						
Endurance	(Notes 8, 11)	$0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations	●	10,000		Cycles
Retention	(Notes 8, 11)	$T_J < 105^\circ\text{C}$	●	20		Years
$t_{\text{MASS\_WRITE}}$	Mass Write Operation Time (Note 9)	STORE_USER_ALL, $0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operations	●		440 4100	ms
<b>Digital Inputs SCL, SDA, CONTROL0, CONTROL1, CONTROL2, CONTROL3, WDI/RESETB, FAULTB0, FAULTB1, WP</b>						
$V_{\text{IH}}$	High Level Input Voltage	FAULTB0, FAULTB1, SDA, SCL, WDI/RESETB, WP	●	2.1		V
		CONTROL $n$ Only	●	1.85		V
$V_{\text{IL}}$	Low Level Input Voltage	FAULTB0, FAULTB1, SDA, SCL, WDI/RESETB, WP	●		1.5	V
		CONTROL $n$ Only	●		1.6	V
$V_{\text{HYST}}$	Input Hysteresis			20		mV
$I_{\text{LEAK}}$	Input Leakage Current	$0\text{V} \leq V_{\text{PIN}} \leq 3.6\text{V}$	●		$\pm 2$	$\mu\text{A}$
$t_{\text{SP}}$	Pulse Width of Spike Suppressed	FAULTB0, FAULTB1, CONTROL $n$			10	$\mu\text{s}$
		SDA, SCL			98	ns
$t_{\text{FAULT\_MIN}}$	Minimum Low Pulse Width for Externally Generated Faults			180		ms
$t_{\text{RESETB}}$	Pulse Width to Assert Reset	$V_{\text{WDI/RESETB}} \leq 1.5\text{V}$	●	300		$\mu\text{s}$
$t_{\text{WDI}}$	Pulse Width to Reset Watchdog Timer	$V_{\text{WDI/RESETB}} \leq 1.5\text{V}$	●	0.3	200	$\mu\text{s}$
$f_{\text{WDI}}$	Watchdog Timer Interrupt Input Frequency		●		1	MHz
$C_{\text{IN}}$	Input Capacitance				10	pF
<b>Digital Input SHARE_CLK</b>						
$V_{\text{IH}}$	High Level Input Voltage		●	1.6		V
$V_{\text{IL}}$	Low Level Input Voltage		●		0.8	V
$f_{\text{SHARE\_CLK\_IN}}$	Input Frequency Operating Range		●	90	110	kHz
$t_{\text{LOW}}$	Assertion Low Time	$V_{\text{SHARE\_CLK}} < 0.8\text{V}$	●	0.825	1.11	$\mu\text{s}$
$t_{\text{RISE}}$	Rise Time	$V_{\text{SHARE\_CLK}} < 0.8\text{V}$ to $V_{\text{SHARE\_CLK}} > 1.6\text{V}$	●		450	ns
$I_{\text{LEAK}}$	Input Leakage Current	$0\text{V} \leq V_{\text{SHARE\_CLK}} \leq V_{\text{DD33}} + 0.3\text{V}$	●		$\pm 1$	$\mu\text{A}$
$C_{\text{IN}}$	Input Capacitance				10	pF
<b>Digital Outputs SDA, ALERTB, SHARE_CLK, FAULTB0, FAULTB1, PWRGD</b>						
$V_{\text{OL}}$	Digital Output Low Voltage	$I_{\text{SINK}} = 3\text{mA}$	●		0.4	V
$f_{\text{SHARE\_CLK\_OUT}}$	Output Frequency Operating Range	5.49k $\Omega$ Pull-Up to $V_{\text{DD33}}$	●	90	100 110	kHz
<b>Digital Inputs ASELO,ASEL1</b>						
$V_{\text{IH}}$	Input High Threshold Voltage		●	$V_{\text{DD33}} - 0.5$		V
$V_{\text{IL}}$	Input Low Threshold Voltage		●		0.5	V
$I_{\text{IH,IL}}$	High, Low Input Current	ASEL[1:0] = 0, $V_{\text{DD33}}$	●		$\pm 95$	$\mu\text{A}$
$I_{\text{HIZ}}$	Hi-Z Input Current		●		$\pm 24$	$\mu\text{A}$
$C_{\text{IN}}$	Input Capacitance				10	pF
<b>Serial Bus Timing Characteristics</b>						
$f_{\text{SCL}}$	Serial Clock Frequency (Note 10)		●	10	400	kHz
$t_{\text{LOW}}$	Serial Clock Low Period (Note 10)		●	1.3		$\mu\text{s}$
$t_{\text{HIGH}}$	Serial Clock High Period (Note 10)		●	0.6		$\mu\text{s}$

## ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t <sub>BUF</sub>	Bus Free Time Between Stop and Start (Note 10)		1.3			μs
t <sub>HD,STA</sub>	Start Condition Hold Time (Note 10)		600			ns
t <sub>SU,STA</sub>	Start Condition Setup Time (Note 10)		600			ns
t <sub>SU,STO</sub>	Stop Condition Setup Time (Note 10)		600			ns
t <sub>HD,DAT</sub>	Data Hold Time (LTC2975 Receiving Data) (Note 10)		0			ns
	Data Hold Time (LTC2975 Transmitting Data) (Note 10)		300		900	ns
t <sub>SU,DAT</sub>	Data Setup Time (Note 10)		100			ns
t <sub>SP</sub>	Pulse Width of Spike Suppressed (Note 10)			98		ns
t <sub>TIMEOUT_BUS</sub>	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0		25	35	ms
		Mfr_config_all_longer_pmbus_timeout = 1		200	280	ms
<b>Additional Digital Timing Characteristics</b>						
t <sub>OFF_MIN</sub>	Minimum Off-Time for Any Channel			100		ms

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the V<sub>DD33</sub> pin only, connect V<sub>PWR</sub> and V<sub>DD33</sub> pins together.

**Note 3:** The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage (V<sub>REF</sub>) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high-resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

**Note 4:** Hysteresis in the output voltage is created by package stress that differs depending on whether IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

**Note 5:** The current sense resolution is determined by the L11 format, the value of IOUT\_CAL\_GAIN, and the magnitude of the current being measured. See Table 5 for details.

**Note 6:** The nominal time between successive ADC conversions (latency of the ADC) for any given channel is t<sub>UPDATE\_ADC</sub>.

**Note 7:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

**Note 8:** EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

**Note 9:** The LTC2975 will not acknowledge any PMBus commands, except for MFR\_COMMON, when a STORE\_USER\_ALL command is being executed. See also OPERATION section.

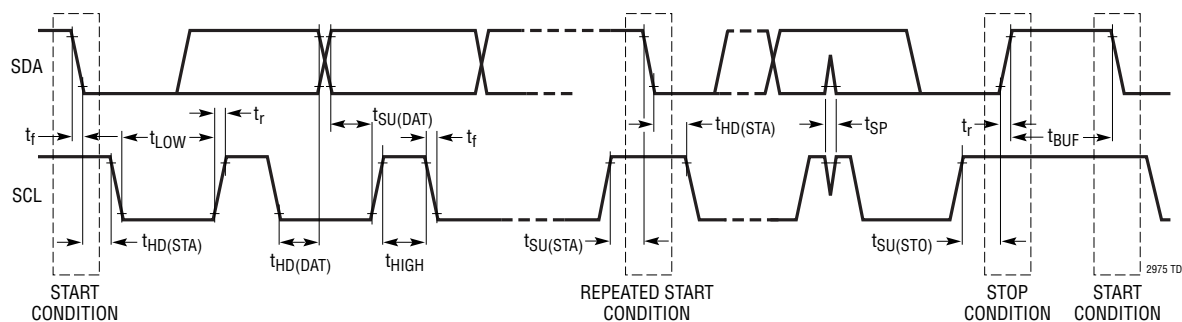
**Note 10:** Maximum capacitive load, C<sub>B</sub>, for SCL and SDA is 400pF. Data and clock rise time (t<sub>r</sub>) and fall time (t<sub>f</sub>) are: (20 + 0.1 • C<sub>B</sub>) (ns) < t<sub>r</sub> < 300ns and (20 + 0.1 • C<sub>B</sub>) (ns) < t<sub>f</sub> < 300ns. C<sub>B</sub> = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V<sub>I0</sub>, is 3.13V < V<sub>I0</sub> < 3.6V.

**Note 11:** EEPROM endurance and retention will be degraded when T<sub>J</sub> > 105°C.

**Note 12:** While READ\_VIN operates with 0V ≤ V<sub>IN\_SNS</sub> ≤ 15V, the valid READ\_IIN, READ\_PIN, and MFR\_EIN operating range is 4.5V ≤ V<sub>IN\_SNS</sub> ≤ 15V.

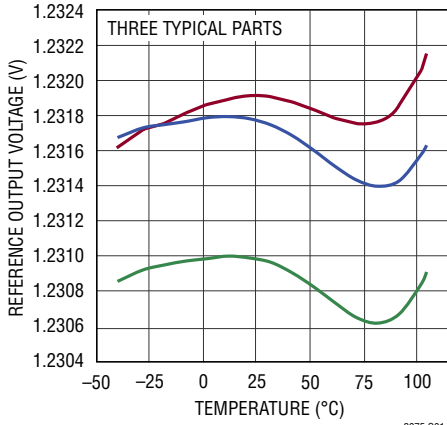
**Note 13:** V<sub>SENSE</sub> and I<sub>SENSE</sub> input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as (I<sup>+</sup> – I<sup>–</sup>) where I<sup>+</sup> is the current into the positive device pin and I<sup>–</sup> is the current into the negative device pin.

# PMBUS TIMING DIAGRAM

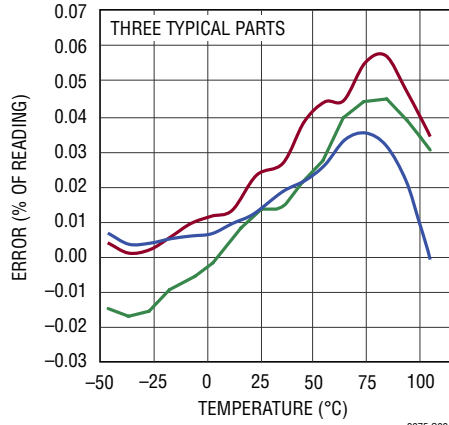


TYPICAL PERFORMANCE CHARACTERISTICS

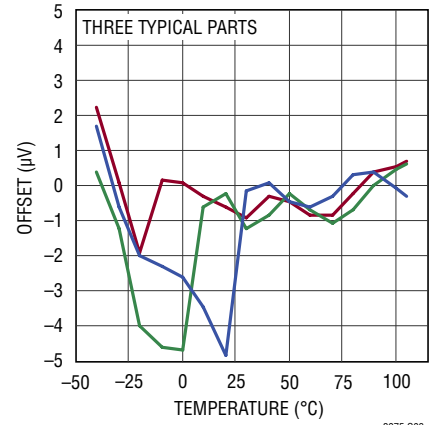
Reference Voltage vs Temperature



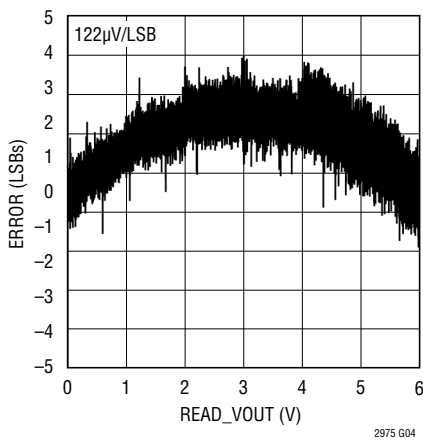
ADC READ\_VOUT ADC Total Unadjusted Error vs Temperature



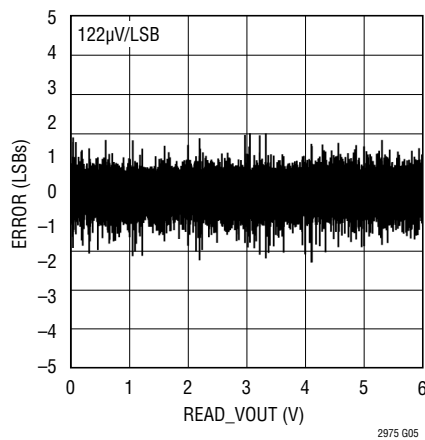
ADC READ\_IOUT Input Referred Offset Voltage vs Temperature



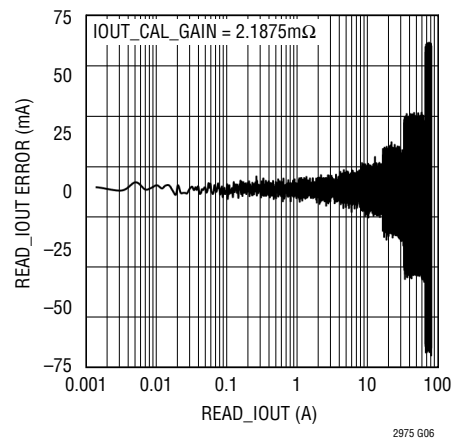
ADC READ\_VOUT-INL



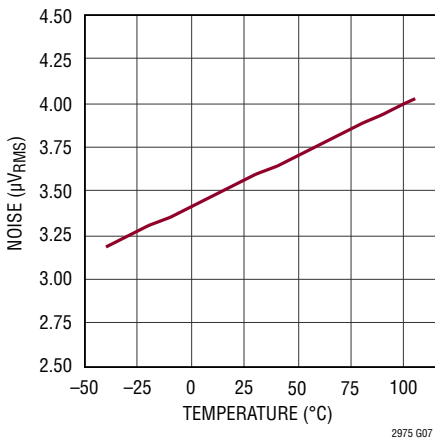
ADC READ\_VOUT-DNL



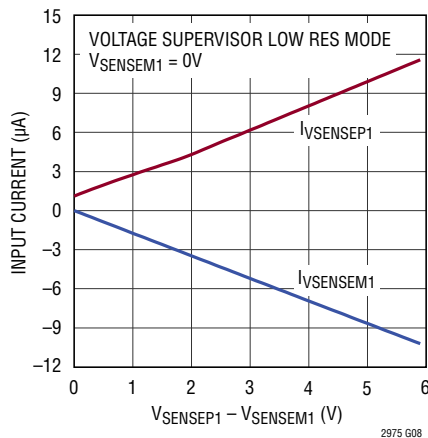
ADC READ\_IOUT Error vs READ\_IOUT



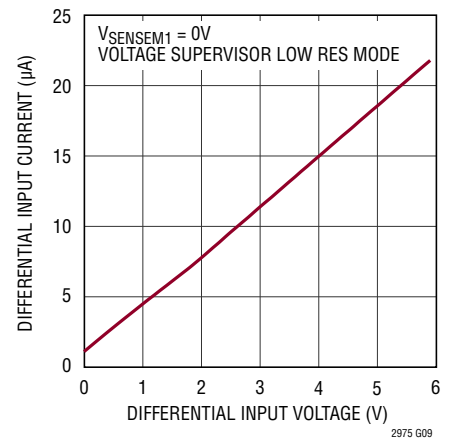
ADC READ\_IOUT Input Referred Noise vs Temperature



Voltage Sense Input Currents vs Differential Input Voltage

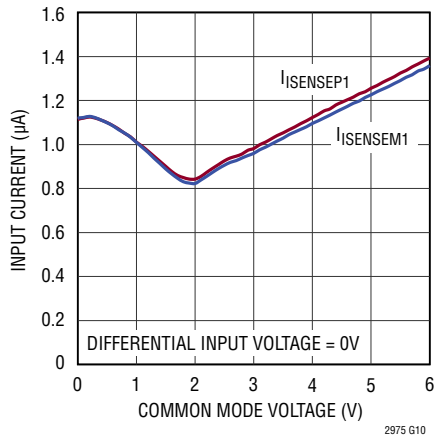


Voltage Sense Differential Input Current vs Differential Input Voltage

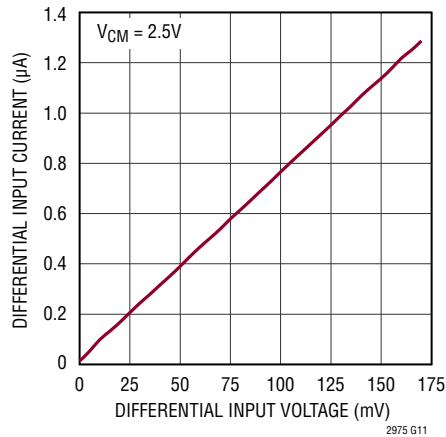


# TYPICAL PERFORMANCE CHARACTERISTICS

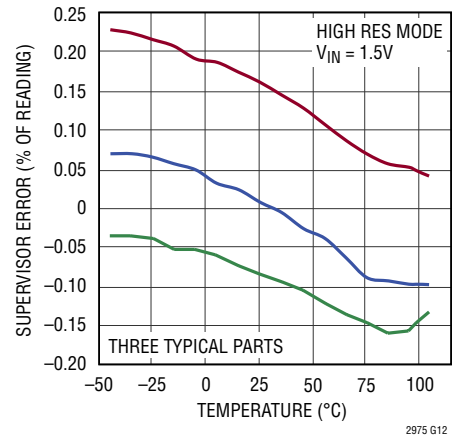
**Current Sense Input Current vs Common Mode Voltage**



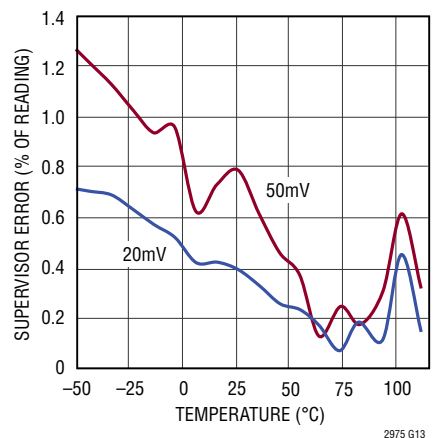
**Current Sense Differential Input Current vs Differential Input Voltage**



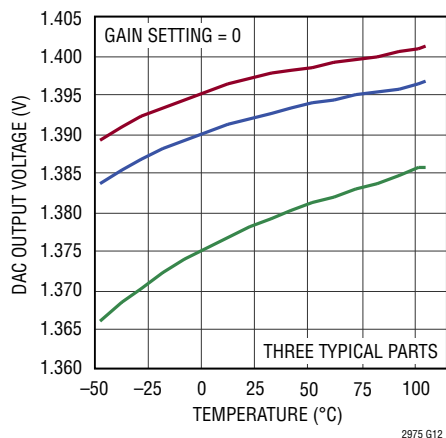
**Voltage Supervisor Total Unadjusted Error vs Temperature**



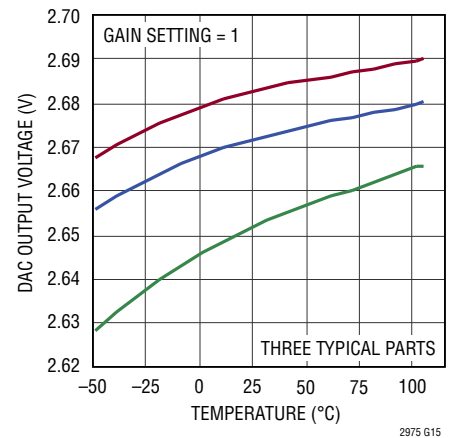
**Current Supervisor Total Unadjusted Error vs Temperature**



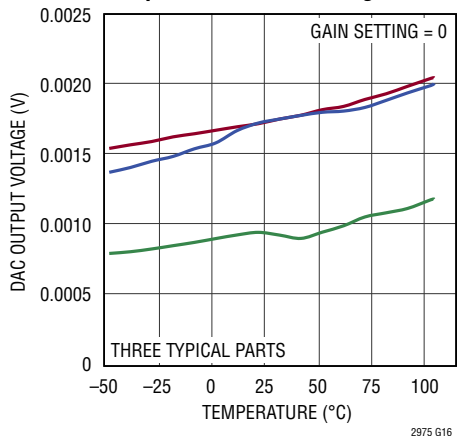
**DAC Full-Scale Voltage vs Temperature, Gain Setting = 0**



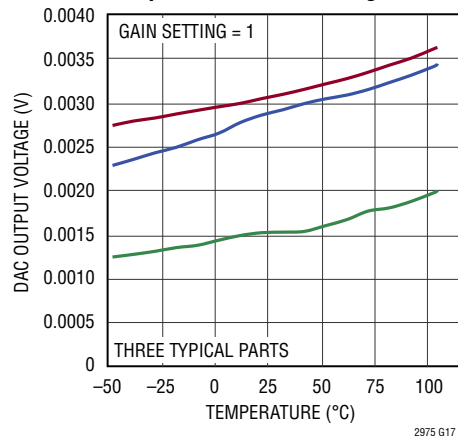
**DAC Full-Scale Voltage vs Temperature, Gain Setting = 1**



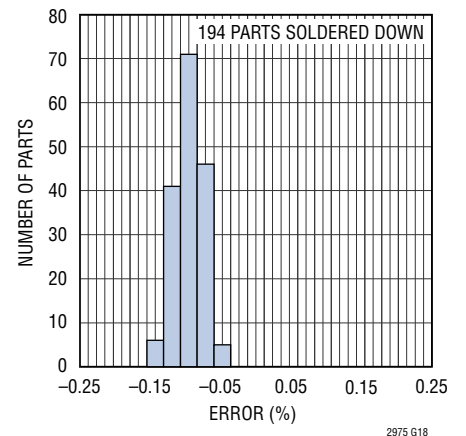
**DAC Offset Voltage vs Temperature, Gain Setting = 0**



**DAC Offset Voltage vs Temperature, Gain Setting = 1**

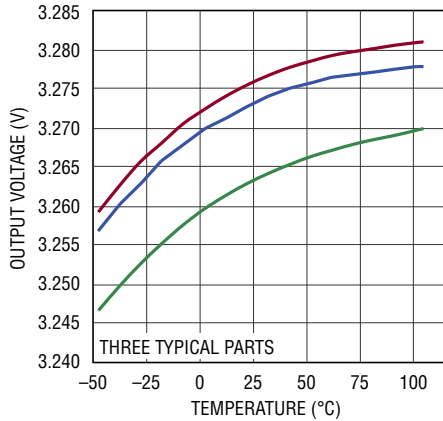


**Closed-Loop Servo Error**

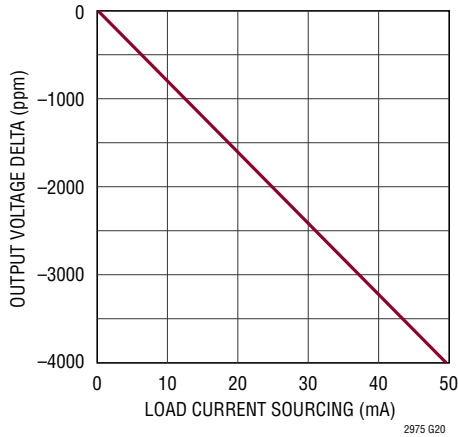


## TYPICAL PERFORMANCE CHARACTERISTICS

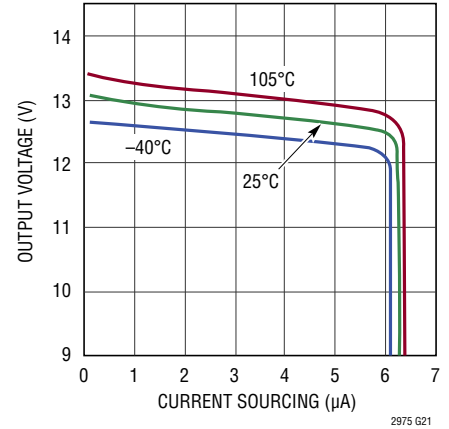
**V<sub>DD33</sub> Regulator Output Voltage vs Temperature**



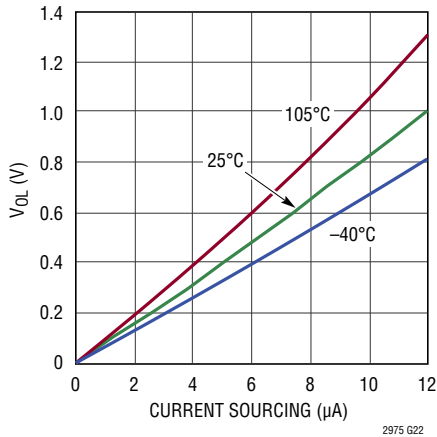
**V<sub>DD33</sub> Regulator Load Regulation**



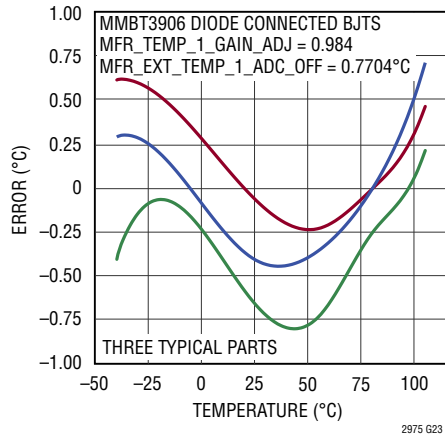
**V<sub>OUT\_EN[0:3]</sub> and AUXFAULTB Output High Voltage vs Load Current**



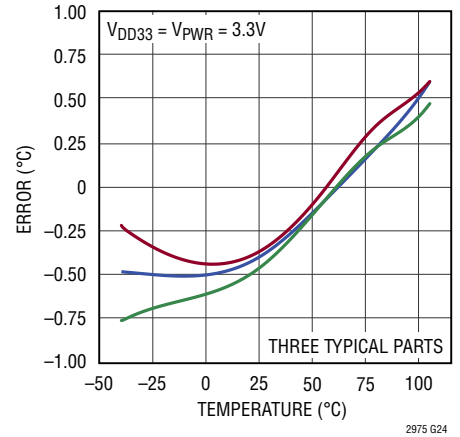
**V<sub>OUT\_EN[0:3]</sub> and AUXFAULTB VOL vs Load Current**



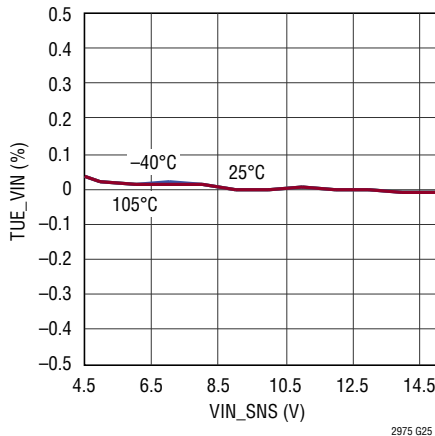
**External Temperature READ\_TEMPERATURE\_1 Error vs Temperature**



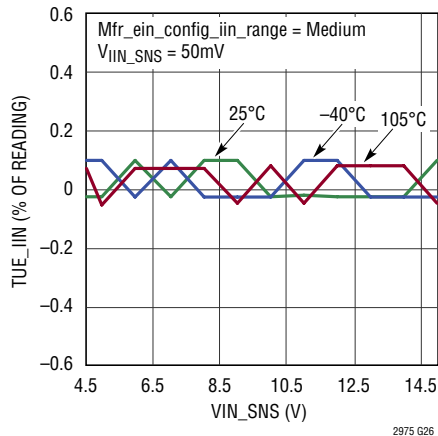
**READ\_TEMPERATURE\_2 Error vs Temperature**



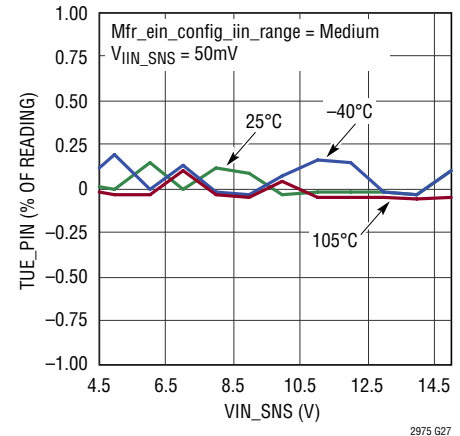
**TUE\_VIN vs VIN\_SNS**



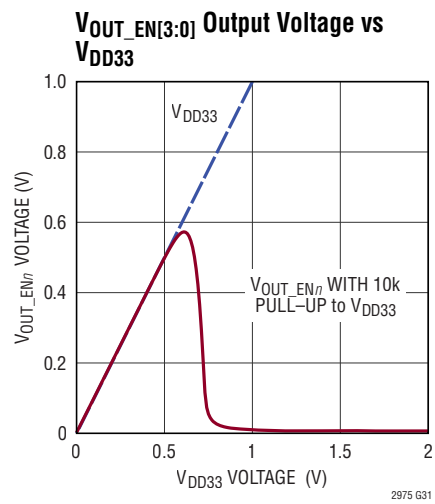
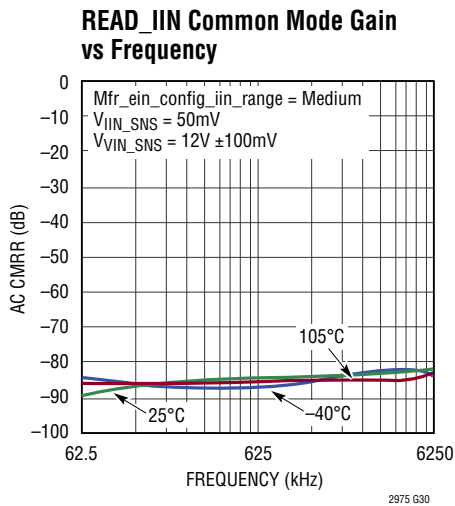
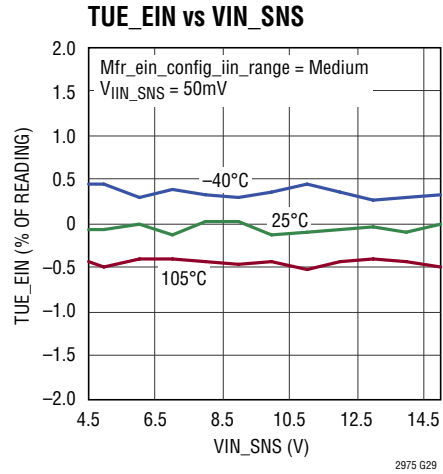
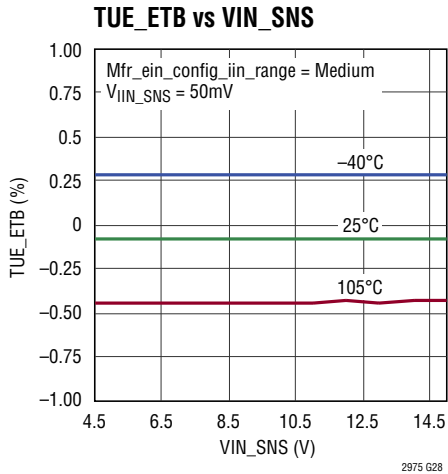
**TUE\_IIN vs VIN\_SNS**



**TUE\_PIN vs VIN\_SNS**



# TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

PIN NAME	PIN NUMBER QFN	PIN NUMBER BGA	PIN TYPE	DESCRIPTION
V <sub>SENSE0</sub>	1*	B2	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
V <sub>SENSE0</sub>	2*	B1	In	DC/DC Converter Differential (-) Output Voltage-0 Sensing Pin
V <sub>OUT_EN0</sub>	3	C2	Out	DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5 $\mu$ A
V <sub>OUT_EN1</sub>	4	C1	Out	DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5 $\mu$ A
V <sub>OUT_EN2</sub>	5	D3	Out	DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5 $\mu$ A
V <sub>OUT_EN3</sub>	6	D1	Out	DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5 $\mu$ A
AUXFAULTB	7	E3	Out	Auxiliary Fault Output Pin. Output High Voltage Optionally Pulled-Up to 12V by 5 $\mu$ A. Can Be Configured to Pull Low When OV/OC/UC Detected
DNC	8	E1	Do Not Connect	Do Not Connect to this Pin
V <sub>IN_SNS</sub>	9	E2	In	V <sub>IN_SNS</sub> SENSE Input. This Voltage is Compared Against the V <sub>IN</sub> On and Off Voltage Thresholds In Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V <sub>PWR</sub>	10	G2	In	V <sub>PWR</sub> Serves as the Unregulated Power Supply Input to the Chip (4.5 to 15V). If a 4.5V to 15V Supply Voltage Is Unavailable, Short V <sub>PWR</sub> to V <sub>DD33</sub> and Power the Chip Directly from a 3.3V Supply. Bypass to GND with 0.1 $\mu$ F Capacitor.
V <sub>DD33</sub>	11, 12	F1	In/Out	If Shorted to V <sub>PWR</sub> , It Serves as 3.13 to 3.47V Supply Input Pin. Otherwise It Is a 3.3V Internally Regulated Voltage Output (Use 0.1 $\mu$ F Decoupling Capacitor to GND). If using the internal regulator to provide V <sub>DD33</sub> , only connect the pull-up resistors and bypass capacitors required to support the LTC2975 in the application.
V <sub>DD25</sub>	13	G1	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1 $\mu$ F Capacitor. Only connect the pull-up resistors and bypass capacitors required to support the LTC2975 in the application.
V <sub>DD25</sub>	14	H1	In	2.5V Supply Voltage Input. Short this Pin to Pin 13. Only connect the pull-up resistors and bypass capacitors required to support the LTC2975 in the application.
T <sub>SENSE0</sub>	15*	F2	In/Out	External Temperature Current Output and Voltage Input for Channel 0. Maximum allowed capacitance is 1 $\mu$ F
T <sub>SENSE1</sub>	16*	F3	In/Out	External Temperature Current Output and Voltage Input for Channel 1. Maximum allowed capacitance is 1 $\mu$ F
PWRGD	17	J1	Out	Power-Good Open Drain Output. Indicates When Selected Outputs Are Power Good. Can be Used as System Power-on Reset
SHARE_CLK	18	J2	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49k $\Omega$ Pull-Up Resistor to V <sub>DD33</sub> . Connect to all other SHARE_CLK pins in the system.
GND	19	D2	Ground	Chip Ground. Must Be Soldered to PCB
GND	20	D4	Ground	Chip Ground. Must Be Soldered to PCB
GND	21	E4	Ground	Chip Ground. Must Be Soldered to PCB
CONTROL2	22	H3	In	Control Pin 2 Input
CONTROL3	23	J3	In	Control Pin 3 Input
WDI/RESETB	24	H2	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k $\Omega$ Pull-Up Resistor to V <sub>DD33</sub> . Rising Edge Resets Watchdog Counter. Holding this Pin Low for More than t <sub>RESETB</sub> Resets the Chip
FAULTB0	25	H4	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-0. Connect a 10k $\Omega$ Pull-Up Resistor to V <sub>DD33</sub>
FAULTB1	26	J4	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-1. Connect a 10k $\Omega$ Pull-Up Resistor to V <sub>DD33</sub>
T <sub>SENSE2</sub>	27*	G5	In/Out	External Temperature Current Output and Voltage Input for Channel 2. Maximum allowed capacitance is 1 $\mu$ F
WP	28	H5	In	Digital Input. Write-Protect Input Pin, Active High
SDA	29	J5	In/Out	PMBus Bidirectional Serial Data Pin
SCL	30	J6	In	PMBus Serial Clock Input Pin (400kHz Maximum)

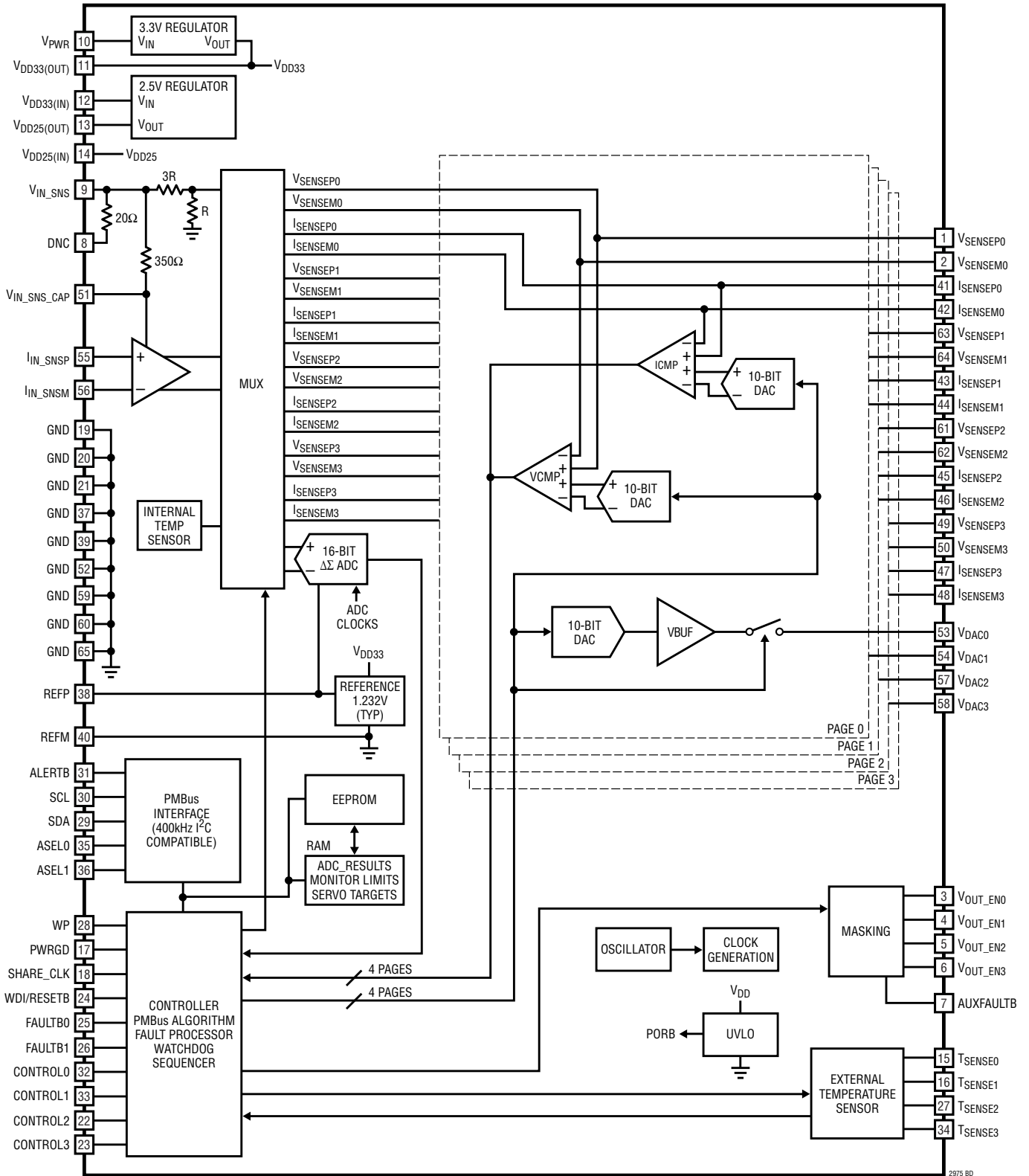


## PIN FUNCTIONS

PIN NAME	PIN NUMBER QFN	PIN NUMBER BGA	PIN TYPE	DESCRIPTION
ALERTB	31	J7	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation
CONTROL0	32	H7	In	Control Pin 0 Input
CONTROL1	33	H6	In	Control Pin 1 Input
T <sub>SENSE3</sub>	34*	G6	In/Out	External Temperature Current Output and Voltage Input for Channel 3. Maximum allowed capacitance is 1 $\mu$ F
ASEL0	35	G7	In	Ternary Address Select Pin 0 Input. Connect to V <sub>DD33</sub> , GND or Float to Encode 1 of 3 Logic States
ASEL1	36	E5	In	Ternary Address Select Pin 1 Input. Connect to V <sub>DD33</sub> , GND or Float to Encode 1 of 3 Logic States
GND	37	F5	Ground	Chip Ground. Must Be Soldered to PCB
REFP	38	F6	Out	Reference Voltage Output. Needs 0.1 $\mu$ F Decoupling Capacitor to REFM
GND	39	F4	Ground	Chip Ground. Must Be Soldered to PCB
REFM	40	F7	Out	Reference Return Pin. Needs 0.1 $\mu$ F Decoupling Capacitor to REFP
I <sub>SENSEP0</sub>	41*	E6	In	DC/DC Converter Differential (+) Output Current-0 Sensing Pin
I <sub>SENSEM0</sub>	42*	D5	In	DC/DC Converter Differential (-) Output Current-0 Sensing Pin
I <sub>SENSEP1</sub>	43*	E7	In	DC/DC Converter Differential (+) Output Current-1 Sensing Pin
I <sub>SENSEM1</sub>	44*	D6	In	DC/DC Converter Differential (-) Output Current-1 Sensing Pin
I <sub>SENSEP2</sub>	45*	D7	In	DC/DC Converter Differential (+) Output Current-2 Sensing Pin
I <sub>SENSEM2</sub>	46*	C7	In	DC/DC Converter Differential (-) Output Current-2 Sensing Pin
I <sub>SENSEP3</sub>	47*	C6	In	DC/DC Converter Differential (+) Output Current-3 Sensing Pin
I <sub>SENSEM3</sub>	48*	B6	In	DC/DC Converter Differential (-) Output Current-3 Sensing Pin
V <sub>SENSEP3</sub>	49*	B7	In	DC/DC Converter Differential (+) Output Voltage-3 Sensing Pin
V <sub>SENSEM3</sub>	50*	A7	In	DC/DC Converter Differential (-) Output Voltage-3 Sensing Pin
V <sub>IN_SNS_CAP</sub>	51	A6	Out	V <sub>IN_SNS</sub> Filter Capacitor Pin. Bypass to Ground with a 10nF Ceramic Capacitor
GND	52	G3	Ground	Chip Ground. Must be Soldered to PCB.
V <sub>DAC0</sub>	53	A5	Out	DAC0 Output
V <sub>DAC1</sub>	54	B5	Out	DAC1 Output
I <sub>IN_SNSP</sub>	55	B4	In	DC/DC Converter Differential (+) Input Current Sensing Pin. If Unused, Connect to V <sub>IN_SNS</sub>
I <sub>IN_SNSM</sub>	56	A4	In	DC/DC Converter Differential (-) Input Current Sensing Pin. If Unused, Connect to V <sub>IN_SNS</sub>
V <sub>DAC2</sub>	57	C4	Out	DAC2 Output
V <sub>DAC3</sub>	58	A3	Out	DAC3 Output
GND	59	C5	Ground	Chip Ground. Must Be Soldered to PCB
GND	60	G4	Ground	Chip Ground. Must Be Soldered to PCB
V <sub>SENSEP2</sub>	61*	B3	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
V <sub>SENSEM2</sub>	62*	C3	In	DC/DC Converter Differential (-) Output Voltage-2 Sensing Pin
V <sub>SENSEP1</sub>	63*	A2	In	DC/DC Converter Differential (+) Output Voltage-1 Sensing Pin
V <sub>SENSEM1</sub>	64*	A1	In	DC/DC Converter Differential (-) Output Voltage-1 Sensing Pin
GND	65	-	Ground	Exposed Pad. Must Be Soldered to PCB, QFN Only

\* Tie any unused V<sub>SENSEP<sub>n</sub></sub>/I<sub>SENSEP<sub>n</sub></sub>, V<sub>SENSEM<sub>n</sub></sub>/I<sub>SENSEM<sub>n</sub></sub> or T<sub>SENSE<sub>n</sub></sub> pins to GND. Refer to Unused ADC Sense Inputs in the Applications Information section.

**BLOCK DIAGRAM**



See Figure 35 for a Typical Application with a Simplified Block Diagram

## OPERATION

### LTC2975 OPERATION OVERVIEW

The LTC2975 is a PMBus programmable power supply controller, monitor, sequencer and voltage and current supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage, output voltage, output current, output temperature, and LTC2975 internal temperature readback through the PMBus interface.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTC2975 supports time-based sequencing and tracking sequencing. Cascade sequence on with time based sequence off is also supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Trim or margin the DC/DC converter output voltage with direct access to the margin DAC.
- Supervise the DC/DC converter input voltage, output voltage, load current and the inductor temperatures for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of current supervisors and ADC current measurement.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF\_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR\_RETRY\_COUNT programs the number of retries (0 to 6 or infinite) for all pages.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow trimming restart if target drifts outside of  $V_{OUT}$  warning limits.
- Store command register contents to EEPROM with CRC and ECC through PMBus programming.
- Restore EEPROM contents through PMBus programming or when  $V_{DD33}$  is applied on power-up.
- Report the DC/DC converter output voltage status through the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTC2975 FAULTB0 and FAULTB1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE\_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output OV, UV, OC and UC faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the on state after a power cycle until a programmable interval (MFR\_RESTART\_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR\_VOUT\_DISCHARGE\_THRESHOLD).
- Read high side input current, input voltage, input power, and accumulated input energy.
- Record minimum and maximum input voltage, input current, input power, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr\_ee\_unlock, Mfr\_ee\_erase, and Mfr\_ee\_data). Facilitates in-house bulk programming.
- Accommodate multiple hosts with Command Plus.

## OPERATION

### EEPROM

The LTC2975 contains internal EEPROM (Non-Volatile Memory) with error-correcting code (ECC) to store configuration settings and fault log information. EEPROM endurance, retention and mass write operation time are specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Non destructive operation above  $T_J = 105^\circ\text{C}$  is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above  $105^\circ\text{C}$  may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above  $105^\circ\text{C}$ , a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE\_USER\_ALL or bulk programming when  $T_J > 85^\circ\text{C}$ .

The degradation in EEPROM retention for temperatures  $>105^\circ\text{C}$  can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[ \left( \frac{E_a}{k} \right) \cdot \left( \frac{1}{T_{USE} + 273} - \frac{1}{T_{STRESS} + 273} \right) \right]}$$

where:

AF = acceleration factor

$E_a$  = activation energy = 1.4eV

$k = 8.617 \cdot 10^{-5} \text{ eV/}^\circ\text{K}$

$T_{USE} = 105^\circ\text{C}$  specified junction temperature

$T_{STRESS} = \text{actual junction temperature } ^\circ\text{C}$

Example: Calculate the effect on retention when operating at a junction temperature of  $125^\circ\text{C}$  for 10 hours.

$T_{STRESS} = 125^\circ\text{C}$

$T_{USE} = 105^\circ\text{C}$

AF = 8.65

Equivalent operating time at  $105^\circ\text{C} = 86.5 \text{ hours.}$

So the overall retention of the EEPROM was degraded by an additional 76.5 hours as a result of operation at a junction temperature of  $125^\circ\text{C}$  for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 175,200 hours at a junction temperature of  $105^\circ\text{C}$ .

### AUXFAULTB

The AUXFAULTB pin can be configured to indicate when some fault conditions have been detected. See Figure 1 for a conceptual view of this multiplexing.

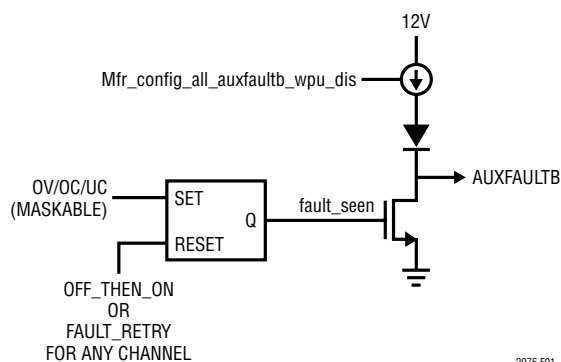


Figure 1. AUXFAULTB MUX

The MFR\_CONFIG2\_LTC2975 and MFR\_CONFIG3\_LTC2975 commands can be used on a per channel basis to select which, if any, fault conditions will cause the AUXFAULTB pin to be driven low. The only fault types which can be propagated to the AUXFAULTB pin are overvoltage faults and overcurrent/undercurrent faults.

Mfr\_config\_all\_auxfaultb\_wpu selects whether the AUXFAULTB pin is in the hi-Z state, or weakly pulled-up to approximately 12V, using a  $5\mu\text{A}$  current. As shown in Figure 1, the pull-down to GND overrides if any enabled faults are detected.

## OPERATION

### RESETB

Holding the WDI/RESETB pin low for more than  $t_{\text{RESETB}}$  will cause the LTC2975 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I<sup>2</sup>C bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2975 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to V<sub>DD33</sub> with a 10k resistor. WDI/RESETB includes an internal 256 $\mu$ s deglitch filter so additional filter capacitance on this pin is not recommended.

### PMBus SERIAL DIGITAL INTERFACE

The LTC2975 communicates with a host (master) using the standard PMBus serial bus interface. The PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2975 is a slave device. The master can communicate with the LTC2975 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus commands are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 2 to 14 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the Mfr\_config\_all\_longer\_pmbus\_timeout setting.

### PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I<sup>2</sup>C with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I<sup>2</sup>C byte commands because they provide timeouts to prevent bus hangs and optional Packet Error Checking (PEC) to ensure data integrity. In general, a master device that can be configured for I<sup>2</sup>C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Section 5: Transport. This can be found at:

[www.pmbus.org](http://www.pmbus.org)

For a description of the differences between SMBus and I<sup>2</sup>C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B – Differences between SMBus and I<sup>2</sup>C. This can be found at:

[www.smbus.org](http://www.smbus.org)

When using an I<sup>2</sup>C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I<sup>2</sup>C read.

### Device Address

The I<sup>2</sup>C/SMBus address of the LTC2975 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to V<sub>DD33</sub>, GND or FLOAT. See Table 3. Using one base address and the nine values of N, nine LTC2975s can be connected together to control thirty six outputs. The base address is stored in the MFR\_I2C\_BASE\_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I<sup>2</sup>C/SMBus device or global addresses, including I<sup>2</sup>C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTC2975 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR\_I2C\_BASE\_ADDRESS register.

Rev. D

## OPERATION

### Processing Commands

The LTC2975 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables. MFR\_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTC2975 is busy.

If a part is busy processing a previous command and a new command arrives, a BUSY fault is created. The ALERTB is pulled low and the second command is not processed. To avoid the occurrence of a BUSY fault, the user can add a polling loop to SEND BYTE, WRITE BYTE, and WRITE WORD commands. A polling loop checks whether the device is busy and the master issues a subsequent command only if the device is not busy. The master performs this check by reading bit 6 in the MFR\_COMMON command. Bit 6 is low when the LTC2975 is busy. EEPROM commands are in table 1 below, which includes typical execution delays.

**Table 1. EEPROM Related Commands**

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	$t_{\text{MASS\_WRITE}}$	These commands have large delays and require monitoring of MFR_COMMON bit 6. If MFR_COMMON bit 6 is low, the LTC2975 will not accept new commands (except MFR_COMMON) and will be in a busy state. If another command is issued while the device is busy, the address byte will be ACKed, the command byte will be NACKed, and ALERTB will be asserted low. MFR_COMMON may always be read without creating a BUSY fault.
RESTORE_USER_ALL	30ms	
MFR_FAULT_LOG_CLEAR	175ms	
MFR_FAULT_LOG_STORE	20ms	
Internal Fault Log	20ms	
MFR_FAULT_LOG_RESTORE	2ms	
MFR_EE_ERASE	Consult Factory	
MFR_EE_DATA	Consult Factory	

\*The typical delay indicates the typical amount of time needed to complete the internal operation. It is measured from the stop of the first command to the start of the next command.

Writes to RAM locations may also cause BUSY faults. Table 2 shows typical delays for commands that may require time to complete the internal operation.

**Table 2. Other Commands**

COMMAND	TYPICAL DELAY*	COMMENT
IOUT_CAL_GAIN	<500 $\mu$ s	The LTC2975 will not accept new commands (except MFR_COMMON) while it is processing this command and will be in a busy state. If another command is issued while the device is busy, the address byte will be ACKed, the command byte will be NACKed, and ALERTB will be asserted low. MFR_COMMON may always be read without creating a BUSY fault.
MFR_IIN_CAL_GAIN	<500 $\mu$ s	
MFR_DATA_PLUS0	<50 $\mu$ s	
MFR_DATA_PLUS1	<50 $\mu$ s	
IOUT_OC_FAULT_LIMIT	<50 $\mu$ s	
MFR_CONFIG	<50 $\mu$ s	
IOUT_UC_FAULT_LIMIT	<50 $\mu$ s	
TON_RISE	<50 $\mu$ s	
VOUT_OV_FAULT_LIMIT	<50 $\mu$ s	
VOUT_UV_FAULT_LIMIT	<50 $\mu$ s	
MFR_DAC	<50 $\mu$ s	

\*The typical delay indicates the typical amount of time needed to complete the internal operation. It is measured from the stop of the first command to the start of the next command.

### Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTC2975 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500 $\mu$ s.

# OPERATION

**Table 3. LTC2975 Address Look-Up Table with MFR\_I2C\_BASE\_ADDRESS Set to 7bit 0x5C**

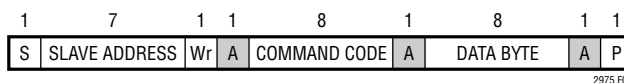
ADDRESS PINS		DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS							R/W
ASEL1	ASEL0		7-Bit	8-Bit	6	5	4	3	2	1	0	
X	X	Alert Response	0C	19	0	0	0	1	1	0	0	1
X	X	Global	5B	B6	1	0	1	1	0	1	1	0
L	L	N = 0	5C*	B8	1	0	1	1	1	0	0	0
L	NC	N = 1	5D	BA	1	0	1	1	1	0	1	0
L	H	N = 2	5E	BC	1	0	1	1	1	1	0	0
NC	L	N = 3	5F	BE	1	0	1	1	1	1	1	0
NC	NC	N = 4	60	C0	1	1	0	0	0	0	0	0
NC	H	N = 5	61	C2	1	1	0	0	0	0	1	0
H	L	N = 6	62	C4	1	1	0	0	0	1	0	0
H	NC	N = 7	63	C6	1	1	0	0	0	1	1	0
H	H	N = 8	64	C8	1	1	0	0	1	0	0	0

H = Tie to V<sub>DD33</sub>, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care  
 \*MFR\_I2C\_BASE\_ADDRESS = 7bit 0x5C (Factory Default)

- S START CONDITION
- Sr REPEATED START CONDITION
- Rd READ (BIT VALUE OF 1)
- Wr WRITE (BIT VALUE OF 0)
- $\bar{A}$  NOT ACKNOWLEDGE (HIGH)
- A ACKNOWLEDGE (LOW)
- P STOP CONDITION
- PEC PACKET ERROR CODE
- MASTER TO SLAVE
- SLAVE TO MASTER
- ... CONTINUATION OF PROTOCOL

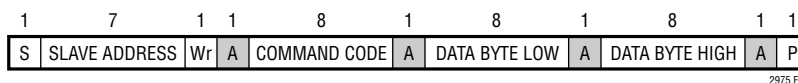
2975 F02

**Figure 2. PMBus Packet Protocol Diagram Element Key**



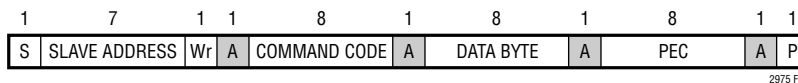
2975 F03

**Figure 3. Write Byte Protocol**



2975 F04

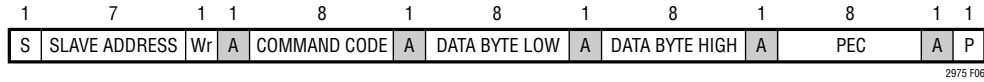
**Figure 4. Write Word Protocol**



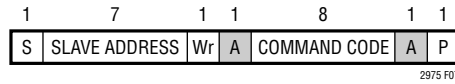
2975 F05

**Figure 5. Write Byte Protocol with PEC**

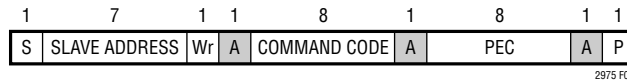
**OPERATION**



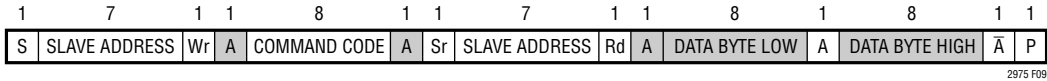
**Figure 6. Write Word Protocol with PEC**



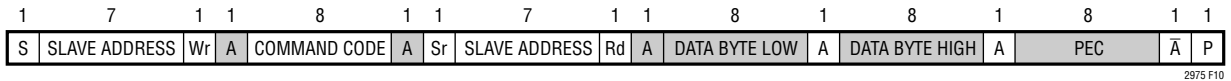
**Figure 7. Send Byte Protocol**



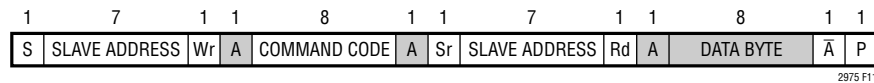
**Figure 8. Send Byte Protocol with PEC**



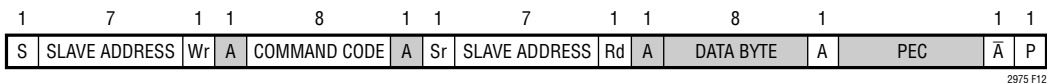
**Figure 9. Read Word Protocol**



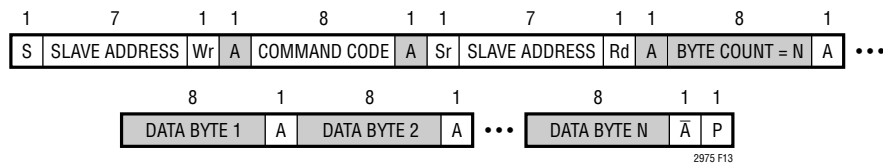
**Figure 10. Read Word Protocol with PEC**



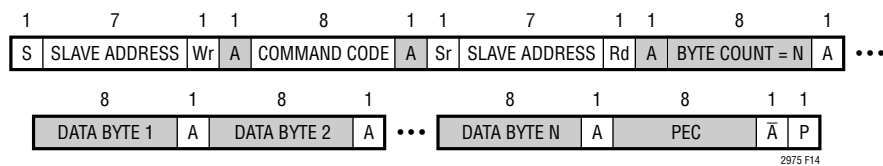
**Figure 11. Read Byte Protocol**



**Figure 12. Read Byte Protocol with PEC**



**Figure 13. Block Read**



**Figure 14. Block Read with PEC**



## PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	31
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	36
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	37
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	65
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	32
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	46
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	46
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	83
VOUT_MODE	0x20	Output voltage data format and mantissa exponent ( $2^{-13}$ ).	R Byte	Y	Reg			0x13	52
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	52
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	52
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	52
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	52
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	48
VIN_OFF	0x36	Input voltage below which power conversion is disabled. All $V_{OUT\_ENn}$ pins go off immediately or sequence off after $TOFF\_DELAY$ (See $Mfr\_track\_en\_chan$ ).	R/W Word	N	L11	V	Y	9.0 0xD240	48
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in $m\Omega$ .	R/W Word	Y	L11	$m\Omega$	Y	1.0 0xBA00	53
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	60
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	60
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	52
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	52
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for $Ton\_max\_fault$ and power good de-assertion.	R/W Word	Y	L16	V	Y	0.9 0x1CCD	52

**Note:** The data format abbreviations are detailed at the end of this table

## PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	60
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	10.0 0xD280	53
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	61
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	5.0 0xCA80	53
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	-1.0 0xB400	53
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	61
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	55
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	62
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	55
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	55
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	-5.0 0xCD80	55
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	62
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	48
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	62
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	14.0 0xD380	48
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	48
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	48
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	62
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.96 0x1EB8	52
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_config_all_pwrzd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	0.94 0x1E14	52
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to VOUT_EN <sub>n</sub> pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	57

## PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
TON_RISE	0x61	Time from when the $V_{OUT\_ENn}$ pin goes high until the LTC2975 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	57
TON_MAX_FAULT_LIMIT	0x62	Maximum time from $V_{OUT\_ENn} = ON$ assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	57
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	63
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to $V_{OUT\_ENn}$ pin = OFF.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	57
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	66
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	66
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	67
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	67
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	67
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	68
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	68
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	68
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	71
READ_IIN	0x89	DC/DC converter input current.	R Word	N	L11	A		NA	71
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	71
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	72
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	72
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	72
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	73
READ_PIN	0x97	DC/DC converter input power.	R Word	N	L11	W		NA	71
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	84
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	84
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	84
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	84
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	84
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	84
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	84
MFR_INFO	0xB6	Manufacturer specific information.	R Word	N	Reg			NA	84

## PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	55
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by $4 \cdot t_{CONV\_SENSE}$ .	R/W Word	Y	L11		Y	0.0 0x8000	55
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	55
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	72
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	84
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	47
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	47
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	47
MFR_EIN	0xC0	Input Energy data bytes.	R Block	N	Reg			NA	49
MFR_EIN_CONFIG	0xC1	Configuration register for energy and input current.	R/W Byte	N	Reg		Y	0x00	50
MFR_SPECIAL_LOT	0xC2	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	84
MFR_IIN_CAL_GAIN_TC	0xC3	Temperature coefficient applied to IIN_CAL_GAIN.	R/W Word	N	CF	ppm	Y	0x0000	51
MFR_IIN_PEAK	0xC4	Maximum measured value of READ_IIN.	R Word	N	L11	A		NA	72
MFR_IIN_MIN	0xC5	Minimum measured value of READ_IIN.	R Word	N	L11	A		NA	72
MFR_PIN_PEAK	0xC6	Maximum measured value of READ_PIN.	R Word	N	L11	W		NA	72
MFR_PIN_MIN	0xC7	Minimum measured value of READ_PIN.	R Word	N	L11	W		NA	72
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				33
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				33
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				33
MFR_CLEAR_ENERGY	0xCC	Clear MFR_EIN time and energy values.	Send Byte	N				NA	51
MFR_CONFIG_LTC2975	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	0x0080	38
MFR_CONFIG_ALL_LTC2975	0xD1	Configuration bits that are common to all pages.	R/W Word	N	Reg		Y	0x0F7B	44
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted off state is propagated to the FAULTB0 pin.	R/W Byte	Y	Reg		Y	0x00	64

## PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted off state is propagated to the FAULTB1 pin.	R/W Byte	Y	Reg		Y	0x00	64
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	58
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the FAULTB0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	64
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the FAULTB1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	64
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	74
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	75
MFR_CONFIG2_LTC2975	0xD9	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	40
MFR_CONFIG3_LTC2975	0xDA	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	41
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	63
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	58
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	74
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	74
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	74
MFR_DAC	0xE0	The code of the 10-bit DAC.	R/W Word	Y	Reg			NA	52
MFR_POWERGOOD_ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	59
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	59
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	59
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x0F	32
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R Word	N	Reg			NA	69
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I <sup>2</sup> C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	33
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTC2975.	R Word	N	Reg		Y	0x0226	84
MFR_IIN_CAL_GAIN	0xE8	The nominal resistance of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	1.0 0xBA00	50
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine V <sub>OUT</sub> off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	52
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	75
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	76

## PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	76
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	76
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	76
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	70
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R/W Word	Y	CF	ppm	Y	0x0000	51
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	63
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = $2^{-14}$ .	R/W Word	Y	CF		Y	1 0x4000	55
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	55
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of the voltage between $I_{SENSEp_n}$ and $I_{SENSEM_n}$ . One LSB = $3.05\mu\text{V}$ .	R Word	Y	CF	$3.05\mu\text{V}$		NA	74
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	74
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	74
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	75

### Data Formats

L11	Linear_5s_11s	<p>PMBus data field b[15:0]            Value = <math>Y \cdot 2^N</math>            where <math>N = b[15:11]</math> is a 5-bit two's complement integer and <math>Y = b[10:0]</math> is an 11-bit two's complement integer            Example:            READ_VIN = 10V            For b[15:0] = 0xD280 = 1101_0010_1000_0000b            Value = <math>640 \cdot 2^{-6} = 10</math>            See PMBus Spec Part II: Paragraph 7.3</p>
L16	Linear_16u	<p>PMBus data field b[15:0]            Value = <math>Y \cdot 2^N</math> where <math>Y = b[15:0]</math> is an unsigned integer and <math>N = \text{Vout\_mode\_parameter}</math> is a 5-bit two's complement exponent that is hardwired to <math>-13</math> decimal.            Example:            VOUT_COMMAND = 4.75V            For b[15:0] = 0x9800 = 1001_1000_0000_0000b            Value = <math>38912 \cdot 2^{-13} = 4.75</math>            See PMBus Spec Part II: Paragraph 8.4.1</p>
Reg	Register	<p>PMBus data field b[15:0] or b[7:0].            Bit field meaning is defined in detailed PMBus Command Register Description.</p>
CF	Custom Format	<p>PMBus data field b[15:0]            Value is defined in detailed PMBus Command Register Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.</p>

## PMBUS COMMAND DESCRIPTION

### ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	31
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	32
MFR_I2C_BASE_ADDRESS	0xE6	Base value of the I <sup>2</sup> C/SMBus address byte.	R/W Byte	N	Reg		Y	0x5C	33
MFR_PAGE_FF_MASK	0xE4	Configuration defining which channels respond to global page commands (PAGE=0xFF).	R/W Byte	N	Reg		Y	0x0F	32
MFR_COMMAND_PLUS	0xC8	Alternate access to block read and other data. Commands for all additional hosts.	R/W Word	N	Reg				33
MFR_DATA_PLUS0	0xC9	Alternate access to block read and other data. Data for additional host 0.	R/W Word	N	Reg				33
MFR_DATA_PLUS1	0xCA	Alternate access to block read and other data. Data for additional host 1.	R/W Word	N	Reg				33

### PAGE

The LTC2975 has four pages that correspond to the four DC/DC converter channels that can be managed. Each DC/DC converter channel can be uniquely programmed by first setting the appropriate page.

Setting PAGE = 0xFF allows a simultaneous write to all pages for PMBus commands that support global page programming. The only commands that support PAGE = 0xFF are CLEAR\_FAULTS, OPERATION and ON\_OFF\_CONFIG. See MFR\_PAGE\_FF\_MASK for additional options. Reading any paged PMBus register with PAGE = 0xFF returns unpredictable data and will trigger a CML fault. Writes to commands that do not support PAGE = 0xFF with PAGE = 0xFF will be ignored and generate a CML fault.

### PAGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Page	Page operation. 0x00: All PMBus commands address channel/page 0. 0x01: All PMBus commands address channel/page 1. 0x02: All PMBus commands address channel/page 2. 0x03: All PMBus commands address channel/page 3. 0xFF: All non specified values reserved. 0xFF: A single PMBus write/send to commands that support this mode will simultaneously address all channel/pages with MFR_PAGE_FF_MASK enabled.

## PMBUS COMMAND DESCRIPTION

### WRITE\_PROTECT

The WRITE\_PROTECT command provides protection against accidental programming of the LTC2975 command registers. All supported commands may have their parameters read, regardless of the WRITE\_PROTECT setting, and the EEPROM contents can also be read regardless of the WRITE\_PROTECT settings.

There are two levels of protection:

- Level 1: Nothing can be changed except the level of write protection itself. Values can be read from all pages. This setting can be stored to EEPROM.
- Level 2: Nothing can be changed except for the level of protection, channel on/off state, and clearing of faults. Values can be read from all pages. This setting can be stored to EEPROM.

#### WRITE\_PROTECT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Write_protect[7:0]	1000_0000b: Level 1 Protection - Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands. 0100_0000b: Level 2 Protection – Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, STORE_USER_ALL, OPERATION, MFR_COMMAND_PLUS, MFR_PAGE_FF_MASK, MFR_CLEAR_ENERGY and CLEAR_FAULTS commands. 0000_0000b: Enable writes to all commands. xxxx_xxxx: All other values reserved.

### Write Protect Pin

The WP pin allows the user to write-protect the LTC2975's configuration registers. The WP pin is active high, and when asserted it provides Level 2 protection: all writes are disabled except to the WRITE\_PROTECT, PAGE, MFR\_EE\_UNLOCK, STORE\_USER\_ALL, OPERATION, MFR\_COMMAND\_PLUS, MFR\_PAGE\_FF\_MASK, MFR\_CLEAR\_ENERGY and CLEAR\_FAULTS commands. The most restrictive setting between the WP pin and WRITE\_PROTECT command will override.

WP PIN STATE	WRITE_PROTECT COMMAND VALUE	WRITE PROTECT LEVEL
Low	0x00	No write protection
	0x40	Level 2
	0x80	Level 1
High	0x00	Level 2
	0x40	Level 2
	0x80	Level 1

### MFR\_PAGE\_FF\_MASK

The MFR\_PAGE\_FF\_MASK command is used to select which channels respond when the global page command (PAGE = 0xFF) is in use.

#### MFR\_PAGE\_FF\_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Always returns 0000b
b[3]	Mfr_page_ff_mask_chan3	Channel 3 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses



## PMBUS COMMAND DESCRIPTION

### MFR\_PAGE\_FF\_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[2]	Mfr_page_ff_mask_chan2	Channel 2 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[1]	Mfr_page_ff_mask_chan1	Channel 1 masking of global page command (PAGE=0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses
b[0]	Mfr_page_ff_mask_chan0	Channel 0 masking of global page command (PAGE = 0xFF) accesses 0 = ignore global page command accesses 1 = fully respond to global page command accesses

### MFR\_I2C\_BASE\_ADDRESS

The MFR\_I2C\_BASE\_ADDRESS command determines the base value for the I<sup>2</sup>C/SMBus address byte. Offsets of 0 to 8 are added to this base address to generate the device I<sup>2</sup>C/SMBus address. The part responds to the device address. For example, with the factory default MFR\_I2C\_BASE\_ADDRESS of 0x5C, with both ASEL1 and ASEL0 High (Offset N=8), the device address would be 0x5C + 8 = 0x64.

### MFR\_I2C\_BASE\_ADDRESS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Reserved	Read only, always returns 0.
b[6:0]	I2C_base_address	This 7-bit value determines the base value of the 7-bit I <sup>2</sup> C/SMBus address. See Device Address in the Operation section.

### MFR\_COMMAND\_PLUS

#### MFR\_DATA\_PLUS0 and MFR\_DATA\_PLUS1

#### MFR\_STATUS\_PLUS0, and MFR\_STATUS\_PLUS1

Similar to the PAGE register, these registers allow the user to indirectly address memory. These registers are useful to advanced users for reading or writing memory as described below.

Command Plus operations use a sequence of word commands to support the following:

- An alternate method for reading block data using sequential standard word reads.
- A peek operation that allows up to two additional hosts to read an internal register using PMBus word protocol where each host has a unique page.
- A poke operation that allows up to two additional hosts to write an internal register using PMBus word protocol where each host has a unique page.
- Peek, Poke and Command Plus block reads do not interfere with normal PMBus accesses or page values set by PAGE. This enables multi master support for up to 3 hosts.

## PMBUS COMMAND DESCRIPTION

### MFR\_COMMAND\_PLUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_command_plus_reserved	Reserved. Always returns 0.
b[14]	Mfr_command_plus_id	Command plus host ID 0: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus0 accesses. 1: Mfr_command_plus pointer and page are cached and used for all Mfr_data_plus1 accesses.
b[13:9]	Mfr_command_plus_page	Page to be used when peeking or poking via Mfr_data_plus0 or Mfr_data_plus1. Allowed values are 0 through 3. This page value is cached separately for Mfr_data_plus0 and Mfr_data_plus1 based on the value of Mfr_command_plus_id when this register is written.
b[8:0]	Mfr_command_plus_pointer	Internal memory location accessed by Mfr_data_plus0 or Mfr_data_plus1. Mfr_data_plus0 and Mfr_data_plus1 pointers are cached separately. Legal values are listed in the CMD Code column of the PMBus COMMAND SUMMARY table. All other values are reserved, except for the special poke enable/disable values listed in the Enabling And Disabling Poke Operations section, and the command values listed below for Mfr_status_plus0 and Mfr_status_plus1.

### MFR\_DATA\_PLUS0 and MFR\_DATA\_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_data_plus0 Mfr_data_plus1	A read from this register returns data referenced by the last matching Mfr_command_plus write. More specifically, writes to Mfr_command_plus by host 0 update Mfr_data_plus0, and writes to Mfr_command_plus by host1 update Mfr_data_plus1. Multiple sequential reads while pointer = Mfr_fault_Log return the complete contents of the block read buffer. Block reads beyond the end of buffer return zeros.  A write to this register will transfer the data to the location referenced by the last matching Mfr_command_plus_pointer when the Poke operation protocol described in the Poke Operation Using Mfr_data_plus0 section is followed.

### MFR\_STATUS\_PLUS0 and MFR\_STATUS\_PLUS1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	
b[1]	Mfr_status_plus_poke_failed0 Mfr_status_plus_poke_failed1	Status of most recent poke for matching host. 0: Last poke operation did not fail. 1: Last poke operation failed because pokes were not enabled, as described in Enabling and Disabling Poke Operations below, or an illegal Mfr_command_plus_page value was used.
b[0]	Mfr_status_plus_poke_failed0 Mfr_status_plus_poke_failed1	Status of most recent poke for matching host. 0: Last poke operation did not fail. 1: Last poke operation failed because pokes were not enabled as described in Enabling and Disabling Poke Operations section.

MFR\_STATUS\_PLUS0 is at command location 0x2C, and MFR\_STATUS\_PLUS1 is at command location 0x2D. These correspond to reserved PMBus command locations. These two status registers can only be read via Command Plus peeks.

### Reading Fault Log Using Command Plus and Mfr\_data\_plus0

Write Mfr\_command\_plus\_pointer = 0xEE with Mfr\_command\_plus\_page = 0 and Mfr\_command\_plus\_id = 0.

Read data from Mfr\_data\_plus0; each read returns the next data word of the MFR\_FAULT\_LOG command:

- The first word read is Byte\_count[15:0] = 0x00FF.
- The next set of words read is the Preamble with 2 bytes packed into a word. Refer to the Fault Log section for details.
- The next set of words read is the Cyclical Loop Data with 2 bytes per word. Refer to the Fault Log section for details.
- Extra reads return zero.

## PMBUS COMMAND DESCRIPTION

- Interleaved PMBus word and byte commands do not interfere with an ongoing Command Plus block read.
- Interleaved PMBus block reads of MFR\_FAULT\_LOG will interrupt this command.

Check status to be sure the data just read was all valid:

- Write Mfr\_command\_plus\_pointer = 0x2C with Mfr\_command\_plus\_page = 0 and Mfr\_command\_plus\_id = 0.
- Read data from Mfr\_data\_plus0 and confirm that Mfr\_status\_plus\_block\_peek\_failed0 = 0.

### Reading Energy Using MFR\_COMMAND\_PLUS and MFR\_DATA\_PLUS0

Write Mfr\_command\_plus\_pointer = 0xC0 with Mfr\_command\_plus\_page = 0 and Mfr\_command\_plus\_id = 0.

Read data from Mfr\_data\_plus\_0; each read returns the next data word of the MFR\_EIN command:

- Byte\_count[15:0] = 0x000C
- Energy\_value[15:0]
- Energy\_value[31:16]
- Energy\_value[47:32]
- Energy\_time[15:0]
- Energy\_time[31:16]
- Energy\_time[47:32]

### Peek Operation Using Mfr\_data\_plus0

Internal words and bytes may be read using Command Plus:

Write Mfr\_command\_plus\_pointer = CMD\_CODE with Mfr\_command\_plus\_page = page and Mfr\_command\_plus\_id = 0.

The CMD\_CODE's are listed in the PMBus COMMAND SUMMARY table.

Read data from Mfr\_data\_plus0. Data is always read using a word read. Byte data is returned with upper byte set to 0.

### Enabling and Disabling Poke Operations

Poke operations to Mfr\_data\_plus0 are enabled by writing Mfr\_command\_plus = 0x0BF6.

Poke operations to Mfr\_data\_plus0 are disabled by writing Mfr\_command\_plus = 0x01F6.

Poke operations to Mfr\_data\_plus1 are enabled by writing Mfr\_command\_plus = 0x4BF6.

Poke operations to Mfr\_data\_plus1 are disabled by writing Mfr\_command\_plus = 0x41F6.

### Poke Operation Using Mfr\_data\_plus0

Internal words and bytes may be written using Command Plus:

Enable poke access for Mfr\_data\_plus0. This need only be done once after a power-up or WDI reset.

Write Mfr\_command\_plus\_pointer = CMD\_CODE with Mfr\_command\_plus\_page = page and Mfr\_command\_plus\_id = 0.

The CMD\_CODEs are listed in the PMBus COMMAND SUMMARY table.

Write the new data value to MFR\_DATA\_PLUS0

## PMBUS COMMAND DESCRIPTION

Optionally check status to be sure data was written as desired:

- Write Mfr\_command\_plus\_pointer = 0x2C with Mfr\_command\_plus\_page = 0 and Mfr\_command\_plus\_id = 0.
- Read data from Mfr\_data\_plus0 and confirm that Mfr\_status\_plus\_poke\_failed0 = 0.

### Command Plus Operations Using Mfr\_data\_plus1

All the previous operations may be accessed via Mfr\_data\_plus1 by substituting Mfr\_command\_plus\_id value with a 1. Poke operations must be enabled for Mfr\_data\_plus1.

## ON/OFF CONTROL, MARGINING AND CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	36
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	37
MFR_CONFIG_LTC2975	0xD0	Configuration bits that are channel specific.	R/W Word	Y	Reg		Y	0x0080	38
MFR_CONFIG2_LTC2975	0xD9	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	40
MFR_CONFIG3_LTC2975	0xDA	Configuration bits that are channel specific	R/W Byte	N	Reg		Y	0x00	41
MFR_CONFIG_ALL_LTC2975	0xD1	Configuration bits that are common to all pages.	R/W Word	N	Reg		Y	0x0F7B	44

### OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the CONTROL pin and ON\_OFF\_CONFIG. This command register responds to the global page command (PAGE = 0xFF). The contents and functions of the data byte are shown in the following tables. A minimum  $t_{OFF\_MIN}$  wait time must be observed between any OPERATION commands used to turn the unit off and then back on.

#### OPERATION Data Contents (On\_off\_config\_use\_pmbus = 1)

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (read only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Turn off immediately	00	XX	XX	00
	Sequence on	10	00	XX	00
	Margin low (ignore faults and warnings)	10	01	01	00
	Margin low	10	01	10	00
	Margin high (ignore faults and warnings)	10	10	01	00
	Margin high	10	10	10	00
	Sequence off with margin to nominal	01	00	XX	00
	Sequence off with margin low (ignore faults and warnings)	01	01	01	00
	Sequence off with margin low	01	01	10	00
	Sequence off with margin high (ignore faults and warnings)	01	10	01	00
	Sequence off with margin high	01	10	10	00
	Reserved		All remaining combinations		

## PMBUS COMMAND DESCRIPTION

### OPERATION Data Contents (On\_off\_config\_use\_pmbus = 0) On or Off

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (read only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Output at nominal	00, 01 or 10	00	XX	00
	Margin low (ignore faults and warnings)	00, 01 or 10	01	01	00
	Margin low	00, 01 or 10	01	10	00
	Margin high (ignore faults and warnings)	00, 01 or 10	10	01	00
	Margin high	00, 01 or 10	10	10	00
	Reserved	All remaining combinations			

### ON\_OFF\_CONFIG

The ON\_OFF\_CONFIG command configures the combination of CONTROL pin input and PMBus commands needed to turn the LTC2975 on/off, including the power-on behavior, as shown in the following table. This command register responds to the global page command (PAGE = 0xFF). After the part has initialized, an additional comparator monitors VIN\_SNS. The VIN\_ON threshold must be exceeded before the output power sequencing can begin. After  $V_{IN}$  is initially applied, the part will typically require  $t_{INIT}$  to initialize and begin the TON\_DELAY timer. The readback of voltages and currents may require an additional wait for  $t_{UPDATE\_ADC}$ . A minimum  $t_{OFF\_MIN}$  wait time must be observed for any CONTROL pin used toggle to turn the unit off and then back on..

### ON\_OFF\_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Reserved	Don't care. Always returns 0.
b[4]	On_off_config_controlled_on	Control default autonomous power up operation. 0: Unit powers up regardless of the CONTROL pin or OPERATION value. Unit always powers up with sequencing. To turn unit on without sequencing, set TON_DELAY = 0. 1: Unit does not power up unless commanded by the CONTROL pin and/or the OPERATION command on the serial bus. If On_off_config[3:2] = 00, the unit never powers up.
b[3]	On_off_config_use_pmbus	Controls how the unit responds to commands received via the serial bus. 0: Unit ignores the Operation_control[1:0]. 1: Unit responds to Operation_control[1:0]. Depending on On_off_config_use_control, the unit may also require the CONTROL pin to be asserted for the unit to start.
b[2]	On_off_config_use_control	Controls how unit responds to the CONTROL pin. 0: Unit ignores the CONTROL pin. 1: Unit requires the CONTROL pin to be asserted to start the unit. Depending on On_off_config_use_pmbus the OPERATION command may also be required to instruct the device to start.
b[1]	Reserved	Not supported. Always returns 1.
b[0]	On_off_config_control_fast_off	CONTROL pin turn off action when commanding the unit to turn off 0: Use the programmed TOFF_DELAY. 1: Turn off the output and stop transferring energy as quickly as possible. The device does not sink current in order to decrease the output voltage fall time.

## PMBUS COMMAND DESCRIPTION

### MFR\_CONFIG\_LTC2975

This command is used to configure various manufacturer specific operating parameters for each channel.

#### MFR\_CONFIG\_LTC2975 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Reserved	Don't care. Always returns 0.
b[14]	Mfr_config_cascade_on	Configures channel's control pin for cascade sequence ON. There is no provision for cascade sequence OFF. See description for time based sequence OFF options.
b[13:12]	Mfr_config_controln_sel	Selects the active control pin input (CONTROL0, CONTROL1, CONTROL2 or CONTROL3) for this channel. 00: Select CONTROL0 pin. 01: Select CONTROL1 pin. 10: Select CONTROL2 pin. 11: Select CONTROL3 pin.
b[11]	Mfr_config_fast_servo_off	Disables fast servo when margining or trimming output voltages: 0: fast-servo enabled. 1: fast-servo disabled.
b[10]	Mfr_config_supervisor_resolution	Selects voltage supervisor resolution: 0: high resolution = 4mV / LSB, range for $V_{VSENSEPN} - V_{VSENSEMn}$ is 0 to 3.8V 1: low resolution = 8mV / LSB, range for $V_{VSENSEPN} - V_{VSENSEMn}$ is 0 to 6.0V
b[9:8]	Reserved	Always returns 0.
b[7]	Mfr_config_servo_continuous	Select whether the UNIT should continuously servo VOUT after it has reached a new margin or nominal target. Only applies when Mfr_config_dac_mode = 00b. 0: Do not continuously servo VOUT after reaching initial target. 1: Continuously servo VOUT to target.
b[6]	Mfr_config_servo_on_warn	Control re-servo on warning feature. Only applies when Mfr_config_dac_mode = 00b and Mfr_config_servo_continuous = 0. 0: Do not allow the unit to re-servo when a VOUT warning threshold is met or exceeded. 1: Allow the unit to re-servo VOUT to nominal target if $V_{OUT} \geq V(V_{out\_ov\_warn\_limit})$ or $V_{OUT} \leq V(V_{out\_uv\_warn\_limit})$ .
b[5:4]	Mfr_config_dac_mode	Determines how DAC is used when channel is in the ON state and TON_RISE has elapsed. 00: Soft-connect (if needed) and servo to target. 01: DAC not connected. 10: DAC connected immediately using value from MFR_DAC command. If this is the configuration after a reset or RESTORE_USER_ALL, MFR_DAC will be undefined and must be written to desired value. 11: DAC is soft-connected. After soft-connect is complete MFR_DAC may be written.
b[3]	Mfr_config_vo_en_wpu_en	V <sub>OUT_EN</sub> pin charge pumped, current-limited pull-up enable. 0: Disable weak pull-up. V <sub>OUT_EN</sub> pin driver is three-stated when channel is on. 1: Use weak current-limited pull-up on V <sub>OUT_EN</sub> pin when the channel is on.
b[2]	Mfr_config_vo_en_wpd_en	V <sub>OUT_EN</sub> pin charge-pumped, current-limited pull-down enable. 0: Use a fast N-channel device to pull down V <sub>OUT_EN</sub> pin when the channel is off for any reason. 1: Use weak current-limited pull-down to discharge V <sub>OUT_EN</sub> pin when channel is off due to soft stop by the CONTROL pin and/or OPERATION command. If the channel is off due to a fault, use the fast pull-down on the V <sub>OUT_EN</sub> pin.

## PMBUS COMMAND DESCRIPTION

### MFR\_CONFIG\_LTC2975 Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	Mfr_config_dac_gain	DAC buffer gain. 0: Select DAC buffer gain dac_gain_0 (1.38V full-scale) 1: Select DAC buffer gain dac_gain_1 (2.65V full-scale)
b[0]	Mfr_config_dac_pol	DAC output polarity. 0: Encodes negative (inverting) DC/DC converter trim input. 1: Encodes positive (non-inverting) DC/DC converter trim input.

### Cascade Sequence ON with Time-Based Sequence OFF

Cascade sequence ON allows a master power supply to sequence on a series of slave supplies by connecting each power supply’s power good output to the control pin of the next power supply in the chain. Please note that the power good signal is that of the power supply and not derived from the LTC2975’s internal power good processing. Power good based cascade sequence OFF is not supported, OFF sequencing must be managed using immediate or time based sequence OFF. See also Tracking Based Sequencing section.

Cascade sequence ON is illustrated in Figure 15. For each slave channel Mfr\_config\_cascade\_on is asserted high and the associated control input is connected to the power good output of the previous power supply. In this configuration each slave channel’s startup is delayed until the previous supply has powered up.

Cascade sequence OFF is not directly supported. Options for reversing the sequence when turning the supplies off include:

- Using the OPERATION command to turn off all the channels with an appropriate off delay.
- Using the FAULT pin to bring all the channels down immediately or in sequence with an appropriate off delay.

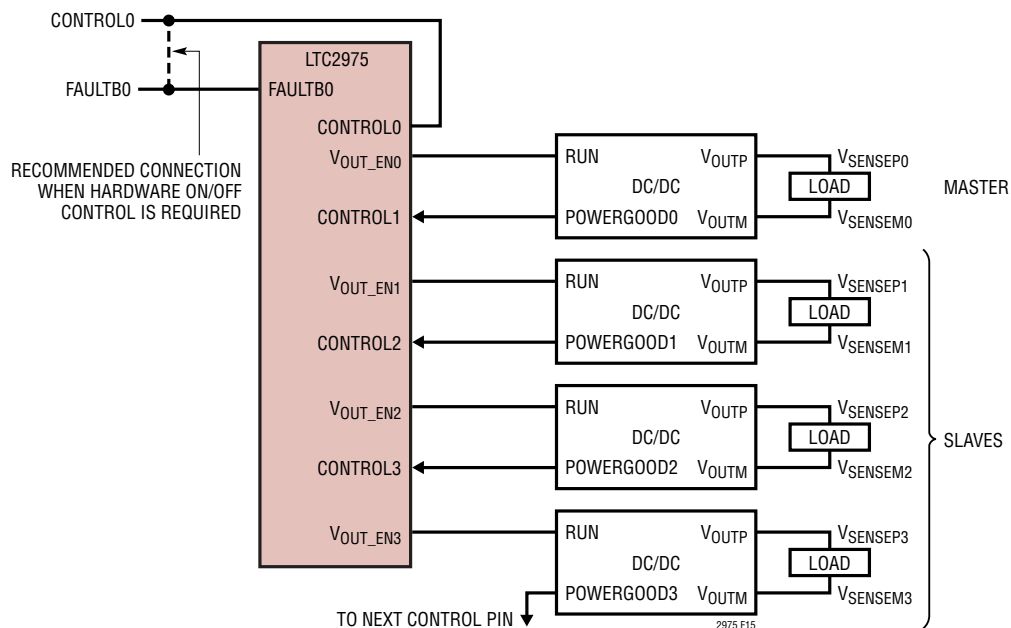


Figure 15. LTC2975 Configured to Cascade Sequence ON and Time-Base Sequence OFF

## PMBUS COMMAND DESCRIPTION

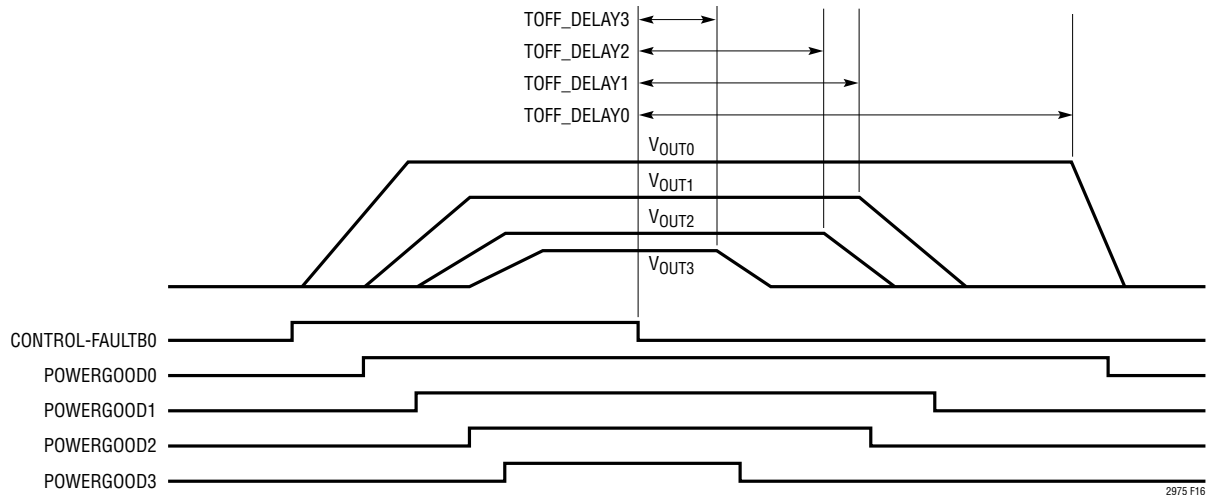


Figure 16. Cascade Sequence ON with Time Based Sequence Down on FAULT0

When asserted, `Mfr_config_cascade_on` enables a slave channel to honor fault retries even when its control pin is low. Additionally, if the system has faulted off after zero or a finite number of retries, an OPERATION command may be used to turn all cascade channels off then on to clear the faulted off state when the slave's control pin is low. For this reason we refer to the control pin as being redefined as a sequence pin.

The waveform of Figure 16 illustrates cascade sequence ON and time based sequence OFF using the configuration illustrated in Figure 15. In this example the FAULTB0 pin is used as a broadcast off signal. Turning the system off with the FAULTB0 requires all slave channels to be configured with `Mfr_faultb0_response_chann` asserted high. After the system is turned off, the LTC2975 will assert ALERTB with all slave channels indicating a `Status_mfr_fault0_in` event.

### MFR\_CONFIG2\_LTC2975

This command register determines whether  $V_{OUT}$  overvoltage or overcurrent faults from a given channel cause the AUXFAULTB pin to be pulled low.

#### MFR\_CONFIG2\_LTC2975 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	<code>Mfr_auxfaultb_oc_fault_response_chan3</code>	Response to channel 3 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[6]	<code>Mfr_auxfaultb_oc_fault_response_chan2</code>	Response to channel 2 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[5]	<code>Mfr_auxfaultb_oc_fault_response_chan1</code>	Response to channel 1 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[4]	<code>Mfr_auxfaultb_oc_fault_response_chan0</code>	Response to channel 0 IOUT_OC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[3]	<code>Mfr_auxfaultb_ov_fault_response_chan3</code>	Response to channel 3 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.

Rev. D



## PMBUS COMMAND DESCRIPTION

### MFR\_CONFIG2\_LTC2975 Data Contents

BIT(S)	SYMBOL	OPERATION
b[2]	Mfr_auxfaultb_ov_fault_response_chan2	Response to channel 2 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[1]	Mfr_auxfaultb_ov_fault_response_chan1	Response to channel 1 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[0]	Mfr_auxfaultb_ov_fault_response_chan0	Response to channel 0 VOUT_OV_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.

### MFR\_CONFIG3\_LTC2975

This command register determines whether  $V_{OUT}$  undercurrent faults from a given channel cause the AUXFAULTB pin to be pulled low. This command also allows tracking to be enabled on any channel.

### MFR\_CONFIG3\_LTC2975 Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_auxfaultb_uc_fault_response_chan3	Response to channel 3 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[6]	Mfr_auxfaultb_uc_fault_response_chan2	Response to channel 2 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[5]	Mfr_auxfaultb_uc_fault_response_chan1	Response to channel 1 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[4]	Mfr_auxfaultb_uc_fault_response_chan0	Response to channel 0 IOUT_UC_FAULT. 1 = Pull AUXFAULTB low via fast pull-down. 0 = Do not pull AUXFAULTB low.
b[3]	Mfr_track_en_chan3	Select if channel 3 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.
b[2]	Mfr_track_en_chan2	Select if channel 2 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.
b[1]	Mfr_track_en_chan1	Select if channel 1 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.
b[0]	Mfr_track_en_chan0	Select if channel 0 is a slave in a tracked power supply system. 0: Channel is not a slave in a tracked power supply system. 1: Channel is a slave in a tracked power supply system. Setting this bit disables UV and UC detection during TOFF_DELAY.

## PMBUS COMMAND DESCRIPTION

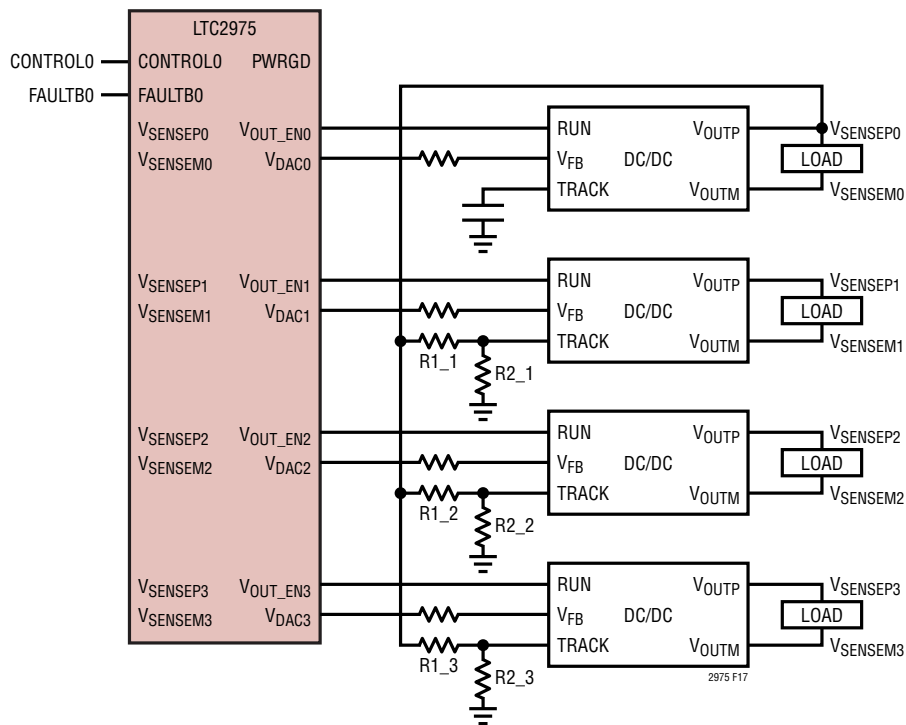


Figure 17. LTC2975 Configured to Control, Supervise and Monitor Power Supplies Equipped with Tracking Pin

### Tracking Supplies On and Off

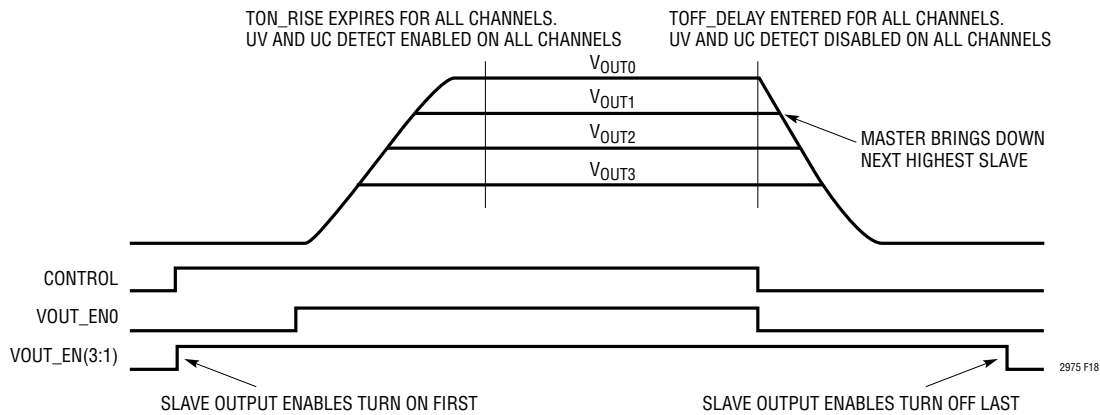
The LTC2975 supports tracking power supplies that are equipped with a tracking pin and configured for tracking. A tracking power supply uses a secondary feedback terminal (TRACK) to allow its output voltage to be scaled to an external master voltage. Typically the external voltage is generated by the supply with the highest voltage in the system, which is fed to the slave track pins (see Figure 17). Supplies that track a master supply must be enabled before the master supply comes up and disabled after the master supply comes down. Enabling the slave supplies when the master is down requires supervisors monitoring the slaves to disable UV detection. Slave UC detection must also be disabled when the slaves are tracking the master down to prevent false UC events. All channels configured for tracking must track off together in response to a fault on any channel or any other condition that can bring one or more of the channels down. Prematurely disabling a slave channel via its RUN pin may cause that channel to shut down out of sequence (see Figure 20)

An important feature of the LTC2975 is the ability to control, monitor and supervise DC/DC converters that are configured to track a master supply on and off.

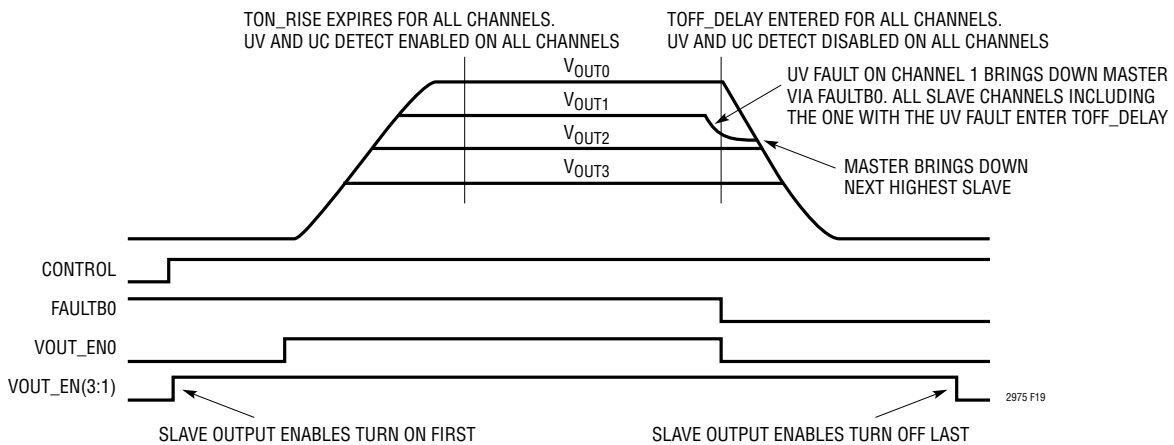
The LTC2975 supports the following tracking features:

- Track channels on and off without issuing false UV/UC events when the slave channels are tracking up or down.
- Track channels down in response to a fault from a slave or master.
- Track channels down when VIN\_SNS drops below VIN\_OFF, share clock is held low or RESTORE\_USER\_ALL is issued.
- Ability to reconfigure selected channels that are part of a tracking group to sequence up after the group has tracked up or sequence down before the group has tracked down.

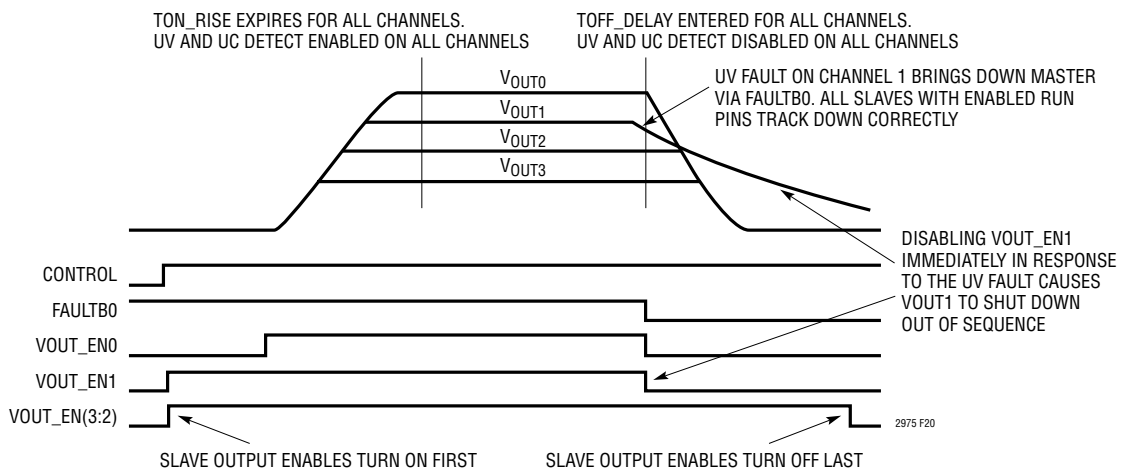
# PMBUS COMMAND DESCRIPTION



**Figure 18. Control Pin Tracking All Supplies Up And Down**



**Figure 19. Fault on Channel 1 Tracking All Supplies Down**



**Figure 20. Improperly Configured Fault Response on Faulting Channel Disrupts Tracking**

## PMBUS COMMAND DESCRIPTION

### Tracking Implementation

The LTC2975 supports tracking through the coordinated programming of Ton\_delay, Ton\_rise, Toff\_delay and Mfr\_track\_en\_chan*n*. The master channel must be configured to turn on after all the slave channels have turned on and to turn off before all the slave channels turn off. Slaves that are enabled before the master will remain off until the tracking pin allows them to turn on. Slaves will be turned off via the tracking pin even though their run pin is still asserted. Ton\_rise must be extended on the slaves so that it ends relative to the rise of the TRACK pin and not the rise of the V<sub>OUT\_EN</sub> pin.

When Mfr\_track\_en\_chan*n* is enabled the channel is reconfigured to:

- Sequence down on fault, VIN\_OFF, SHARE\_CLK low or RESTORE\_USER\_ALL.
- Ignore UV and UC during TOFF\_DELAY. Note that ignoring UV and UC during TON\_RISE and TON\_MAX\_FAULT always happens regardless of how this bit is set.

The following example illustrates configuring an LTC2975 with one master channel and three slaves.

Master channel 0

TON\_DELAY = Ton\_delay\_master

TON\_RISE = Ton\_rise\_master

TOFF\_DELAY = Toff\_delay\_master

Mfr\_track\_en\_chan0 = 0

Slave channel *n*

TON\_DELAY = Ton\_delay\_slave

TON\_RISE = Ton\_delay\_master + Ton\_rise\_slave

TOFF\_DELAY = Toff\_delay\_master + T\_off\_delay\_slave

Mfr\_track\_en\_chan0 = 1

Where:

Ton\_delay\_master – Ton\_delay\_slave > RUN to TRACK setup time

Toff\_delay\_slave > time for master supply to fall.

The system response to a control pin toggle is illustrated in Figure 18.

The system response to a UV fault on a slave channel is illustrated in Figure 19.

### ***MFR\_CONFIG\_ALL\_LTC2975***

This command is used to configure parameters that are common to all channels on the IC. They may be set or reviewed from any PAGE setting.

## PMBUS COMMAND DESCRIPTION

### MFR\_CONFIG\_ALL\_LTC2975 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:12]	Reserved	Don't care. Always returns 0.
b[11]	Mfr_config_all_pwrgrd_off_uses_uv	Selects PWRGD de-assertion source for all channels. 0: PWRGD is de-asserted based on $V_{OUT}$ being below or equal to POWER_GOOD_OFF. This option uses the ADC. Response time is approximately 100ms to 200ms. 1: PWRGD is de-asserted based on $V_{OUT}$ being below or equal to VOUT_UV_LIMIT. This option uses the high speed supervisor. Response time is approximately 12 $\mu$ s.
b[10]	Reserved	Don't care.
b[9]	Mfr_config_all_control3_pol	Selects active polarity of CONTROL3 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[8]	Mfr_config_all_control2_pol	Selects active polarity of CONTROL2 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[7]	Mfr_config_all_fault_log_enable	Enable fault logging to EEPROM in response to Fault. 0: Fault logging to EEPROM is disabled. 1: Fault logging to EEPROM is enabled.
b[6]	Mfr_config_all_vin_on_clr_faults_en	Allow VIN_ON rising edge to clear all latched faults. 0: VIN_ON clear faults feature is disabled. 1: VIN_ON clear faults feature is enabled.
b[5]	Mfr_config_all_control1_pol	Selects active polarity of CONTROL1 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[4]	Mfr_config_all_control0_pol	Selects active polarity of CONTROL0 pin 0: Active low (pull pin low to start unit). 1: Active high (pull pin high to start unit).
b[3]	Mfr_config_all_vin_share_enable	Allow this unit to hold Share-clock pin low when $V_{IN}$ has not risen above VIN_ON or has fallen below VIN_OFF. When enabled this unit will also turn all channels off in response to Share-clock being held low. 0: Share-clock inhibit is disabled. 1: Share-clock inhibit is enabled.
b[2]	Mfr_config_all_pec_en	PMBus packet error checking enable. 0: PEC is accepted but not required. 1: PEC is enabled.
b[1]	Mfr_config_all_longer_pmbus_timeout	Increase PMBus timeout interval by a factor of 8. Recommended for fault logging. 0: PMBus timeout is not multiplied by a factor of 8. 1: PMBus timeout is multiplied by a factor of 8.
b[0]	Mfr_config_all_auxfaultb_wpu_dis	AUXFAULTB charge-pumped, current-limited pull-up disable. 0: Use weak current-limited pull-up on AUXFAULTB after power-up, as long as no faults have forced AUXFAULTB off. 1: Disable weak pull-up. AUXFAULTB driver is three-stated after power-up as long as no faults have forced AUXFAULTB off.

## PMBUS COMMAND DESCRIPTION

### PROGRAMMING USER EEPROM SPACE

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	46
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	46
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	47
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	47
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	47

#### ***STORE\_USER\_ALL and RESTORE\_USER\_ALL***

STORE\_USER\_ALL, RESTORE\_USER\_ALL commands provide access to User EEPROM space. Once a command is stored in User EEPROM, it will be restored with explicit restore command, when the part emerges from power-on reset after power is applied, or after toggling the Reset pin. While either of these commands is being processed, the part will indicate it is busy, see Response When Part Is Busy on page 48.

STORE\_USER\_ALL. Issuing this command will store all operating memory commands with a corresponding EEPROM memory location.

RESTORE\_USER\_ALL. Issuing this command will restore all commands from EEPROM Memory. It is recommended that this command not be executed while a unit is enabled since all monitoring is suspended while the EEPROM is transferred to operating memory, and intermediate values from EEPROM may not be compatible with the values initially stored in operating memory.

#### **Bulk Programming the User EEPROM Space**

The MFR\_EE\_UNLOCK, MFR\_EE\_ERASE and MFR\_EE\_DATA commands provide a method for 3rd party EEPROM programming houses and end users to easily program the LTC2975 independent of any order dependencies or delays between PMBus commands. All data transfers are directly to and from the EEPROM and do not affect the volatile RAM space currently configuring the device.

The first step is to program a master reference part with the desired configuration. MFR\_EE\_UNLOCK and MFR\_EE\_DATA are then used to read back all the data in User EEPROM space as sequential words. This information is stored to the master programming HEX file. Subsequent parts may be cloned to match the master part using MFR\_EE\_UNLOCK, MFR\_EE\_ERASE and MFR\_EE\_DATA to transfer data from the master HEX file. These commands operate directly on the EEPROM independent of the part configurations stored in RAM space. During EEPROM access the part will indicate that it is busy as described below.

In order to support simple programming fixtures the bulk programming features only uses PMBus word and byte commands. The MFR\_UNLOCK configures the appropriate access mode and resets an internal address pointer allowing a series of word commands to behave as a block read or write with the address pointer being incremented after each operation. PEC use is optional and is configured by the MFR\_EE\_UNLOCK operation.

## PMBUS COMMAND DESCRIPTION

### ***MFR\_EE\_UNLOCK***

The MFR\_EE\_UNLOCK command prevents accidental EEPROM access in normal operation and configures the required EEPROM bulk programming mode for bulk initialization, sequential writes, or reads. MFR\_EE\_UNLOCK augments the protection provided by write protect. Upon unlocking the part for the required operation, an internal address pointer is reset allowing a series of MFR\_EE\_DATA reads or writes to sequentially transfer data, similar to a block read or block write. The MFR\_EE\_UNLOCK command can clear or set PEC mode based on the desired level of error protection. An MFR\_EE\_UNLOCK sequence consists of writing two or three unlock codes as described below. The following table documents the allowed sequences. Writing a non-supported sequence locks the part. Reading MFR\_EE\_UNLOCK returns the last byte written or zero if the part is locked.

#### **MFR\_EE\_UNLOCK Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_unlock[7:0]	To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC allowed: Write 0x2b followed by 0xd4.  To unlock user EEPROM space for Mfr_ee_erase and Mfr_ee_data read or write operations with PEC required: Write 0x2b followed by 0xd5.  To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC allowed: Write 0x2b, followed by 0x91 followed by 0xe4.  To unlock user and manufacturer EEPROM space for Mfr_ee_data read only operations with PEC required: Write 0x2b, followed by 0x91 followed by 0xe5.

### ***MFR\_EE\_ERASE***

The MFR\_EE\_ERASE command is used to erase the entire contents of the user EEPROM space and configures this space to accept new program data. Writing values other than 0x2B will lock the part. Reads return the last value written.

#### **MFR\_EE\_ERASE Data contents**

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_ee_erase[7:0]	To erase the user EEPROM space and configure to accept new data: 1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_erase commands with or without PEC. 2) Write 0x2B to Mfr_ee_erase.  The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.

### ***MFR\_EE\_DATA***

The MFR\_EE\_DATA command allows the user to transfer data directly to or from the EEPROM without affecting RAM space.

To read the user EEPROM space issue the appropriate Mfr\_ee\_unlock command and perform Mfr\_ee\_data reads until the EEPROM has been completely read. Extra reads will lock the part and return zero. The first read returns the 16-bit EEPROM packing revision ID that is stored in ROM. The second read returns the number of 16-bit words available; this is the number of reads or writes to access all memory locations. Subsequent reads return EEPROM data starting with lowest address.

To write to the user EEPROM space issue the appropriate Mfr\_ee\_unlock and Mfr\_ee\_erase commands followed by successive Mfr\_ee\_data word writes until the EEPROM is full. Extra writes will lock the part. The first write is to the lowest address.

Mfr\_ee\_data reads and writes must not be mixed.

## PMBUS COMMAND DESCRIPTION

### MFR\_EE\_DATA Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_ee_data[15:0]	<p>To read user space</p> <ol style="list-style-type: none"> <li>1) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC.</li> <li>2) Read Mfr_ee_data[0] = PackingId (MFR Specific ID).</li> <li>3) Read Mfr_ee_data[1] = NumberOfUserWords (total number of 16-bit word available).</li> <li>4) Read Mfr_ee_data[2] through Mfr_ee_data[NumberOfWord+1] (User EEPROM data contents)</li> </ol> <p>To write user space</p> <ol style="list-style-type: none"> <li>1) Initialize the user memory using the sequence described for the MFR_EE_ERASE command.</li> <li>2) Use the appropriate Mfr_ee_unlock sequence to configure for Mfr_ee_data commands with or without PEC.</li> <li>3) Write Mfr_ee_data[0] through Mfr_ee_data[NumberOfWord-1] (User EEPROM data content to be written)</li> </ol> <p>The part will indicate it is busy erasing the EEPROM by the mechanism detailed below.</p>

### Response When Part Is Busy

The part will indicate it is busy accessing the EEPROM by:

- 1) Asserting low the Mfr\_common\_busy of the MFR\_COMMON register. MFR\_COMMON can always be read and will never NACK a byte read request even if the part is busy.
- 2) NACKing commands other than MFR\_COMMON.
- 3) Asserting ALERTB low if any commands other than MFR\_COMMON are issued.

### MFR\_EE Erase and Write Programming Time

The program time per word is typically 0.17ms and will require spacing the I<sup>2</sup>C/SMBus writes at greater than 0.17ms to guarantee the write has completed. The Mfr\_ee\_erase command takes approximately 400ms. We recommend using MFR\_COMMON for handshaking.

### INPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	48
VIN_OFF	0x36	Input voltage below which power conversion is disabled. All V <sub>OUT_ENn</sub> pins go off immediately or sequence off after TOFF_DELAY (See Mfr_track_en_chann).	R/W Word	N	L11	V	Y	9.0 0xD240	48
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	48
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	14.0 0xD380	48
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	48
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	48

### VIN\_ON, VIN\_OFF, VIN\_OV\_FAULT\_LIMIT, VIN\_OV\_WARN\_LIMIT, VIN\_UV\_WARN\_LIMIT and VIN\_UV\_FAULT\_LIMIT

These commands provide voltage supervising limits for the input voltage V<sub>IN\_SNS</sub>.



## PMBUS COMMAND DESCRIPTION

### INPUT CURRENT AND ENERGY

COMMAND NAME		DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_EIN	0xC0	Input Energy data bytes.	R Block	N	Reg			NA	49
MFR_EIN_CONFIG	0xC1	Configuration register for energy and input current.	R/W Byte	N	Reg		Y	0x00	50
MFR_IIN_CAL_GAIN_TC	0xC3	Temperature coefficient applied to IIN_CAL_GAIN.	R/W Word	N	CF	ppm	Y	0x0000	51
MFR_IIN_CAL_GAIN	0xE8	The nominal resistance of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	1.0 0xBA00	50
MFR_CLEAR_ENERGY	0xCC	Clear MFR_EIN time and energy values.	Send Byte	N				NA	51

### Energy Measurement and Reporting

Input energy measurement and monitoring supports the following:

- Input energy derived from the accumulated product of READ\_VIN and READ\_IIN.
- Reporting input energy value as a 48-bit integer in mJ. Returning value in Joules eliminates the need for the host to manage time.
- Reporting input energy time as a 48-bit integer in ms, where input energy time is the elapsed time since energy monitoring was last reset.
- Resetting time and energy accumulators whenever MFR\_EIN\_CONFIG or MFR\_CLEAR\_ENERGY is written.
- Wrapping of time and energy accumulators when full.
- An optional HD mode allowing the user to give priority to energy measurement by forcing the ADC to measure READ\_VIN and READ\_IIN between every other ADC measurement.
- Reporting energy and time values coherently.
- Ability to decrement energy to prevent rectification and accumulation of noise when the channel is off. Energy is not allowed to decrement below zero.

### MFR\_EIN

Read only. This 12 byte data block returns the input energy value and time. Once the block read starts, MFR\_EIN updates are suspended until the block read completes. However, energy and time continue to accumulate internally during block reads.

**Table 4. MFR\_EIN Data Block Contents**

DATA	BYTE*	DESCRIPTION
Energy_value [7:0]	0	Energy Value in mJ. This is the accumulated energy since Mfr_ein_config was last written or MFR_CLEAR_ENERGY was last written.
Energy_value [15:8]	1	
Energy_value [23:16]	2	
Energy_value [31:24]	3	
Energy_value [39:32]	4	
Energy_value [47:40]	5	

## PMBUS COMMAND DESCRIPTION

Table 4. MFR\_EIN Data Block Contents

DATA	BYTE*	DESCRIPTION
Energy_time [7:0]	6	Energy Time in ms. This is the elapsed time since Mfr_ein_config or MFR_CLEAR_ENERGY was last written.
Energy_time [15:8]	7	
Energy_time [23:16]	8	
Energy_time [31:24]	9	
Energy_time [39:32]	10	
Energy_time [47:40]	11	

### MFR\_EIN\_CONFIG

This command configures energy and input current related parameters.

MFR\_EIN\_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:3]	Mfr_ein_config_reserved	Don't care. Always returns 0.
b[2]	Mfr_ein_config_hd	Optimize ADC polling sequence for higher definition input energy measurement. 0: Standard ADC polling sequence 1: Read_vin and Read_iin measurements are interleaved between every other ADC measurement.
b[1:0]	Mfr_ein_config_iin_range	Input sense amplifier range setting. 0: High Range 1: Medium Range 2: Low Range 3: Reserved The range sets the Full-Scale Input Voltage Range (FS_IIN). Lower range settings have lower input referred noise.

### MFR\_IIN\_CAL\_GAIN

The MFR\_IIN\_CAL\_GAIN command is used to set the ratio of the voltage at the input current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the sense resistor (units are expressed in mΩ). MFR\_IIN\_CAL\_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting.

Calculations using IIN\_CAL\_GAIN are:

$$\text{READ\_IIN} = \frac{V_{\text{IIN\_SNSPn}} - V_{\text{IIN\_SNSMn}}}{(\text{MFR\_IIN\_CAL\_GAIN}) \cdot T_{\text{CORRECTION}}}$$

where:

$$T_{\text{CORRECTION}} = [1 + \text{MFR\_IIN\_CAL\_GAIN\_TC} \cdot 1\text{E-}6 \cdot (\text{READ\_TEMPERATURE\_2} - 25.0)]$$

Note:

$T_{\text{CORRECTION}}$  is limited by hardware to a value between 0.25 and 4.0.

READ\_TEMPERATURE\_2 is the internal die temperature.

Mfr\_ein\_config\_iin\_range[1:0] may be used to minimize noise in systems with low sense resistor values.

## PMBUS COMMAND DESCRIPTION

### MFR\_IIN\_CAL\_GAIN\_TC

The MFR\_IIN\_CAL\_GAIN\_TC sets the temperature coefficient of the MFR\_IIN\_CAL\_GAIN register value in ppm/°C. This command uses the internal die temperature.

Refer to MFR\_IIN\_CAL\_GAIN for details on proper usage.

#### MFR\_IOUT\_CAL\_GAIN\_TC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iin_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement number. Example: Mfr_iin_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C Value = 3900

### MFR\_CLEAR\_ENERGY

This send byte command clears the accumulated energy and time value in MFR\_EIN and can be written even when the LTC2975 is write-protected with level 2 protection. The LTC2975 may internally delay the application of this command by up to  $t_{UPDATE\_ADC}$  in order to avoid corrupting an ongoing energy calculation.

## OUTPUT VOLTAGE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_MODE	0x20	Output voltage data format and mantissa exponent ( $2^{-13}$ ).	R Byte	Y	Reg			0x13	52
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	52
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	52
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	52
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	52
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	52
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	52
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	52
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and power good de-assertion.	R/W Word	Y	L16	V	Y	0.9 0x1CCD	52
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.96 0x1EB8	52
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_config_all_pwrzd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	0.94 0x1E14	52
MFR_VOUT_DISCHARGE_THRESHOLD	0xE9	Coefficient used to multiply VOUT_COMMAND in order to determine $V_{OUT}$ off threshold voltage.	R/W Word	Y	L11		Y	2.0 0xC200	52
MFR_DAC	0xE0	The code of the 10-bit DAC.	R/W Word	Y	Reg			0x0000	52

## PMBUS COMMAND DESCRIPTION

### *VOUT\_MODE*

This command is read only and specifies the mode and exponent for all commands with a L16 data format. See Data Formats on page 27.

#### **VOUT\_MODE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:5]	Vout_mode_type	Reports linear mode. Hard-wired to 000b.
b[4:0]	Vout_mode_parameter	Linear mode exponent. 5-bit two's complement integer. Hardwired to 0x13 (-13 decimal).

### *VOUT\_COMMAND, VOUT\_MAX, VOUT\_MARGIN\_HIGH, VOUT\_MARGIN\_LOW, VOUT\_OV\_FAULT\_LIMIT, VOUT\_OV\_WARN\_LIMIT, VOUT\_UV\_WARN\_LIMIT, VOUT\_UV\_FAULT\_LIMIT, POWER\_GOOD\_ON and POWER\_GOOD\_OFF*

These commands provide various servo, margining and supervising limits for a channel's output voltage.

### *MFR\_VOUT\_DISCHARGE\_THRESHOLD*

This register contains the coefficient that multiplies VOUT\_COMMAND in order to determine the OFF threshold voltage for the associated output. If the output voltage has not decayed below MFR\_VOUT\_DISCHARGE\_THRESHOLD • VOUT\_COMMAND prior to the channel being commanded to enter/re-enter the ON state, the Status\_mfr\_discharge bit in the STATUS\_MFR\_SPECIFIC register will be set and the ALERTB pin will be asserted low. In addition, the channel will not enter the ON state until the output has decayed below its off-threshold voltage. Setting this to a value greater than 1.0 effectively disables DISCHARGE\_THRESHOLD checking, allowing the channel to turn back on even if it has not decayed at all.

Other channels can be held-off if a particular output has failed to discharge by using the bidirectional FAULTB<sub>n</sub> pins (refer to the MFR\_FAULTB<sub>n</sub>\_RESPONSE and MFR\_FAULTB<sub>n</sub>\_PROPOGATE registers).

### *MFR\_DAC*

This command register allows the user to directly program the 10-bit DAC. Manual DAC writes require the channel to be in the ON state, TON\_RISE to have expired and MFR\_CONFIG\_LTC2975 b[5:4] = 10b or 11b. Writing MFR\_CONFIG\_LTC2975 b[5:4] = 10b commands the DAC to hard connect with the value in Mfr\_dac\_direct\_val. Writing b[5:4] = 11b commands the DAC to soft connect. Once the DAC has soft connected, Mfr\_dac\_direct\_val returns the value that allowed the DAC to be connected without perturbing the power supply. MFR\_DAC writes are ignored when MFR\_CONFIG\_LTC2975 b[5:4] = 00b or 01b.

#### **MFR\_DAC Data Contents**

BIT(S)	SYMBOL	OPERATION
b[15:10]	Reserved	Read only, always returns 0.
b[9:0]	Mfr_dac_direct_val	DAC code value.

## PMBUS COMMAND DESCRIPTION

### OUTPUT CURRENT COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	53
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	10.0 0xD280	53
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	5.0 0xCA80	53
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	-1.0 0xB400	53
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient applied to IOUT_CAL_GAIN.	R/W Word	Y	CF	ppm	Y	0x0000	53

#### ***IOUT\_CAL\_GAIN***

The IOUT\_CAL\_GAIN command is used to set the ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the same value as the resistance of the resistor (units are expressed in mΩ). IOUT\_CAL\_GAIN is internally limited to values between 0.01mΩ to 1,000mΩ. The register readback value always returns what was last written and does not reflect internal limiting.

Calculations using IOUT\_CAL\_GAIN are:

$$V_{IOUT\_OC\_FAULT\_LIMIT} = IOUT\_OC\_FAULT\_LIMIT \cdot IOUT\_CAL\_GAIN \cdot T_{CORRECTION}$$

$$V_{IOUT\_UC\_FAULT\_LIMIT} = IOUT\_UC\_FAULT\_LIMIT \cdot IOUT\_CAL\_GAIN \cdot T_{CORRECTION}$$

where:

$$T_{CORRECTION} = (1 + MFR\_IOUT\_CAL\_GAIN\_TC \cdot 1E-6 \cdot (READ\_TEMPERATURE\_1 + MFR\_T\_SELF\_HEAT - 25.0))$$

$$READ\_IOUT = \frac{V_{IOUT\_SNSPn} - V_{IOUT\_SNSMn}}{(IOUT\_CAL\_GAIN) \cdot T_{CORRECTION}}$$

Note:

T<sub>CORRECTION</sub> is limited by hardware to a value between 0.25 and 4.0.

READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated T<sub>SENSE</sub> network fails to detect a valid temperature. See READ\_TEMPERATURE\_1 for more information.

#### ***IOUT\_OC\_FAULT\_LIMIT, IOUT\_OC\_WARN\_LIMIT and IOUT\_UC\_FAULT\_LIMIT***

I<sub>OUT</sub> supervisor fault and warning limits.

IOUT\_OC\_FAULT\_LIMIT is internally limited to values greater or equal to zero. The register readback value always returns what was last written and does not reflect internal limiting.

IOUT\_UC\_FAULT\_LIMIT is internally limited to values less than zero. The register readback value always returns what was last written and does not reflect internal limiting.

#### ***MFR\_IOUT\_CAL\_GAIN\_TC***

## PMBUS COMMAND DESCRIPTION

The MFR\_IOUT\_CAL\_GAIN\_TC is a paged command that sets the temperature coefficient of the IOUT\_CAL\_GAIN register value in ppm/°C. This command uses the temperature measured by the external temperature diode for the associated page.

Refer to IOUT\_CAL\_GAIN for details on proper usage.

### MFR\_IOUT\_CAL\_GAIN\_TC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_cal_gain_tc	16-bit twos complement integer representing the temperature coefficient. Value = Y where Y = b[15:0] is a twos complement. Example: Mfr_iout_cal_gain_tc = 3900ppm For b[15:0] = 0x0F3C Value = 3900

### EXTERNAL TEMPERATURE COMMANDS AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	55
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	55
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	55
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	-5.0 0xCD80	55
MFR_TEMP_1_GAIN	0xF8	Inverse of external diode temperature non ideality factor. One LSB = 2 <sup>-14</sup> .	R/W Word	Y	CF		Y	1 0x4000	55
MFR_TEMP_1_OFFSET	0xF9	Offset value for the external temperature.	R/W Word	Y	L11	°C	Y	0 0x8000	55
MFR_T_SELF_HEAT	0xB8	Calculated temperature rise due to self-heating of output current sense device above value measured by external temperature sensor.	R Word	Y	L11	°C		NA	55
MFR_IOUT_CAL_GAIN_TAU_INV	0xB9	Inverse of time constant for Mfr_t_self_heat changes scaled by 4 • tCONV_SENSE.	R/W Word	Y	L11		Y	0.0 0x8000	55
MFR_IOUT_CAL_GAIN_THETA	0xBA	Thermal resistance from inductor core to point measured by external temperature sensor.	R/W Word	Y	L11	°C/W	Y	0.0 0x8000	55

## PMBUS COMMAND DESCRIPTION

### *OT\_FAULT\_LIMIT, OT\_WARN\_LIMIT, UT\_WARN\_LIMIT and UT\_FAULT\_LIMIT*

These commands provide supervising limits for temperature as measured by the external diode.

### *MFR\_TEMP\_1\_GAIN and MFR\_TEMP\_1\_OFFSET*

The MFR\_TEMP\_1\_GAIN command specifies the inverse of the temperature sensor ideality factor. The MFR\_TEMP\_1\_OFFSET allows an offset to be applied to the measured temperature.

Calculations using these paged commands are:

$$\text{READ\_TEMPERATURE\_1} = T_{\text{EXT}} \cdot \text{MFR\_TEMP\_1\_GAIN} - 273.15 + \text{MFR\_TEMP\_1\_OFFSET}$$

where:

$$T_{\text{EXT}} = \text{Measured external temperature in degrees Kelvin.}$$

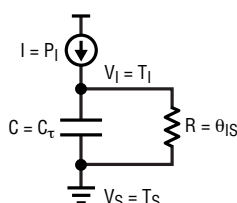
READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated T\_SENSE network fails to detect a valid temperature. Under these conditions MFR\_TEMP\_1\_GAIN and MFR\_TEMP\_1\_OFFSET will have no effect. See READ\_TEMPERATURE\_1 for more information.

### MFR\_TEMP\_1\_GAIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_temp_1_gain[15:0]	16-bit integer representing inverse of temperature non-ideality factor. Value = $Y \cdot 2^{14}$ where $Y = b[15:0]$ is an unsigned integer. Example: MFR_TEMP_1_GAIN = 1.0 For b[15:0] = 0x4000 Value = $16384 \cdot 2^{-14} = 1.0$

### *MFR\_T\_SELF\_HEAT, MFR\_IOUT\_CAL\_GAIN\_TAU\_INV and MFR\_IOUT\_CAL\_GAIN\_THETA*

The LTC2975 uses an innovative (patent pending) algorithm to dynamically model the temperature rise from the external temperature sensor to the inductor core. This temperature rise is called MFR\_T\_SELF\_HEAT and is used to calculate the final temperature correction required by IOUT\_CAL\_GAIN. The temperature rise is a function of the power dissipated in the inductor DCR, the thermal resistance from the inductor core to the remote temperature sensor and the thermal time constant of the inductor to board system. The algorithm simplifies the placement requirements for the external temperature sensor and compensates for the significant steady state and transient temperature error from the inductor core to the primary inductor heat sink.



- $P_l$  = CURRENT REPRESENTING THE POWER DISSIPATED BY THE INDUCTOR ( $V_{\text{DCR}} \cdot \text{READ\_IOUT}$  WHERE  $V_{\text{DCR}} = (V_{\text{ISENSEP}} - V_{\text{ISENSM}})$ )
- $C_\tau$  = CAPACITANCE REPRESENTING THERMAL HEAT CAPACITY OF THE INDUCTOR (INCLUDED IN MFR\_IOUT\_CAL\_GAIN\_TAU\_INV)
- $T_l$  = VOLTAGE REPRESENTING THE TEMPERATURE OF THE INDUCTOR
- $\theta_{lS}$  = RESISTANCE REPRESENTING THE THERMAL RESISTANCE FROM THE DCR TO THE REMOTE TEMPERATURE SENSOR (MFR\_IOUT\_CAL\_GAIN\_THETA)
- $T_S$  = VOLTAGE REPRESENTING THE TEMPERATURE AT THE REMOTE TEMPERATURE SENSOR

2975 F21

Figure 21. Electronic Analogy for Inductor Temperature Model

## PMBUS COMMAND DESCRIPTION

The best way to understand the self-heating effect inside the inductor is to model the system using the circuit analogy of Figure 21. The 1st order differential equation for the above model may be approximated by the following difference equation:

$$P_I - T_I/\theta_{IS} = C_\tau \Delta T_I/\Delta t \text{ (Eq1) (when } T_S = 0)$$

from which:

$$\Delta T_I = \Delta t (P_I \theta_{IS} - T_I)/(\theta_{IS} C_\tau) \text{ (Eq2) or}$$

$$\Delta T_I = (P_I \theta_{IS} - T_I) \cdot \tau_{INV} \text{ (Eq3)}$$

where

$$\tau_{INV} = \Delta t/(\theta_{IS} C_\tau) \text{ (Eq4)}$$

and  $\Delta t$  is the sample period of the external temperature ADC.

The LTC2975 implements the self-heating algorithm using Eq3 and Eq4 where:

$$\Delta T_I = \Delta MFR\_T\_SELF\_HEAT$$

$$P_I = READ\_IOUT \cdot (V_{ISENSEP} - V_{ISENSEM})$$

$$T_S = READ\_TEMPERATURE\_1$$

$$T_I = MFR\_T\_SELF\_HEAT + T_S$$

$$\Delta t = 4 \cdot t_{CONV\_SENSE} \text{ (One complete external temperature loop period)}$$

$$\tau_{INV} = MFR\_IOUT\_CAL\_GAIN\_TAU\_INV$$

$$\theta_{IS} = MFR\_IOUT\_CAL\_GAIN\_THETA$$

Initially self heat is set to zero. After each temperature measurement self heat is updated to be the previous value of self heat incremented or decremented by  $\Delta MFR\_T\_SELF\_HEAT$ .

The actual value of  $C_\tau$  is not required. The important quantity is the thermal time constant  $\tau_{INV} = (\theta_{IS} C_\tau)$ . For example, if an inductor has a thermal time constant  $\tau_{INV} = 5$  seconds then:

$$MFR\_IOUT\_CAL\_GAIN\_TAU\_INV = (4 \cdot t_{CONV\_SENSE})/5 = 4 \cdot 66\text{ms}/5\text{s} = 0.0528$$

Refer to the application section for more information on calibrating  $\theta_{IS}$  and  $\tau_{INV}$ .

READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated  $T_{SENSE}$  network fails to detect a valid temperature. Under these conditions  $T_S = READ\_TEMPERATURE\_2$  and the self-heating correction is applied using the internal die temperature. See READ\_TEMPERATURE\_1 for more information.

### MFR\_T\_SELF\_HEAT Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_t_self_heat	Values are limited to the range 0°C to 50°C.

### MFR\_IOUT\_CAL\_GAIN\_THETA Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_iout_cal_gain_theta	Values $\leq 0$ set MFR_T_SELF_HEAT to zero.



## PMBUS COMMAND DESCRIPTION

### MFR\_IOUT\_CAL\_GAIN\_TAU\_INV Data Content

Bit(s)	Symbol	Operation
b[15:0]	Mfr_iout_cal_gain_tau_inv	Values $\leq 0$ set MFR_T_SELF_HEAT to zero. Values $\geq 1$ set MFR_T_SELF_HEAT to $MFR\_IOUT\_CAL\_GAIN\_THETA \cdot READ\_IOUT \cdot (V_{ISENSEP} - V_{ISENSEM})$ .

### SEQUENCING TIMING LIMITS AND CLOCK SHARING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to $V_{OUT\_ENn}$ pin = ON.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	57
TON_RISE	0x61	Time from when the $V_{OUT\_ENn}$ pin goes high until the LTC2975 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	ms	Y	10.0 0xD280	57
TON_MAX_FAULT_LIMIT	0x62	Maximum time from $V_{OUT\_ENn}$ = ON assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	ms	Y	15.0 0xD3C0	57
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to $V_{OUT\_ENn}$ pin = OFF.	R/W Word	Y	L11	ms	Y	1.0 0xBA00	57
MFR_RESTART_DELAY	0xDC	Delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W Word	N	L11	ms	Y	400 0xFB20	58

#### ***TON\_DELAY, TON\_RISE, TON\_MAX\_FAULT\_LIMIT and TOFF\_DELAY***

These commands share the same format and provide sequencing and timer fault and warning delays in ms.

TON\_DELAY sets the amount of time in milliseconds that a channel waits following the start of an ON sequence before its  $V_{OUT\_EN}$  pin enables a DC/DC converter. This delay is counted using SHARE\_CLK only.

TON\_RISE sets the amount of time in ms that elapses after the power supply has been enabled until the LTC2975's DAC soft connects and servos the output voltage to the desired level if Mfr\_dac\_mode = 00b. This delay is counted using SHARE\_CLK only.

TON\_MAX\_FAULT\_LIMIT is the maximum amount of time that the power supply being controlled by the LTC2975 can attempt to power up the output without reaching the  $V_{OUT\_UV\_FAULT\_LIMIT}$ . If it does not, then a TON\_MAX\_FAULT is declared. If the output reaches  $V_{OUT\_UV\_FAULT\_LIMIT}$  prior to TON\_MAX\_FAULT\_LIMIT, the LTC2975 unmask the  $V_{OUT\_UV\_FAULT\_LIMIT}$  threshold. (Note that a value of zero means there is no limit to how long the power supply can attempt to bring up its output voltage.) This delay is counted using SHARE\_CLK only.

TOFF\_DELAY is the amount of time that elapses after the CONTROL pin and/or OPERATION command is de-asserted until the channel is disabled (soft-off). This delay is counted using SHARE\_CLK if available, otherwise the internal oscillator is used.

All of the above TON and TOFF delays are internally limited to 655ms, and rounded to the nearest 10 $\mu$ s. The read value of these commands always returns what was last written and does not reflect internal limiting.

## PMBUS COMMAND DESCRIPTION

### MFR\_RESTART\_DELAY

This command essentially sets the off time of a CONTROL pin initiated restart. If the CONTROL pin is toggled off for at least 10 $\mu$ s then on, all dependent channels are disabled, held off for a time = Mfr\_restart\_delay, then sequenced back on. CONTROL pin transitions whose OFF time exceeds Mfr\_restart\_delay are not affected by this command. A value of all zeros disables this feature. This delay is counted using SHARE\_CLK only.

This delay is internally limited to 13.1 seconds, and rounded to the nearest 200 $\mu$ s. The read value of this command always returns what was last written and does not reflect internal limiting.

### Clock Sharing

Multiple ADI PMBus devices can synchronize their clocks in an application by connecting together the open-drain SHARE\_CLK input/outputs to a pull-up resistor as a wired OR. In this case the fastest clock will take over and synchronize all other chips to its falling edge.

SHARE\_CLK can optionally be used to synchronize ON/OFF dependency on  $V_{IN}$  across multiple chips by setting the Mfr\_config\_all\_vin\_share\_enable bit of the MFR\_CONFIG\_ALL register. When configured this way the chip will hold SHARE\_CLK low when the unit is off for insufficient input voltage, and upon detecting that SHARE\_CLK is held low the chip will disable all channels after a brief deglitch period. When the SHARE\_CLK pin is allowed to rise, the chip will respond by beginning a start sequence. In this case the slowest VIN\_ON detection will take over and synchronize other chips to its start sequence.

### WATCHDOG TIMER AND POWER GOOD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_PWRGD_EN	0xD4	Configuration that maps WDI/RESETB status and individual channel power good to the PWRGD pin.	R/W Word	N	Reg		Y	0x0000	58
MFR_POWERGOOD_ASSERTION_DELAY	0xE1	Power-good output assertion delay.	R/W Word	N	L11	ms	Y	100 0xEB20	59
MFR_WATCHDOG_T_FIRST	0xE2	First watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	59
MFR_WATCHDOG_T	0xE3	Watchdog timer interval.	R/W Word	N	L11	ms	Y	0 0x8000	59

### MFR\_PWRGD\_EN

This command register controls the mapping of the watchdog and channel power good status to the PWRGD pin.

#### MFR\_PWRGD\_EN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:9]	Reserved	Read only, always returns 0s.
b[8]	Mfr_pwrgd_en_wdog	Watchdog. 1 = Watchdog timer not-expired status is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = Watchdog timer does not affect the PWRGD pin.
b[7:4]	Reserved	Always returns 0000b.
b[3]	Mfr_pwrgd_en_chan3	Channel 3. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

## PMBUS COMMAND DESCRIPTION

### MFR\_PWRGD\_EN Data Contents

BIT(S)	SYMBOL	OPERATION
b[2]	Mfr_pwrgd_en_chan2	Channel 2. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[1]	Mfr_pwrgd_en_chan1	Channel 1. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.
b[0]	Mfr_pwrgd_en_chan0	Channel 0. 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PWRGD status for this channel does not affect the PWRGD pin.

### MFR\_POWERGOOD\_ASSERTION\_DELAY

This command register allows the user to program the delay from when the internal power-good signal becomes valid until the power-good output is asserted. This delay is counted using SHARE\_CLK if available, otherwise the internal oscillator is used. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200 $\mu$ s. The read value of this command always returns what was last written and does not reflect internal limiting.

The power good de-assertion delay and threshold source is controlled by Mfr\_config\_all\_pwrgd\_off\_uses\_uv. Systems that require a fast power good de-assertion should set Mfr\_config\_all\_pwrgd\_off\_uses\_uv = 1. This uses the VOUT\_UV\_FAULT\_LIMIT and the high speed comparator to de-assert the PWRGD pin. Systems that require a separate power good off threshold should set Mfr\_config\_all\_pwrgd\_off\_uses\_uv = 0. This uses the slower ADC polling loop and POWER\_GOOD\_OFF to de-assert the PWRGD pin.

### Watchdog Operation

A non-zero write to the MFR\_WATCHDOG\_T register will reset the watchdog timer. Low-to-high transitions on the WDI/RESETB pin also reset the watchdog timer. If the timer expires, ALERTB is asserted and the PWRGD output is optionally de-asserted and then reasserted after MFR\_PWRGD\_ASSERTION\_DELAY ms. Writing 0 to either the MFR\_WATCH\_DOG\_T or MFR\_WATCHDOG\_T\_FIRST registers will disable the timer.

### MFR\_WATCHDOG\_T\_FIRST and MFR\_WATCHDOG\_T

The MFR\_WATCHDOG\_T\_FIRST register allows the user to program the duration of the first watchdog timer interval following assertion of the PWRGD pin, assuming the PWRGD pin reflects the status of the watchdog timer. If assertion of PWRGD is not conditioned by the watchdog timer's status, then MFR\_WATCHDOG\_T\_FIRST applies to the first timing interval after the timer is enabled. Writing a value of 0ms to the MFR\_WATCHDOG\_T\_FIRST register disables the watchdog timer. This delay is internally limited to 65 seconds and rounded to the nearest 1ms.

The MFR\_WATCHDOG\_T register allows the user to program watchdog timer intervals subsequent to the MFR\_WATCHDOG\_T\_FIRST timing interval. Writing a value of 0ms to the MFR\_WATCHDOG\_T register disables the watchdog timer. This delay is internally limited to 655ms and rounded to the nearest 10 $\mu$ s.

Both timers operate on an internal clock independent of SHARE\_CLK. The read value of both commands always returns what was last written and does not reflect internal limiting.

## PMBUS COMMAND DESCRIPTION

### FAULT RESPONSES

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	60
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	60
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	61
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	61
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	62
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	62
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	62
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	62
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	63
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	N	L11	ms	Y	200 0xF320	63
MFR_RETRY_COUNT	0xF7	Retry count for all faulted off conditions that enable retry.	R/W Byte	N	Reg		Y	0x07	63

### Clearing Latched Faults

Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the  $V_{IN\_SNS}$  pin. All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR\_FAULTS command resets the contents of the status registers and de-asserts the ALERTB output. The CLEAR\_FAULTS does not clear a faulted off state nor allow a channel to turn back on.

### VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE

The fault response documented here is for voltages that are measured by the high speed supervisor. These voltages are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTC2975 will also:

- Set the appropriate bit(s) in the STATUS\_BYTE.
- Set the appropriate bit(s) in the STATUS\_WORD.
- Set the appropriate bit in the corresponding STATUS\_VOUT register, and
- Notify the host by pulling the ALERTB pin low.

## PMBUS COMMAND DESCRIPTION

### VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Vout_ov_fault_response_action, Vout_uv_fault_response_action	<p>Response action:</p> <p>00b: The unit continues operation without interruption.</p> <p>01b: The unit continues operating for the delay time specified by bits[2:0] in increments of <math>t_{S\_VS}</math>. See Electrical Characteristics Table. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].</p> <p>10b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].</p>
b[5:3]	Vout_ov_fault_response_retry, Vout_uv_fault_response_retry	<p>Response retry behavior:</p> <p>000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.</p> <p>001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.</p> <p>Changing the value might not take effect until the next off-then-on sequence on that channel.</p>
b[2:0]	Vout_ov_fault_response_delay, Vout_uv_fault_response_delay	<p>This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults.</p> <p>000b: There is no additional deglitch delay applied to fault detection.</p> <p>001b-111b: The fault is deglitched for deglitch period of b[2:0] samples at a sampling period of <math>t_{S\_VS}</math> (12.2<math>\mu</math>s typical).</p>

### IOUT\_OC\_FAULT\_RESPONSE and IOUT\_UC\_FAULT\_RESPONSE

The fault response documented here is for currents that are measured by the high speed supervisor. These currents are measured over a short period of time and may require a deglitch period. Note that in addition to the response described by these commands, the LTC2975 will also:

- Set the appropriate bit in the STATUS\_BYTE.
- Set the appropriate bit in the STATUS\_WORD.
- Set the appropriate bit in the corresponding STATUS\_IOUT register, and
- Notify the host by pulling the ALERTB pin low.

### IOUT\_OC\_FAULT\_RESPONSE and IOUT\_UC\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Iout_oc_fault_response_action, Iout_uc_fault_response_action	<p>Response action:</p> <p>00b and 01b: The unit continues operation without interruption. Note that the current will not be limited to the value of Iout_oc_fault_limit or Iout_uc_fault_limit.</p> <p>10b: The unit continues operating for the delay time specified by bits [2:0]. If the fault is still present at the end of the delay time, the unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3]. Note that the current will not be limited to the value of Iout_oc_fault_limit or Iout_uc_fault_limit.</p> <p>11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].</p>

## PMBUS COMMAND DESCRIPTION

### IOUT\_OC\_FAULT\_RESPONSE and IOUT\_UC\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION																
b[5:3]	lout_oc_fault_response_retry, lout_uc_fault_response_retry	<p>Response retry behavior:</p> <p>000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.</p> <p>001-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded off (by the control pin or operation command or both), bias power is removed, or another fault condition causes the unit to shut down.</p> <p>Changing the value might not take effect until the next off-then-on sequence on that channel.</p>																
b[2:0]	lout_oc_fault_response_delay, lout_uc_fault_response_delay	<p>This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to deglitch fast faults.</p> <p>000b: There is no additional deglitch delay applied to fault detection.</p> <p>001b-111b: The fault is deglitched for the interval selected by b[2:0] as follows.</p> <table border="1"> <thead> <tr> <th>b[2:0]</th> <th>Deglitch interval</th> </tr> </thead> <tbody> <tr> <td>001b</td> <td>100µs</td> </tr> <tr> <td>010b</td> <td>1ms</td> </tr> <tr> <td>011b</td> <td>5ms</td> </tr> <tr> <td>100b</td> <td>10ms</td> </tr> <tr> <td>101b</td> <td>20ms</td> </tr> <tr> <td>110b</td> <td>50ms</td> </tr> <tr> <td>111b</td> <td>100ms</td> </tr> </tbody> </table>	b[2:0]	Deglitch interval	001b	100µs	010b	1ms	011b	5ms	100b	10ms	101b	20ms	110b	50ms	111b	100ms
b[2:0]	Deglitch interval																	
001b	100µs																	
010b	1ms																	
011b	5ms																	
100b	10ms																	
101b	20ms																	
110b	50ms																	
111b	100ms																	

### OT\_FAULT\_RESPONSE, UT\_FAULT\_RESPONSE, VIN\_OV\_FAULT\_RESPONSE and VIN\_UV\_FAULT\_RESPONSE

The fault response documented here is for values that are measured by the ADC. Note that in addition to the response described by these commands, the LTC2975 will also:

- Set the appropriate bit(s) in the STATUS\_BYTE.
- Set the appropriate bit(s) in the STATUS\_WORD.
- Set the appropriate bit in the corresponding STATUS\_VIN or STATUS\_TEMPERATURE register, and
- Notify the host by pulling the ALERTB pin low.

### OT\_FAULT\_RESPONSE, UT\_FAULT\_RESPONSE, VIN\_OV\_FAULT\_RESPONSE, VIN\_UV\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ot_fault_response_action, Ut_fault_response_action, Vin_ov_fault_response_action, Vin_uv_fault_response_action	<p>Response action:</p> <p>00b: The unit continues operation without interruption.</p> <p>01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].</p>
b[5:3]	Ot_fault_response_retry, Ut_fault_response_retry, Vin_ov_fault_response_retry, Vin_uv_fault_response_retry	<p>Response retry behavior:</p> <p>000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.</p> <p>001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.</p> <p>Changing the value might not take effect until the next off-then-on sequence on that channel.</p>
b[2:0]	Ot_fault_response_delay, Ut_fault_response_delay, Vin_ov_fault_response_delay, Vin_uv_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

## PMBUS COMMAND DESCRIPTION

### TON\_MAX\_FAULT\_RESPONSE

This command defines the LTC2975 response to a TON\_MAX\_FAULT. It may be used to protect against a short-circuited output at startup. After startup use VOUT\_UV\_FAULT\_RESPONSE to protect against a short-circuited output.

The device also:

- Sets the HIGH\_BYTE bit in the STATUS\_BYTE,
- Sets the VOUT bit in the STATUS\_WORD,
- Sets the TON\_MAX\_FAULT bit in the STATUS\_VOUT register, and
- Notifies the host by asserting ALERTB.

#### TON\_MAX\_FAULT\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ton_max_fault_response_action	Response action: 00b: The unit continues operation without interruption. 01b-11b: The unit shuts down immediately or sequences off after TOFF_DELAY (See Mfr_track_en_chann). After shutting down, the device responds according to the retry settings in bits [5:3].
b[5:3]	Ton_max_fault_response_retry	Response retry behavior: 000b: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 001b-111b: The PMBus device attempts to restart the number of times specified by the global Mfr_retry_count[2:0] until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Changing the value might not take effect until the next off-then-on sequence on that channel.
b[2:0]	Ton_max_fault_response_delay	Hard coded to 000b: There is no additional deglitch delay applied to fault detection.

### MFR\_RETRY\_DELAY

This command determines the retry interval when the LTC2975 is in retry mode in response to a fault condition. This delay is counted using SHARE\_CLK only. This delay is internally limited to 13.1 seconds, and rounded to the nearest 200µs. The read value of this command always returns what was last written and does not reflect internal limiting.

### MFR\_RETRY\_COUNT

The MFR\_RETRY\_COUNT is a global command that sets the number of retries attempted when any channel faults off with its fault response retry field set to a non zero value.

In the event of multiple or recurring retry faults on the same channel the total number of retries equals MFR\_RETRY\_COUNT. If a channel has not been faulted off for at least 16 seconds, its retry counter is cleared. Toggling a channel's CONTROL pin off then on or issuing OPERATION off then on commands will synchronously clear the retry count.

#### MFR\_RETRY\_COUNT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:3]	Reserved	Always returns zero.
b[2:0]	Mfr_retry_count [2:0]	0: No retries: 1-6: Number of retries. 7: Infinite retries. Changing the value might not take effect until the next off-then-on sequence on that channel.

## PMBUS COMMAND DESCRIPTION

### SHARED EXTERNAL FAULTS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULTB0_PROPAGATE	0xD2	Configuration that determines if a channel's faulted off state is propagated to the FAULTB0 pin.	R/W Byte	Y	Reg		Y	0x00	64
MFR_FAULTB1_PROPAGATE	0xD3	Configuration that determines if a channel's faulted off state is propagated to the FAULTB1 pin.	R/W Byte	Y	Reg		Y	0x00	64
MFR_FAULTB0_RESPONSE	0xD5	Action to be taken by the device when the FAULTB0 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	64
MFR_FAULTB1_RESPONSE	0xD6	Action to be taken by the device when the FAULTB1 pin is asserted low.	R/W Byte	N	Reg		Y	0x00	64

#### ***MFR\_FAULTB0\_PROPAGATE and MFR\_FAULTB1\_PROPAGATE***

These manufacturer specific commands enable channels that have faulted off to propagate that state to the appropriate fault pin. MFR\_FAULTB0\_PROPAGATE allows any channel's faulted off state to propagate to the FAULTB0 pin. MFR\_FAULTB1\_PROPAGATE allows any channel's faulted off state to propagate to the FAULTB1 pin.

Note that pulling a fault pin low will have no effect for channels that have MFR\_FAULTBn\_RESPONSE set to 0. The channel continues operation without interruption. This fault response is called Ignore (0x0) in LTpowerPlay.

#### **MFR\_FAULT0\_PROPAGATE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb0_propagate	Enable fault propagation. 0: Channel's faulted off state does not assert FAULTB0 low. 1: Channel's faulted off state asserts FAULTB0 low.

#### **MFR\_FAULT1\_PROPAGATE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb1_propagate	Enable fault propagation. 0: Channel's faulted off state does not assert FAULTB1 low. 1: Channel's faulted off state asserts FAULTB1 low.

#### ***MFR\_FAULTB0\_RESPONSE and MFR\_FAULTB1\_RESPONSE***

These manufacturer specific commands share the same format and specify the response to assertions of the FAULTB pins. MFR\_FAULTB0\_RESPONSE determines which channels shut off when the FAULTB0 pin is asserted low and MFR\_FAULTB1\_RESPONSE determines which channels shut off when the FAULTB1 pin is asserted low. When a channel shuts off in response to a FAULTBn pin, the ALERTB pin is asserted low and the appropriate bit is set in the STATUS\_MFR\_SPECIFIC register. For a graphical explanation, see the switches on the left hand side of Figure 32: Channel Fault Management Block Diagram.

Faults will not propagate for channels that have MFR\_FAULTBn\_RESPONSE set to 0: The channel continues operation without interruption. Note that this fault response is called No Action in LTpowerPlay.



## PMBUS COMMAND DESCRIPTION

### MFR\_FAULTB0\_RESPONSE and MFR\_FAULTB1\_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Read only, always returns 0000b.
b[3]	Mfr_faultb0_response_chan3, Mfr_faultb1_response_chan3	Channel 3 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10 $\mu$ s. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[2]	Mfr_faultb0_response_chan2, Mfr_faultb1_response_chan2	Channel 2 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10 $\mu$ s. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[1]	Mfr_faultb0_response_chan1, Mfr_faultb1_response_chan1	Channel 1 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10 $\mu$ s. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[0]	Mfr_faultb0_response_chan0, Mfr_faultb1_response_chan0	Channel 0 response. 0: The channel continues operation without interruption 1: The channel shuts down if the corresponding FAULTB pin is still asserted after 10 $\mu$ s. When the FAULTB pin subsequently de-asserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.

### FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	65
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	66
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	66
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	67
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	67
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	67
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	68
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	68
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	68
MFR_PADS	0xE5	Current state of selected digital I/O pads.	R Word	N	Reg			NA	69
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	70

### CLEAR\_FAULTS

The CLEAR\_FAULTS command is used to clear status bits that have been set. This command clears all fault and warning bits in all unpagged status registers, and pagged status registers selected by the current PAGE setting. At the same time, the device negates (clears, releases) its contribution to ALERTB.

The CLEAR\_FAULTS command does not cause a unit that has latched off for a fault condition to restart. See Clearing Latched Faults for more information.

If the fault is present after the fault is cleared, the fault status bit will be set again and the host notified by the usual means.

Note: this command responds to the global page command. (PAGE=0xFF)

## PMBUS COMMAND DESCRIPTION

### STATUS\_BYTE

The STATUS\_BYTE command returns the summary of the most critical faults or warnings which have occurred, as shown in the following table. STATUS\_BYTE is a subset of STATUS\_WORD and duplicates the same information.

#### STATUS\_BYTE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_byte_busy	Same as Status_word_busy.
b[6]	Status_byte_off	Same as Status_word_off.
b[5]	Status_byte_vout_ov	Same as Status_word_vout_ov.
b[4]	Status_byte_iout_oc	Same as Status_word_iout_oc.
b[3]	Status_byte_vin_uv	Same as Status_word_vin_uv.
b[2]	Status_byte_temp	Same as Status_word_temp.
b[1]	Status_byte_cml	Same as Status_word_cml.
b[0]	Status_byte_high_byte	Same as Status_word_high_byte.

### STATUS\_WORD

The STATUS\_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate detailed status register.

The low byte of the STATUS\_WORD is the same register as the STATUS\_BYTE command.

#### STATUS\_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Status_word_vout	An output voltage fault or warning has occurred. See STATUS_VOUT.
b[14]	Status_word_iout	An output current fault or warning has occurred. See STATUS_IOUT.
b[13]	Status_word_input	An input voltage fault or warning has occurred. See STATUS_INPUT.
b[12]	Status_word_mfr	A manufacturer specific fault has occurred. See STATUS_MFR_SPECIFIC.
b[11]	Status_word_power_not_good	The PWRGD pin, if enabled, is negated. Power is not good.
b[10]	Status_word_fans	Not supported. Always returns 0.
b[9]	Status_word_other	Not supported. Always returns 0.
b[8]	Status_word_unknown	Not supported. Always returns 0.
b[7]	Status_word_busy	Device busy when PMBus command received. See OPERATION: Processing Commands.
b[6]	Status_word_off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. The off-bit is clear if unit is allowed to provide power to the output.
b[5]	Status_word_vout_ov	An output overvoltage fault has occurred.
b[4]	Status_word_iout_oc	An output overcurrent fault has occurred.
b[3]	Status_word_vin_uv	A $V_{IN}$ undervoltage fault has occurred.
b[2]	Status_word_temp	A temperature fault or warning has occurred. See STATUS_TEMPERATURE.
b[1]	Status_word_cml	A communication, memory or logic fault has occurred. See STATUS_CML.
b[0]	Status_word_high_byte	A fault/warning not listed in b[7:1] has occurred or Status_word_power_not_good = 1.

## PMBUS COMMAND DESCRIPTION

### STATUS\_VOUT

The STATUS\_VOUT command returns the summary of the output voltage faults or warnings which have occurred, as shown in the following table:

#### STATUS\_VOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_vout_ov_fault	Overvoltage fault.
b[6]	Status_vout_ov_warn	Overvoltage warning.
b[5]	Status_vout_uv_warn	Undervoltage warning
b[4]	Status_vout_uv_fault	Undervoltage fault.
b[3]	Status_vout_max_warn	VOUT_MAX warning. An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
b[2]	Status_vout_ton_max_fault	TON_MAX_FAULT sequencing fault.
b[1]	Status_vout_toff_max_warn	Not supported. Always returns 0.
b[0]	Status_vout_tracking_error	Not supported. Always returns 0.

### STATUS\_IOUT

The STATUS\_IOUT command returns the summary of the output current faults or warnings which have occurred, as shown in the following table:

#### STATUS\_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_iout_oc_fault	Overcurrent fault.
b[6]	Status_iout_oc_uv_fault	Not Supported. Always returns 0.
b[5]	Status_iout_oc_warn	Overcurrent warning
b[4]	Status_iout_uc_fault	Undercurrent fault.
b[3]	Status_iout_curr_share_fault	Not Supported. Always returns 0.
b[2]	Status_pout_power_limiting	Not Supported. Always returns 0.
b[1]	Status_pout_overpower_fault	Not Supported. Always returns 0.
b[0]	Status_pout_overpower_warn	Not Supported. Always returns 0.

### STATUS\_INPUT

The STATUS\_INPUT command returns the summary of the  $V_{IN}$  faults or warnings which have occurred, as shown in the following table:

#### STATUS\_INPUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_input_ov_fault	$V_{IN}$ overvoltage fault
b[6]	Status_input_ov_warn	$V_{IN}$ overvoltage warning
b[5]	Status_input_uv_warn	$V_{IN}$ undervoltage warning
b[4]	Status_input_uv_fault	$V_{IN}$ undervoltage fault
b[3]	Status_input_off	Unit is off for insufficient input voltage.
b[2]	IIN overcurrent fault	Not supported. Always returns 0.
b[1]	IIN overcurrent warn	Not supported. Always returns 0.
b[0]	PIN overpower warn	Not supported. Always returns 0.

## PMBUS COMMAND DESCRIPTION

### STATUS\_TEMPERATURE

The STATUS\_TEMPERATURE command returns the summary of the temperature faults or warnings which have occurred, as shown in the following table. Note that this information is paged and refers to the temperature of the associated external diode.

#### STATUS\_TEMPERATURE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_temperature_ot_fault	Overtemperature fault.
b[6]	Status_temperature_ot_warn	Overtemperature warning.
b[5]	Status_temperature_ut_warn	Undertemperature warning.
b[4]	Status_temperature_ut_fault	Undertemperature fault.
b[3]	Reserved	Reserved. Always returns 0.
b[2]	Reserved	Reserved. Always returns 0.
b[1]	Reserved	Reserved. Always returns 0.
b[0]	Reserved	Reserved. Always returns 0.

### STATUS\_CML

The STATUS\_CML command returns the summary of the communication, memory and logic faults or warnings which have occurred, as shown in the following table:

#### STATUS\_CML Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_cml_cmd_fault	1 = An illegal or unsupported command fault has occurred. 0 = No fault has occurred.
b[6]	Status_cml_data_fault	1 = Illegal or unsupported data received. 0 = No fault has occurred.
b[5]	Status_cml_pec_fault	1 = A packet error check fault has occurred. Note: PEC checking is always active in the LTC2975. Any extra byte received before a STOP will set Status_cml_pec_fault unless the extra byte is a matching PEC byte. 0 = No fault has occurred.
b[4]	Status_cml_memory_fault	1 = A fault has occurred in the EEPROM. 0 = No fault has occurred.
b[3]	Status_cml_processor_fault	Not supported, always returns 0.
b[2]	Reserved	Reserved, always returns 0.
b[1]	Status_cml_pmbus_fault	1 = A communication fault other than ones listed in this table has occurred. This is a catch all category for illegally formed I <sup>2</sup> C/SMBus commands (Example: An address byte with read =1 received immediately after a START). 0 = No fault has occurred.
b[0]	Status_cml_unknown_fault	Not supported, always returns 0.

### STATUS\_MFR\_SPECIFIC

The STATUS\_MFR\_SPECIFIC command returns manufacturer specific status flags. Bits marked CHANNEL = All are not paged. Bits marked STICKY = Yes stay set until a CLEAR\_FAULTS is issued or the channel is commanded on by the user. Bits marked ALERT = Yes pull ALERTB low when the bit is set. Bits marked OFF = Yes indicate that the event can be configured elsewhere to turn the channel off.

## PMBUS COMMAND DESCRIPTION

### STATUS\_MFR\_SPECIFIC Data Contents

BIT(S)	SYMBOL	OPERATION	CHANNEL	STICKY	ALERT	OFF
b[7]	Status_mfr_discharge	1 = A $V_{OUT}$ discharge fault occurred while attempting to enter the ON state. 0 = No $V_{OUT}$ discharge fault has occurred.	Current Page	Yes	Yes	Yes
b[6]	Status_mfr_fault1_in	This channel attempted to turn on while the FAULTB1 pin was asserted low, or this channel has shut down at least once in response to a FAULTB1 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command.	Current Page	Yes	Yes	Yes
b[5]	Status_mfr_fault0_in	This channel attempted to turn on while the FAULTB0 pin was asserted low, or this channel has shut down at least once in response to a FAULTB0 pin asserting low since the last CONTROL pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command.	Current Page	Yes	Yes	Yes
b[4]	Status_mfr_servo_target_reached	Servo target has been reached.	Current Page	No	No	No
b[3]	Status_mfr_dac_connected	DAC is connected and driving $V_{DAC}$ pin.	Current Page	No	No	No
b[2]	Status_mfr_dac_saturated	A previous servo operation terminated with maximum or minimum DAC value.	Current Page	Yes	No	No
b[1]	Status_mfr_auxfaultb_faulted_off	AUXFAULTB has been de-asserted due to a $V_{OUT}$ or $I_{OUT}$ fault.	All	No	No	No
b[0]	Status_mfr_watchdog_fault	1 = A watchdog fault has occurred. 0 = No watchdog fault has occurred.	All	Yes	Yes	No

### MFR\_PADS

The MFR\_PADS command provides read-only access of digital pads (pins). The input values are before any deglitching logic.

### MFR\_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_pads_pwrpd_drive	0 = PWRGD pad is being driven low by this chip. 1 = PWRGD pad is not being driven low by this chip.
b[14]	Mfr_pads_alertb_drive	0 = ALERTB pad is being driven low by this chip. 1 = ALERTB pad is not being driven low by this chip.
b[13:12]	Mfr_pads_faultb_drive[1:0]	bit[1] used for FAULTB0 pad, bit[0] used for FAULTB1 pad as follows: 0 = FAULTB pad is being driven low by this chip. 1 = FAULTB pad is not being driven low by this chip.
b[11:10]	Reserved[1:0]	Always returns 00b.
b[9:8]	Mfr_pads_asel1[1:0]	11: Logic high detected on ASEL1 input pad. 10: ASEL1 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL1 input pad.
b[7:6]	Mfr_pads_asel0[1:0]	11: Logic high detected on ASEL0 input pad. 10: ASEL0 input pad is floating. 01: Reserved. 00: Logic low detected on ASEL0 input pad.

## PMBUS COMMAND DESCRIPTION

### MFR\_PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[5]	Mfr_pads_control1	1: Logic high detected on CONTROL1 pad. 0: Logic low detected on CONTROL1 pad.
b[4]	Mfr_pads_control0	1: Logic high detected on CONTROL0 pad. 0: Logic low detected on CONTROL0 pad.
b[3:2]	Mfr_pads_faultb[1:0]	bit[1] used for FAULTB0 pad, bit[0] used for FAULTB1 pad as follows: 1: Logic high detected on FAULTB pad. 0: Logic low detected on FAULTB pad.
b[1]	Mfr_pads_control2	1: Logic high detected on CONTROL2 pad. 0: Logic low detected on CONTROL2 pad.
b[0]	Mfr_pads_control3	1: Logic high detected on CONTROL3 pad. 0: Logic low detected on CONTROL3 pad.

### MFR\_COMMON

This command returns status information for the alert, device busy, share-clock pin (SHARE\_CLK) and the write-protect pin (WP).

This is the only command that may still be read when the LTC2975 is busy processing an EEPROM or other command. It may be polled by the host to determine when the LTC2975 is available to process a PMBus command. A busy device will always acknowledge its address but will NACK the command byte and set Status\_byte\_busy and Status\_word\_busy when it receives a command that it cannot immediately process. ALERTB will be asserted low in this case.

### MFR\_COMMON Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_common_alertb	Returns alert status. 1: ALERTB is de-asserted high. 0: ALERTB is asserted low.
b[6]	Mfr_common_busyb	Returns device busy status. 1: The device is available to process PMBus commands. 0: The device is busy and will NACK PMBus commands.
b[5:2]	Reserved	Read only, always returns 1s.
b[1]	Mfr_common_share_clk	Returns the status of the share-clock pin. 1: Share-clock pin is being held low. 0: Share-clock pin is active.
b[0]	Mfr_common_write_protect	Returns the status of the write-protect pin. 1: Write-protect pin is high. 0: Write-protect pin is low.

## PMBUS COMMAND DESCRIPTION

### TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	71
READ_IIN	0x89	DC/DC converter input current.	R Word	N	L11	A		NA	71
READ_PIN	0x97	DC/DC converter input power.	R Word	N	L11	W		NA	71
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	71
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	72
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	72
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	72
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	73
MFR_READ_IOUT	0xBB	Alternate data format for READ_IOUT. One LSB = 2.5mA.	R Word	Y	CF	2.5mA		NA	73
MFR_IIN_PEAK	0xC4	Maximum measured value of READ_IIN	R Word	N	L11	A		NA	72
MFR_IIN_MIN	0xC5	Minimum measured value of READ_IIN.	R Word	N	L11	A		NA	72
MFR_PIN_PEAK	0xC6	Maximum measured value of READ_PIN.	R Word	N	L11	W		NA	72
MFR_PIN_MIN	0xC7	Minimum measured value of READ_PIN.	R Word	N	L11	W		NA	72
MFR_IOUT_SENSE_VOLTAGE	0xFA	Absolute value of the voltage between I <sub>SENSEp<sub>n</sub></sub> and I <sub>SENSEm<sub>n</sub></sub> . One LSB = 3.05µV.	R Word	Y	CF	3.05µV		NA	74
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN.	R Word	N	L11	V		NA	74
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT.	R Word	Y	L16	V		NA	74
MFR_IOUT_PEAK	0xD7	Maximum measured value of READ_IOUT.	R Word	Y	L11	A		NA	74
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	74
MFR_VIN_MIN	0xFC	Minimum measured value of READ_VIN.	R Word	N	L11	V		NA	74
MFR_VOUT_MIN	0xFB	Minimum measured value of READ_VOUT.	R Word	Y	L16	V		NA	74
MFR_IOUT_MIN	0xD8	Minimum measured value of READ_IOUT.	R Word	Y	L11	A		NA	75
MFR_TEMPERATURE_1_MIN	0xFD	Minimum measured value of READ_TEMPERATURE_1.	R Word	Y	L11	°C		NA	75

#### READ\_VIN

This command returns the most recent ADC measured value of the input voltage at the V<sub>IN\_SNS</sub> pin.

#### READ\_IIN

This command returns the most recent ADC measured value of the input current derived from the voltage difference between the IIN\_SNSP and IIN\_SNSM pins. The READ\_IIN value reported is automatically corrected to account for the range selected by Mfr\_ein\_config\_iin\_range[1:0].

#### READ\_PIN

This command returns the most recent ADC measured value of the input power in watts. This is the product of READ\_IIN and READ\_VIN.

#### READ\_VOUT

This command returns the most recent ADC measured value of the channel's output voltage.

## **PMBUS COMMAND DESCRIPTION**

### ***READ\_IOUT***

This command returns the most recent ADC measured value of the channel's output current.

### ***MFR\_IIN\_PEAK***

This command returns the maximum ADC measured value of the input current. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_IIN\_MIN***

This command returns the minimum ADC measured value of the input current. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_PIN\_PEAK***

This command returns the maximum ADC measured value of the input power. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_PIN\_MIN***

This command returns the minimum ADC measured value of the input power. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***READ\_TEMPERATURE\_1***

This command returns the most recent measured value of the external diode temperature in °C. This value is used for all temperature related operations and calculations. This command is paged. READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if the associated T<sub>SENSE</sub> network fails to detect a valid temperature.

The T<sub>SENSE</sub> network will fail to detect a valid temperature under the following conditions:

- The T<sub>SENSE</sub> pin is shorted to a constant voltage.

- The sense diode has an ideality factor greater than N<sub>TS</sub> max.

### ***READ\_TEMPERATURE\_2***

This command returns the most recent ADC measured value of junction temperature in °C as determined by the LTC2975's internal temperature sensor. This register is for information purposes and does not generate any faults, warnings, or affect any other registers or internal calculations unless it is used as READ\_TEMPERATURE\_1. This command is not paged.

READ\_TEMPERATURE\_2 is substituted for READ\_TEMPERATURE\_1 if a channel's T<sub>SENSE</sub> network fails to detect a valid temperature.



## PMBUS COMMAND DESCRIPTION

### READ\_POUT

This command returns the most recent ADC measured value of the channel's output power in watts.

### MFR\_READ\_IOUT

This command returns the most recent ADC measured value of the channel's output current, using a custom format that provides better numeric representation granularity than the READ\_IOUT command for currents whose absolute value is between 2A and 82A.

#### MFR\_READ\_IOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_read_iout[15:0]	Channel output current expressed in custom format for improved resolution at high currents. Value = $Y \cdot 2.5$ where $Y = b[15:0]$ is a signed two's-complement number. Example: MFR_READ_IOUT = 5mA For b[15:0] = 0x0002 Value = $2 \cdot 2.5 = 5\text{mA}$

The granularity of the returned value is always 2.5mA, and the return value is limited to  $\pm 81.92\text{A}$ . The READ\_IOUT command provides the best resolution for currents less than 2A and must be used for currents larger than 82A. Note that the accuracy of the returned value is always limited by the ADC Characteristics listed in the Electrical Characteristics section.

**Table 5. Comparison of Granularity Due to Numeric Format**

CURRENT RANGE	READ_IOUT GRANULARITY	MFR_READ_IOUT GRANULARITY
$31.25\text{mA} \leq I_{\text{OUT}} < 62.5\text{mA}$	61 $\mu\text{A}$	2.5mA
$62.5\text{mA} \leq I_{\text{OUT}} < 125\text{mA}$	122 $\mu\text{A}$	2.5mA
$125\text{mA} \leq I_{\text{OUT}} < 250\text{mA}$	244 $\mu\text{A}$	2.5mA
$250\text{mA} \leq I_{\text{OUT}} < 500\text{mA}$	488 $\mu\text{A}$	2.5mA
$0.5\text{A} \leq I_{\text{OUT}} < 1\text{A}$	977 $\mu\text{A}$	2.5mA
$1\text{A} \leq I_{\text{OUT}} < 2\text{A}$	1.95mA	2.5mA
$2\text{A} \leq I_{\text{OUT}} < 4\text{A}$	3.9mA	2.5mA
$4\text{A} \leq I_{\text{OUT}} < 8\text{A}$	7.8mA	2.5mA
$8\text{A} \leq I_{\text{OUT}} < 16\text{A}$	15.6mA	2.5mA
$16\text{A} \leq I_{\text{OUT}} < 32\text{A}$	31.3mA	2.5mA
$32\text{A} \leq I_{\text{OUT}} < 64\text{A}$	62.5mA	2.5mA
$64\text{A} \leq I_{\text{OUT}} < 82\text{A}$	125mA	2.5mA
$82\text{A} \leq I_{\text{OUT}} < 128\text{A}$	125mA	Saturated
$128\text{A} \leq I_{\text{OUT}} < 256\text{A}$	250mA	Saturated

## PMBUS COMMAND DESCRIPTION

### ***MFR\_IOUT\_SENSE\_VOLTAGE***

This command returns the absolute value of the voltage measured between  $I_{SENSEp_n}$  and  $I_{SENSEM_n}$  during the last READ\_IOUT ADC conversion without any temperature correction.

#### **MFR\_IOUT\_SENSE\_VOLTAGE Data Contents**

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_iout_sense_voltage	Absolute value of raw voltage conversion measured between $I_{SENSEp_n}$ and $I_{SENSEM_n}$ . Value = $Y \cdot 0.025 \cdot 2^{-13}$ where $Y = b[15:0]$ is an unsigned integer. Example: MFR_IOUT_SENSE_VOLTAGE = 1.544mV For b[15:0] = 0x1FA=506 Value = $506 \cdot 0.025 \cdot 2^{-13} = 1.544\text{mV}$

### ***MFR\_VIN\_PEAK***

This command returns the maximum ADC measured value of the input voltage. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_VOUT\_PEAK***

This command returns the maximum ADC measured value of the channel's output voltage. This register is reset to 0xF800 (0.0) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### ***MFR\_IOUT\_PEAK***

This command returns the maximum ADC measured value of the channel's output current. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### ***MFR\_TEMPERATURE\_1\_PEAK***

This command returns the maximum measured value of the external diode temperature in °C. This register is reset to 0x7C00 ( $-2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### ***MFR\_VIN\_MIN***

This command returns the minimum ADC measured value of the input voltage. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to any page is executed, or a channel goes through an off-to-on transition.

### ***MFR\_VOUT\_MIN***

This command returns the minimum ADC measured value of the channel's output voltage. This register is reset to 0xFFFF (7.9999) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

## PMBUS COMMAND DESCRIPTION

### MFR\_IOUT\_MIN

This command returns the minimum ADC measured value of the channel's output current. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

### MFR\_TEMPERATURE\_1\_MIN

This command returns the minimum measured value of the external diode temperature in °C. This register is reset to 0x7BFF (approximately  $2^{25}$ ) when the LTC2975 emerges from power-on reset, when a CLEAR\_FAULTS command to the page is executed, or the channel goes through an off-to-on transition.

## FAULT LOGGING

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	75
MFR_FAULT_LOG_RESTORE	0xEB	Command a transfer of the fault log previously stored in EEPROM back to RAM.	Send Byte	N				NA	76
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	76
MFR_FAULT_LOG_STATUS	0xED	Fault logging status.	R Byte	N	Reg		Y	NA	76
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	76

### Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 22. The fault log provides black box capability for the LTC2975. During normal operation the contents of the status registers, the output voltage/current/temperature readings, the input voltage readings, as well as peak and min values of these quantities, are stored in a continuously updated buffer in RAM. You can think of the operation as being similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for non volatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time.

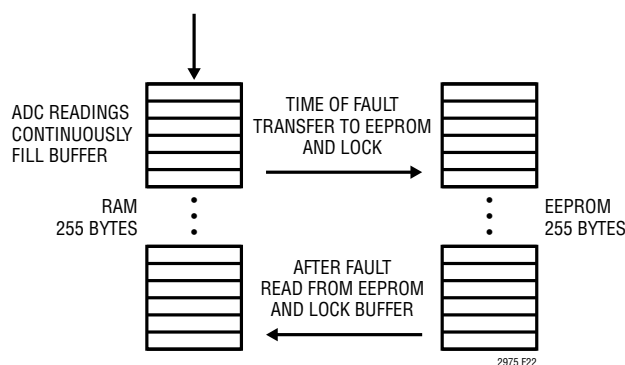


Figure 22. Fault Logging

### MFR\_FAULT\_LOG\_STORE

This command allows the user to transfer data from the RAM buffer to EEPROM.

## PMBUS COMMAND DESCRIPTION

### ***MFR\_FAULT\_LOG\_RESTORE***

This command allows the user to transfer a copy of the fault-log data from the EEPROM to the RAM buffer. After a restore the RAM buffer is locked until a successful Mfr\_fault\_log read.

### ***MFR\_FAULT\_LOG\_CLEAR***

This command initializes the EEPROM block reserved for fault logging. Any previous fault log stored in EEPROM will be erased by this operation and logging of the fault log RAM to EEPROM will be enabled. Make sure that Mfr\_fault\_log\_status\_ram = 0 before issuing the MFR\_FAULT\_LOG\_CLEAR command.

### ***MFR\_FAULT\_LOG\_STATUS***

This register is used to manage fault log events. The Mfr\_fault\_log\_status\_eeprom bit is set after a MFR\_FAULT\_LOG\_STORE command or a faulted-off event triggers a transfer of the fault log from RAM to EEPROM. This bit is cleared by a MFR\_FAULT\_LOG\_CLEAR command.

Mfr\_fault\_log\_status\_ram is set after a MFR\_FAULT\_LOG\_RESTORE to indicate that the data in the RAM has been restored from EEPROM and not yet read using a MFR\_FAULT\_LOG command. This bit is cleared only by a successful execution of an MFR\_FAULT\_LOG command.

#### **MFR\_FAULT\_LOG\_STATUS Data Contents**

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Read only, always returns 0s.
b[1]	Mfr_fault_log_status_ram	Fault log RAM status: 0: The fault log RAM allows updates. 1: The fault log RAM is locked until the next Mfr_fault_log read.
b[0]	Mfr_fault_log_status_eeprom	Fault log EEPROM status: 0: The transfer of the fault log RAM to the EEPROM is enabled. 1: The transfer of the fault log RAM to the EEPROM is inhibited.

### ***MFR\_FAULT\_LOG***

Read only. This 2040-bit (255 byte) data block contains a copy of the RAM buffer fault log. The RAM buffer is continuously updated after each ADC conversion as long as Mfr\_fault\_log\_status\_eeprom is clear.

With Mfr\_config\_fault\_log\_enable = 1 and Mfr\_fault\_log\_status\_eeprom = 0, the RAM buffer is transferred to EEPROM whenever an LTC2975 fault causes a channel to latch off or a MFR\_FAULT\_LOG\_STORE command is received. This transfer is delayed until the ADC has updated its READ values for all channels when Mfr\_config\_all\_fast\_fault\_log is clear, otherwise it happens within 24ms. This optional delay can be used to ensure that the slower ADC monitored values are all updated for the case where a fast supervisor detected fault initiates the transfer to EEPROM.

Mfr\_fault\_log\_status\_eeprom is set high after the RAM buffer is transferred to EEPROM and not cleared until a Mfr\_fault\_log\_clear is received, even if the LTC2975 is reset or powered down. Fault log EEPROM transfers are not initiated as a result of Status\_mfr\_discharge events.

During a Mfr\_fault\_log read, data is returned one byte at a time as defined in Table 6. The fault log data is partitioned into two sections. The first section is referred to as the preamble and contains the Position\_last pointer, time information and peak and min values. The second section contains a chronological record of telemetry and requires Position\_last for proper interpretation. The fault log stores approximately 300ms seconds of telemetry. To prevent timeouts during block reads, it is recommended that Mfr\_config\_all\_longer\_pmbus\_timeout be set to 1.

## PMBUS COMMAND DESCRIPTION

**Table 6. Data Block Contents**

DATA	BYTE*	DESCRIPTION
Position_last[7:0]	0	Position of fault log pointer when fault occurred.
SharedTime[7:0]	1	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
SharedTime[15:8]	2	
SharedTime[23:16]	3	
SharedTime[31:24]	4	
SharedTime[39:32]	5	
SharedTime[40]	6	
Mfr_vout_peak0[7:0]	7	
Mfr_vout_peak0[15:8]	8	
Mfr_vout_min0[7:0]	9	
Mfr_vout_min0[15:8]	10	
Mfr_temperature_peak0[7:0]	11	
Mfr_temperature_peak0[15:8]	12	
Mfr_temperature_min0[7:0]	13	
Mfr_temperature_min0[15:8]	14	
Mfr_iout_peak0[7:0]	15	
Mfr_iout_peak0[15:8]	16	
Mfr_iout_min0[7:0]	17	
Mfr_iout_min0[15:8]	18	
Mfr_vin_peak[7:0]	19	
Mfr_vin_peak[15:8]	20	
Mfr_vin_min[7:0]	21	
Mfr_vin_min[15:8]	22	
Mfr_iin_peak[7:0]	23	
Mfr_iin_peak[15:8]	24	
Mfr_iin_min[7:0]	25	
Mfr_iin_min[15:8]	26	
Mfr_pin_peak[7:0]	27	
Mfr_pin_peak[15:8]	28	
Mfr_pin_min[7:0]	29	
Mfr_pin_min[15:8]	30	
Mfr_vout_peak1[7:0]	31	
Mfr_vout_peak1[15:8]	32	
Mfr_vout_min1[7:0]	33	
Mfr_vout_min1[15:8]	34	
Mfr_temperature_peak1[7:0]	35	
Mfr_temperature_peak1[15:8]	36	
Mfr_temperature_min1[7:0]	37	
Mfr_temperature_min1[15:8]	38	

**Table 6. Data Block Contents**

DATA	BYTE*	DESCRIPTION
Mfr_iout_peak1[7:0]	39	
Mfr_iout_peak1[15:8]	40	
Mfr_iout_min1[7:0]	41	
Mfr_iout_min1[15:8]	42	
Mfr_vout_peak2[7:0]	43	
Mfr_vout_peak2[15:8]	44	
Mfr_vout_min2[7:0]	45	
Mfr_vout_min2[15:8]	46	
Mfr_temperature_peak2[7:0]	47	
Mfr_temperature_peak2[15:8]	48	
Mfr_temperature_min2[7:0]	49	
Mfr_temperature_min2[15:8]	50	
Mfr_iout_peak2[7:0]	51	
Mfr_iout_peak2[15:8]	52	
Mfr_iout_min2[7:0]	53	
Mfr_iout_min2[15:8]	54	
Mfr_vout_peak3[7:0]	55	
Mfr_vout_peak3[15:8]	56	
Mfr_vout_min3[7:0]	57	
Mfr_vout_min3[15:8]	58	
Mfr_temperature_peak3[7:0]	59	
Mfr_temperature_peak3[15:8]	60	
Mfr_temperature_min3[7:0]	61	
Mfr_temperature_min3[15:8]	62	
Mfr_iout_peak3[7:0]	63	
Mfr_iout_peak3[15:8]	64	
Mfr_iout_min3[7:0]	65	
Mfr_iout_min3[15:8]	66	
Status_vout0[7:0]	67	
Status_iout0[7:0]	68	
Status_mfr_specific0[7:0]	69	
Status_vout1[7:0]	70	
Status_iout1[7:0]	71	
Status_mfr_specific1[7:0]	72	
Status_vout2[7:0]	73	
Status_iout2[7:0]	74	
Status_mfr_specific2[7:0]	75	
Status_vout3[7:0]	76	
Status_iout3[7:0]	77	
Status_mfr_specific3[7:0]	78	
		79 bytes for preamble

## PMBUS COMMAND DESCRIPTION

**Table 6. Data Block Contents**

DATA	BYTE*	DESCRIPTION
Fault_log [Position_last]	79	
Fault_log [Position_last-1]	80	
...		
Fault_log [Position_last-170]	237	
Reserved	238-254	
		Number of loops: $(238 - 79)/58 = 2.7$

\*Note that PMBus data byte numbers start at 1 rather than 0. See Figure 13 Block Read.

The data returned between bytes 79 and 237 of the previous table is interpreted using Position\_last and the following table. The key to identifying the data located in byte 79 is to locate the DATA corresponding to POSITION = Position\_last in the next table. Subsequent bytes are identified by decrementing the value of POSITION. For example: If Position\_last = 8 then the first data returned in a block read is Status\_temperature of page 0 followed by Read\_temperature\_1[15:8] of page 0 followed by Read\_temperature\_1[7:0] of page 0 and so on. See Table 7.

**Table 7. Interpreting Cyclical Loop Data**

POSITION	DATA
0	Read_temperature_2[7:0]
1	Read_temperature_2[15:8]
2	Read_vout0[7:0]
3	Read_vout0[15:8]
4	Status_vout0[7:0]
5	Status_mfr_specific0[7:0]
6	Read_temperature_1_0[7:0]
7	Read_temperature_1_0[15:8]
8	Status_temperature0[7:0]
9	Status_iout0[7:0]
10	Read_iout0[7:0]
11	Read_iout0[15:8]
12	Read_pout0[7:0]
13	Read_pout0[15:8]
14	Read_vin[7:0]
15	Read_vin[15:8]
16	Status_input[7:0]
17	0x0

**Table 7. Interpreting Cyclical Loop Data**

POSITION	DATA
18	Read_iin[7:0]
19	Read_iin[15:8]
20	Read_pin[7:0]
21	Read_pin[15:8]
22	Read_vout1[7:0]
23	Read_vout1[15:8]
24	Status_vout1[7:0]
25	Status_mfr_specific1[7:0]
26	Read_temperature_1_1[7:0]
27	Read_temperature_1_1[15:8]
28	Status_temperature1[7:0]
29	Status_iout1[7:0]
30	Read_iout1[7:0]
31	Read_iout1[15:8]
32	Read_pout1[7:0]
33	Read_pout1[15:8]
34	Read_vout2[7:0]
35	Read_vout2[15:8]
36	Status_vout2[7:0]
37	Status_mfr_specific2[7:0]
38	Read_temperature_1_2[7:0]
39	Read_temperature_1_2[15:8]
40	Status_temperature2[7:0]
41	Status_iout2[7:0]
42	Read_iout2[7:0]
43	Read_iout2[15:8]
44	Read_pout2[7:0]
45	Read_pout2[15:8]
46	Read_vout3[7:0]
47	Read_vout3[15:8]
48	Status_vout3[7:0]
49	Status_mfr_specific3[7:0]
50	Read_temperature_1_3[7:0]
51	Read_temperature_1_3[15:8]
52	Status_temperature3[7:0]
53	Status_iout3[7:0]
54	Read_iout3[7:0]
55	Read_iout3[15:8]
56	Read_pout3[7:0]
57	Read_pout3[15:8]
	Total Bytes = 58

## PMBUS COMMAND DESCRIPTION

### MFR\_FAULT\_LOG Read Example

The following table fully decodes a sample fault log read with Position\_last = 13 to help clarify the cyclical nature of the operation.

#### Data Block Contents

PREAMBLE INFORMATION				
BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
0	00		Position_last[7:0] = 13	Position of fault-log pointer when fault occurred.
1	01		SharedTime[7:0]	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments.
2	02		SharedTime[15:8]	
3	03		SharedTime[23:16]	
4	04		SharedTime[31:24]	
5	05		SharedTime[39:32]	
6	06		SharedTime[40]	
7	07		Mfr_vout_peak0[7:0]	
8	08		Mfr_vout_peak0[15:8]	
9	09		Mfr_vout_min0[7:0]	
10	0A		Mfr_vout_min0[15:8]	
11	0B		Mfr_temperature_peak0[7:0]	
12	0C		Mfr_temperature_peak0[15:8]	
13	0D		Mfr_temperature_min0[7:0]	
14	0E		Mfr_temperature_min0[15:8]	
15	0F		Mfr_iout_peak0[7:0]	
16	10		Mfr_iout_peak0[15:8]	
17	11		Mfr_iout_min0[7:0]	
18	12		Mfr_iout_min0[15:8]	
19	13		Mfr_vin_peak_[7:0]	
20	14		Mfr_vin_peak_[15:8]	
21	15		Mfr_vin_min_[7:0]	
22	16		Mfr_vin_min_[15:8]	
23	17		Mfr_iin_peak[7:0]	
24	18		Mfr_iin_peak[15:8]	
25	19		Mfr_iin_min[7:0]	
26	1A		Mfr_iin_min[15:8]	
27	1B		Mfr_pin_peak[7:0]	

#### PREAMBLE INFORMATION (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX		DATA	DESCRIPTION
28	1C		Mfr_pin_peak[15:8]	
29	1D		Mfr_pin_min[7:0]	
30	1E		Mfr_pin_min[15:8]	
31	1F		Mfr_vout_peak1[7:0]	
32	20		Mfr_vout_peak1[15:8]	
33	21		Mfr_vout_min1[7:0]	
34	22		Mfr_vout_min1[15:8]	
35	23		Mfr_temperature_peak1[7:0]	
36	24		Mfr_temperature_peak1[15:8]	
37	25		Mfr_temperature_min1[7:0]	
38	26		Mfr_temperature_min1[15:8]	
39	27		Mfr_iout_peak1[7:0]	
40	28		Mfr_iout_peak1[15:8]	
41	29		Mfr_iout_min1[7:0]	
42	2A		Mfr_iout_min1[15:8]	
43	2B		Mfr_vout_peak2[7:0]	
44	2C		Mfr_vout_peak2[15:8]	
45	2D		Mfr_vout_min2[7:0]	
46	2E		Mfr_vout_min2[15:8]	
47	2F		Mfr_temperature_peak2[7:0]	
48	30		Mfr_temperature_peak2[15:8]	
49	31		Mfr_temperature_min2[7:0]	
50	32		Mfr_temperature_min2[15:8]	
51	33		Mfr_iout_peak2[7:0]	
52	34		Mfr_iout_peak2[15:8]	
53	35		Mfr_iout_min2[7:0]	
54	36		Mfr_iout_min2[15:8]	
55	37		Mfr_vout_peak3[7:0]	
56	38		Mfr_vout_peak3[15:8]	
57	39		Mfr_vout_min3[7:0]	
58	3A		Mfr_vout_min3[15:8]	
59	3B		Mfr_temperature_peak3[7:0]	

## PMBUS COMMAND DESCRIPTION

### PREAMBLE INFORMATION (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	DATA	DESCRIPTION
60	3C	Mfr_temperature_peak3[15:8]	
61	3D	Mfr_temperature_min3[7:0]	
62	3E	Mfr_temperature_min3[15:8]	
63	3F	Mfr_iout_peak3[7:0]	
64	40	Mfr_iout_peak3[15:8]	
65	41	Mfr_iout_min3[7:0]	
66	42	Mfr_iout_min3[15:8]	
67	43	Status_vout0[7:0]	
68	44	Status_iout0[7:0]	
69	45	Status_temperature0[7:0]	
70	46	Status_vout1[7:0]	
71	47	Status_iout1[7:0]	
72	48	Status_temperature1[7:0]	
73	49	Status_vout2[7:0]	
74	4A	Status_iout2[7:0]	
75	4B	Status_temperature2[7:0]	
76	4C	Status_vout3[7:0]	
77	4D	Status_iout3[7:0]	
78	4E	Status_temperature3[7:0]	End of Preamble

### CYCLICAL MUX LOOP DATA PARTIAL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 0	58 BYTES PER LOOP
79	4F	13	Read_pout0[15:8]	Position_last
80	50	12	Read_pout0[7:0]	
81	51	11	Read_iout0[15:8]	
82	52	10	Read_iout0[7:0]	
83	53	9	Status_iout0[7:0]	

### CYCLICAL MUX LOOP DATA PARTIAL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 0	58 BYTES PER LOOP
84	54	8	Status_temperature0[7:0]	
85	55	7	Read_temperature_1_0[15:8]	
86	56	6	Read_temperature_1_0[7:0]	
87	57	5	Status_mfr_specific0[7:0]	
88	58	4	Status_vout0[7:0]	
89	59	3	Read_vout0[15:8]	
90	5A	2	Read_vout0[7:0]	
91	5B	1	Read_temperature_2[15:8]	
92	5C	0	Read_temperature_2[7:0]	

### CYCLICAL MUX LOOP DATA FULL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	58 BYTES PER LOOP
93	5D	57	Read_pout3[15:8]	
94	5E	56	Read_pout3[7:0]	
95	5F	55	Read_iout3[15:8]	
96	60	54	Read_iout3[7:0]	
97	61	53	Status_iout3[7:0]	
98	62	52	Status_temperature3[7:0]	
99	63	51	Read_temperature_1_3[15:8]	
100	64	50	Read_temperature_1_3[7:0]	
101	65	49	Status_mfr_specific3[7:0]	
102	66	48	Status_vout3[7:0]	
103	67	47	Read_vout3[15:8]	
104	78	46	Read_vout3[7:0]	
105	69	45	Read_pout2[15:8]	
106	6A	44	Read_pout2[7:0]	
107	6B	43	Read_iout2[15:8]	
108	6C	42	Read_iout2[7:0]	



## PMBUS COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	58 BYTES PER LOOP
109	6D	41	Status_iout2[7:0]	
110	6E	40	Status_temperature2[7:0]	
111	6F	39	Read_temperature_1_2[15:8]	
112	70	38	Read_temperature_1_2[7:0]	
113	71	37	Status_mfr_specific2[7:0]	
114	72	36	Status_vout2[7:0]	
115	73	35	Read_vout2[15:8]	
116	74	34	Read_vout2[7:0]	
117	75	33	Read_pout1[15:8]	
118	76	32	Read_pout1[7:0]	
119	77	31	Read_iout1[15:8]	
120	78	30	Read_iout1[7:0]	
121	79	29	Status_iout1[7:0]	
122	7A	28	Status_temperature2[7:0]	
123	7B	27	Read_temperature_1_1[15:8]	
124	7C	26	Read_temperature_1_1[7:0]	
125	7D	25	Status_mfr_specific1[7:0]	
126	7E	24	Status_vout1[7:0]	
127	7F	23	Read_vout1[15:8]	
128	80	22	Read_vout1[7:0]	
129	81	21	Read_pin[15:8]	
130	82	20	Read_pin[7:0]	
131	83	19	Read_in[15:8]	
132	84	18	Read_in[7:0]	
133	85	17	0x0	
134	86	16	Status_input[7:0]	
135	87	15	Read_vin[15:8]	
136	88	14	Read_vin[7:0]	
137	89	13	Read_pout0[15:8]	
138	8A	12	Read_pout0[7:0]	
139	8B	11	Read_iout0[15:8]	
140	8C	10	Read_iout0[7:0]	

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 1	58 BYTES PER LOOP
141	8D	9	Status_iout0[7:0]	
142	8E	8	Status_temperature0[7:0]	
143	8F	7	Read_temperature_1_0[15:8]	
144	90	6	Read_temperature_1_0[7:0]	
145	91	5	Status_mfr_specific0[7:0]	
146	92	4	Status_vout0[7:0]	
147	93	3	Read_vout0[15:8]	
148	94	2	Read_vout0[7:0]	
149	95	1	Read_temperature_2[15:8]	
150	96	0	Read_temperature_2[7:0]	

CYCLICAL MUX LOOP DATA FULL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	58 BYTES PER LOOP
151	97	57	Read_pout3[15:8]	
152	98	56	Read_pout3[7:0]	
153	99	55	Read_iout3[15:8]	
154	9A	54	Read_iout3[7:0]	
155	9B	53	Status_iout3[7:0]	
156	9C	52	Status_temperature3[7:0]	
157	9D	51	Read_temperature_1_3[15:8]	
158	9E	50	Read_temperature_1_3[7:0]	
159	9F	49	Status_mfr_specific3[7:0]	
160	A0	48	Status_vout3[7:0]	
161	A1	47	Read_vout3[15:8]	
162	A2	46	Read_vout3[7:0]	
163	A3	45	Read_pout2[15:8]	
164	A4	44	Read_pout2[7:0]	
165	A5	43	Read_iout2[15:8]	
166	A6	42	Read_iout2[7:0]	

## PMBUS COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	58 BYTES PER LOOP
167	A7	41	Status_iout2[7:0]	
168	A8	40	Status_temperature2[7:0]	
169	A9	39	Read_temperature_1_2[15:8]	
170	AA	38	Read_temperature_1_2[7:0]	
171	AB	37	Status_mfr_specific2[7:0]	
172	AC	36	Status_vout2[7:0]	
173	AD	35	Read_vout2[15:8]	
174	AE	34	Read_vout2[7:0]	
175	AF	33	Read_pout1[15:8]	
176	B0	32	Read_pout1[7:0]	
177	B1	31	Read_iout1[15:8]	
178	B2	30	Read_iout1[7:0]	
179	B3	29	Status_iout1[7:0]	
180	B4	28	Status_temperature2[7:0]	
181	B5	27	Read_temperature_1_1[15:8]	
182	B6	26	Read_temperature_1_1[7:0]	
183	B7	25	Status_mfr_specific1[7:0]	
184	B8	24	Status_vout1[7:0]	
185	B9	23	Read_vout1[15:8]	
186	BA	22	Read_vout1[7:0]	
187	BB	21	Read_pin[15:8]	
188	BC	20	Read_pin[7:0]	
189	BD	19	Read_in[15:8]	
190	BE	18	Read_in[7:0]	
191	BF	17	0x0	
192	C0	16	Status_input[7:0]	
193	C1	15	Read_vin[15:8]	
194	C2	14	Read_vin[7:0]	
195	C3	13	Read_pout0[15:8]	
196	C4	12	Read_pout0[7:0]	
197	C5	11	Read_iout0[15:8]	
198	C6	10	Read_iout0[7:0]	
199	C7	9	Status_iout0[7:0]	

CYCLICAL MUX LOOP DATA FULL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 2	58 BYTES PER LOOP
200	C8	8	Status_temperature0[7:0]	
201	C9	7	Read_temperature_1_0[15:8]	
202	CA	6	Read_temperature_1_0[7:0]	
203	CB	5	Status_mfr_specific0[7:0]	
204	CC	4	Status_vout0[7:0]	
205	CD	3	Read_vout0[15:8]	
206	CE	2	Read_vout0[7:0]	
207	CF	1	Read_temperature_2[15:8]	
208	D0	0	Read_temperature_2[7:0]	

CYCLICAL MUX LOOP DATA PARTIAL LOOP

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	58 BYTES PER LOOP
209	D1	57	Read_pout3[15:8]	
210	D2	56	Read_pout3[7:0]	
211	D3	55	Read_iout3[15:8]	
212	D4	54	Read_iout3[7:0]	
213	D5	53	Status_iout3[7:0]	
214	D6	52	Status_temperature_3[7:0]	
215	D7	51	Read_temperature_1_3[15:8]	
216	D8	50	Read_temperature_1_3[7:0]	
217	D9	49	Status_mfr_specific3[7:0]	
218	DA	48	Status_vout3[7:0]	
219	DB	47	Read_vout3[15:8]	
220	DC	46	Read_vout3[7:0]	
221	DD	45	Read_pout2[15:8]	
222	DE	44	Read_pout2[7:0]	
223	DF	43	Read_iout2[15:8]	
224	E0	42	Read_iout2[7:0]	
225	E1	41	Status_iout2[7:0]	

## PMBUS COMMAND DESCRIPTION

CYCLICAL MUX LOOP DATA PARTIAL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	58 BYTES PER LOOP
226	E2	40	Status_temperature2[7:0]	
227	E3	39	Read_temperature_1_2[15:8]	
228	E4	38	Read_temperature_1_2[7:0]	
229	E5	37	Status_mfr_specific2[7:0]	
230	E6	36	Status_vout2[7:0]	
231	E7	35	Read_vout2[15:8]	
232	E8	34	Read_vout2[7:0]	
233	E9	33	Read_pout1[15:8]	
234	EA	32	Read_pout1[7:0]	
235	EB	31	Read_iout1[15:8]	
236	EC	30	Read_iout1[7:0]	
237	ED	29	Status_iout1[7:0]	Last valid fault log byte
238	EE		0x00	Bytes EE - FE return 0x00
239	EF		0x00	

CYCLICAL MUX LOOP DATA PARTIAL LOOP (CONT.)

BYTE NUMBER DECIMAL	BYTE NUMBER HEX	LOOP BYTE NUMBER DECIMAL	MUX LOOP 3	58 BYTES PER LOOP
240	F0		0x00	
241	F1		0x00	
242	F2		0x00	
243	F3		0x00	
244	F4		0x00	
245	F5		0x00	
246	F6		0x00	
247	F7		0x00	
248	F8		0x00	
249	F9		0x00	
250	FA		0x00	
251	FB		0x00	
252	FC		0x00	
253	FD		0x00	
254	FE		0x00	This is PMBUS byte 255. It must be read to clear Mfr_fault_log_status_ram.

## IDENTIFICATION/INFORMATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	83
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	84
MFR_SPECIAL_ID	0xE7	Manufacturer code for identifying the LTC2975.	R Word	N	Reg		Y	0x0226	84
MFR_SPECIAL_LOT	0xC2	Customer dependent codes that identify the factory programmed user configuration stored in EEPROM. Contact factory for default value.	R Byte	Y	Reg		Y	NA	84
MFR_INFO	0xB6	Manufacturer specific information.	R Word	N	Reg			NA	84

## CAPABILITY

The CAPABILITY command provides a way for a host system to determine some key capabilities of the LTC2975.

### CAPABILITY Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Capability_pec	Hard coded to 1 indicating Packet Error Checking is supported. Reading the Mfr_config_all_pec_en bit will indicate whether PEC is currently required.
b[6:5]	Capability_scl_max	Hard coded to 01b indicating the maximum supported bus speed is 400kHz.
b[4]	Capability_smb_alert	Hard coded to 1 indicating this device does have an ALERTB pin and does support the SMBus Alert Response Protocol.
b[3:0]	Reserved	Always returns 0.

Rev. D

## PMBUS COMMAND DESCRIPTION

### PMBUS\_REVISION

#### PMBUS\_REVISION Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	PMBus_rev	Reports the PMBus standard revision compliance. This is hard-coded to 0x11 for revision 1.1.

### MFR\_SPECIAL\_ID

This register contains the manufacturer ID for the LTC2975. Always returns 0x0226.

### MFR\_SPECIAL\_LOT

These paged registers contain information that identifies the user configuration that was programmed at the factory. Contact the factory to request a custom factory programmed user configuration and special lot number.

### MFR\_INFO

The MFR\_INFO register contains manufacturer specific information and is updated after a power-on reset, a RESTORE\_USER\_ALL command, or an EEPROM bulk read operation.

#### MFR\_INFO Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:6]	Reserved	Reserved.
b[5]	Mfr_info_ecc_user	EEPROM ECC status. 0: Corrections made in the EEPROM user space. 1: No corrections made in the EEPROM user space.
b[4:0]	Reserved	Reserved.

## USER SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE	REF PAGE
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	84
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	84
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	84
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	84
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	84
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	84
MFR_LTC_RESERVED_2	0xBC	Manufacturer reserved.	R/W Word	Y	Reg			NA	84

### USER\_DATA\_00, USER\_DATA\_01, USER\_DATA\_02, USER\_DATA\_03, USER\_DATA\_04, MFR\_LTC\_RESERVED\_1 and MFR\_LTC\_RESERVED\_2

These registers are provided as user scratchpad and additional manufacturer reserved locations.

USER\_DATA\_03 and USER\_DATA\_04 are available for user scratchpad use. These 10 bytes (1 unpagged word plus 4 paged words) might be used for traceability or revision information such as serial number, board model number, assembly location, or assembly date.

## APPLICATIONS INFORMATION

### OVERVIEW

The LTC2975 is a 4-channel Power System Management IC that is capable of sequencing, margining, trimming, supervising output voltage for OV/UV conditions, supervising output current for OC/UC conditions, fault management, voltage/current/ temperature readback for four DC/DC converter channels, and readback of high side input current, input voltage, input power, input energy, and junction temperature. Multiple Analog Devices Power System Managers can coordinate operation using the SHARE\_CLK, FAULTB, and CONTROL pins. The LTC2975 utilizes a PMBus compliant interface and command set.

### POWERING THE LTC2975

The LTC2975 can be powered two ways. The first method requires that a voltage between 4.5V and 15V be applied to the  $V_{PWR}$  pin. See Figure 23. An internal linear regulator converts  $V_{PWR}$  down to 3.3V which drives all of the internal circuitry of the LTC2975.

Alternatively, power from an external 3.3V supply may be applied directly to the  $V_{DD33}$  pins 11 and 12 using a voltage between 3.13V and 3.47V. See Figure 24. Tie  $V_{PWR}$  to the

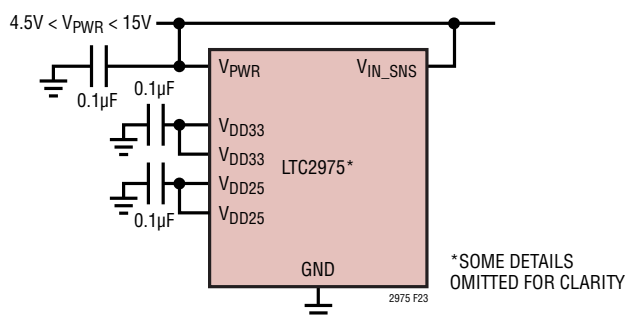


Figure 23. Powering LTC2975 Directly from an Intermediate Bus

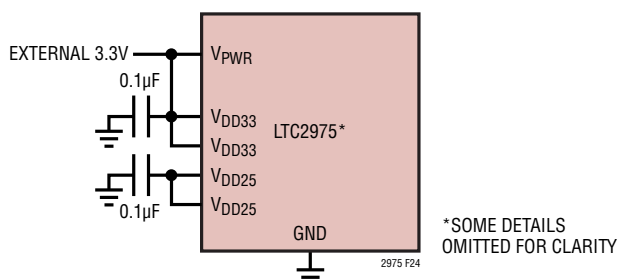


Figure 24. Powering LTC2975 from External 3.3V Supply

$V_{DD33}$  pins. All functionality is available when using this alternate power method. The higher voltages needed for the  $V_{OUT\_EN}$  pins and bias for the  $V_{SENSE}$  pins are charge pumped from  $V_{DD33}$ .

### SETTING COMMAND REGISTER VALUES

The command register settings described herein are intended as a reference and for the purpose of understanding the registers in a software development environment. In actual practice, the LTC2975 can be completely configured for stand-alone operation with the DC1613 USB to I<sup>2</sup>C/SMBus/PMBus controller and software GUI using intuitive menu driven objects.

### MEASURING INPUT CURRENT

The LTC2975 is capable of measuring the current of the input power source. The device also measures the input supply voltage, enabling it to calculate input power. The LTC2975 has an accurate internal time base allowing the chip to calculate input energy since energy is the product of power and time. The units for each of the measured parameters are amps, volts, watts, and millijoules.

Input current is measured by placing a sense resistor,  $R_{SENSE}$ , in series with the desired current load path as shown in Figure 25. If  $R_{SENSE}$  has low thermal drift characteristics, the MFR\_IIN\_CAL\_GAIN\_TC register value may be set to zero. Otherwise, choose a setting for the MFR\_IIN\_CAL\_GAIN\_TC value in units of ppm/°C to correct for  $R_{SENSE}$  thermal drift.

For best results, it is recommended to locate  $R_{SENSE}$  close to and isothermal with the LTC2975.

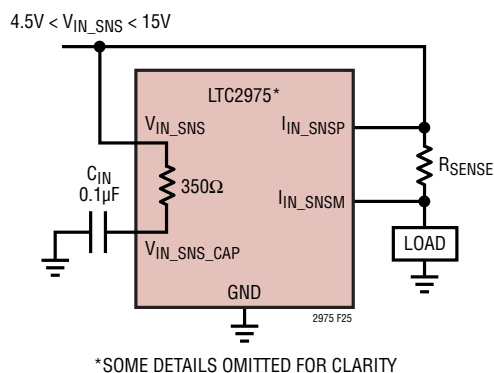


Figure 25. Measuring Input Current

## APPLICATIONS INFORMATION

The input current sense path includes an internal, anti-aliasing low pass filter with typical 32dB rejection at 62.5kHz. To improve high frequency current sense common mode rejection, add a 0.01μF capacitor,  $C_{IN}$ , to the  $V_{IN\_SNS\_CAP}$  pin.

The  $Mfr\_ein\_config\_iin\_range$  bits select one of three input current sense amplifier ranges: high, medium and low. The  $R_{SENSE}$  value should be chosen to satisfy the input range. The maximum allowable input ranges are as follows: ±100mV range for high range, ±50mV for medium range and ±20mV for low range. For best accuracy, use the lowest range setting encompassing the maximum input signal.

To help choose the  $R_{SENSE}$  value and  $Mfr\_ein\_config\_iin\_range$  setting for your application, use the Electrical Characteristics table for TUE\_IIN, along with Figures 26 and 27. Figures 26 and 27 serve as extrapolated guides while the Electrical Characteristics table shows tested TUE\_IIN conditions. After selecting  $R_{SENSE}$ , write its value in mΩ to the  $MFR\_IIN\_CAL\_GAIN$  register, and  $READ\_IIN$  will return the sensed current in amps. Figures 26 and 27 show absolute value of the expected worst case  $READ\_IIN$  Total Unadjusted Error, TUE\_IIN, in μV and in relative % of current sense input voltage reading,  $V_{IIN\_SNS}$ , as a function of  $V_{IIN\_SNS}$  ( $V_{IIN\_SNSP} - V_{IIN\_SNSM}$ ) for high range, medium range and low range settings.

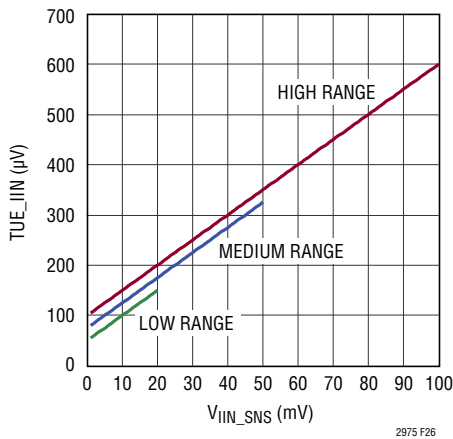


Figure 26. TUE\_IIN vs READ\_IIN Input Voltage in μV

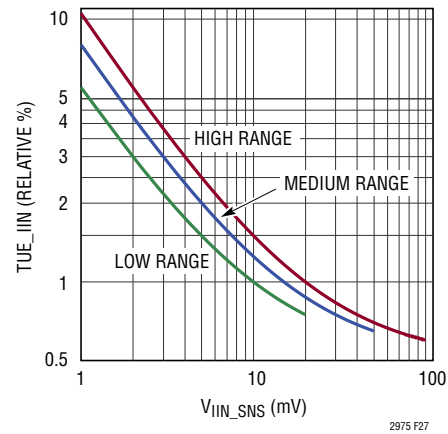


Figure 27. TUE\_IIN vs READ\_IIN Input Voltage in Percentage

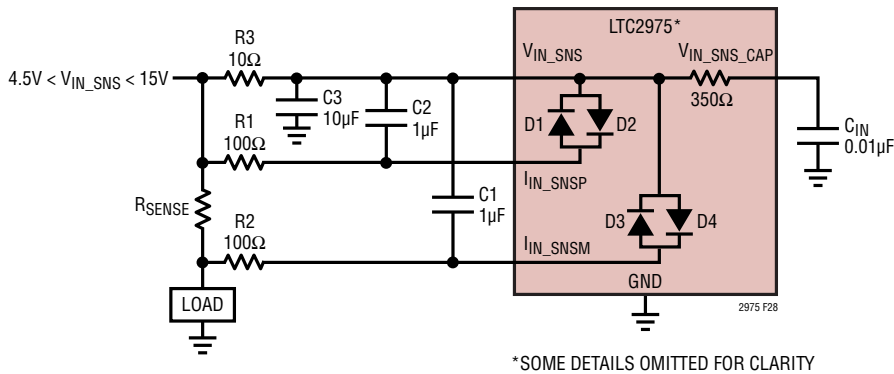


Figure 28. Optional  $V_{IN\_SNS}$  Filtering

## APPLICATIONS INFORMATION

### MEASURING INPUT VOLTAGE

READ\_VIN returns input voltage on the  $V_{IN\_SNS}$  pin. TUE\_VIN reflects READ\_VIN measurement error. Large ripple on the  $V_{IN\_SNS}$  pin may affect READ\_VIN, READ\_PIN, and MFR\_EIN accuracy. To reduce ripple induced measurement errors, consider adding the optional anti-aliasing filter components shown in Figure 28. R3 and C3 filter  $V_{IN\_SNS}$  with 30dB attenuation at 62.5kHz. R1, R2, C1, C2 add additional filtering for IIN\_SNS inputs and prevent the internal diodes, D1 to D4, from turning on.

### MEASURING INPUT POWER

READ\_PIN returns input power in watts calculated from the product of the most recent  $V_{VIN\_SNS}$  and  $I_{IN\_SNS}$  measurements. Although the Electrical Characteristics table only specifies READ\_PIN Total Unadjusted Error (TUE\_PIN) under typical conditions, TUE\_PIN is actually bounded by the sum of TUE\_IIN and TUE\_VIN.

$$TUE\_PIN \leq TUE\_IIN + TUE\_VIN$$

For example, if  $15mV < |V_{IIN\_SNS}| < 50mV$  with the current sense amplifier set for medium range,  $TUE\_IIN \leq 1\%$  and  $TUE\_PIN$  is less than  $1\% (TUE\_IIN) + 0.5\% (TUE\_VIN) = 1.5\%$ .

Since current sense ranges include positive and negative inputs, READ\_PIN returns signed values indicating power transfer magnitude and direction.

### MEASURING INPUT ENERGY

The 12 byte data block, MFR\_EIN, contains a 48-bit accumulated energy measurement in mJ, Energy\_value[47:0], and a 48-bit elapsed time in milliseconds since energy began accumulating, Energy\_time[47:0]. Refer to INPUT CURRENT AND ENERGY and MFR\_COMMAND\_PLUS sections of the PMBUS COMMAND DESCRIPTION for accumulated energy and elapsed time data access details. Energy\_value can accumulate up to  $(2^{48}-1)$  mJ of energy before wrapping. Energy can accumulate for  $(2^{48}-1)$  ms, or about 8925 years, before Energy\_time wraps. Accumulation of negative power measurements decreases Energy\_value, and the energy meter saturates when it reaches 0 millijoules.

The energy meter time base error (TUE\_ETB) specifies error in the internal energy time base accuracy: Energy\_time is accurate with maximum error of TUE\_ETB. Accumulated energy includes errors from current sense measurements, voltage sense measurements, and the internal time base. Energy\_value error (TUE\_EIN) is bounded by the summation of TUE\_IIN, TUE\_VIN, and TUE\_ETB:

$$TUE\_EIN \leq TUE\_IIN + TUE\_VIN + TUE\_ETB$$

For example, if  $V_{IIN\_SNS} = 20mV$  with high current sense amplifier range,  $TUE\_IIN$  is less than 1% error,  $TUE\_VIN$  is less than 0.5% error, and  $TUE\_ETB$  is less than 1.5% error. Therefore the energy measurement error ( $TUE\_EIN$ ) is less than 3%.

### SEQUENCE, SERVO, MARGIN AND RESTART OPERATIONS

#### Command Units On or Off

Three control parameters determine how a particular channel is turned on and off: The CONTROL pins, the OPERATION command and the value of the input voltage measured at the  $V_{IN\_SNS}$  pin ( $V_{IN}$ ). In all cases,  $V_{IN}$  must exceed  $V_{IN\_ON}$  in order to enable the device to respond to the CONTROL pins or OPERATION commands. When  $V_{IN}$  drops below  $V_{IN\_OFF}$  an immediate OFF or sequence off after  $TOFF\_DELAY$  of all channels will result (See Mfr\_track\_en\_chann). Refer to the OPERATION section in the data sheet for a detailed description of the ON\_OFF\_CONFIG command.

Some examples of typical ON/OFF configurations are:

1. A DC/DC converter may be configured to turn on any time  $V_{IN}$  exceeds  $V_{IN\_ON}$ .
2. A DC/DC converter may be configured to turn on only when it receives an OPERATION command.
3. A DC/DC converter may be configured to turn on only via the CONTROL pin.
4. A DC/DC converter may be configured to turn on only when it receives an OPERATION command and the CONTROL pin is asserted.

## APPLICATIONS INFORMATION

### On Sequencing

The `TON_DELAY` command sets the amount of time that a channel will wait following the start of an ON sequence before its `VOUT_EN` pin will enable a DC/DC converter. Once the DC/DC converter has been enabled, the `TON_RISE` value determines the time at which the device soft-connects the DAC and servos the DC/DC converter output to the `VOUT_COMMAND` value. The `TON_MAX_FAULT_LIMIT` value determines the time at which the device checks for an undervoltage condition. If a `TON_MAX_FAULT` occurs, the channel can be configured to disable the DC/DC converter and propagate the fault to other channels using the bidirectional `FAULTB` pins. Figure 29 shows a typical on-sequence using the `CONTROL` pin. Note that overvoltage faults are checked against the `VOUT_OV_FAULT_LIMIT` value at all times the device is powered up and not in a reset state nor margining while ignoring OVs.

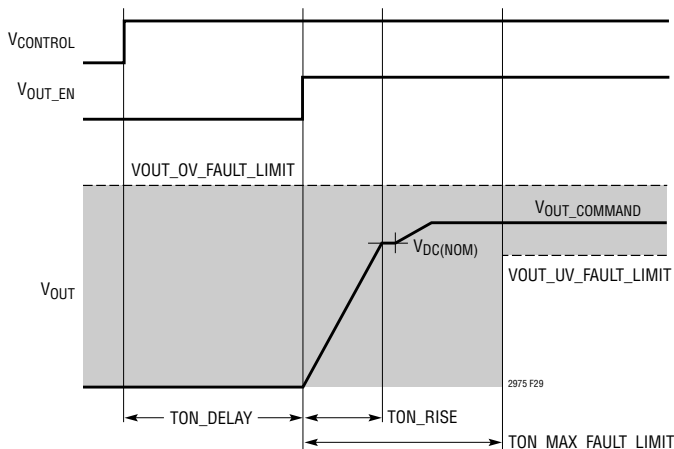


Figure 29. Typical ON Sequence Using Control Pin

### On State Operation

Once a channel has reached the ON state, the `OPERATION` command can be used to command the DC/DC converter's output to margin high, margin low, or return to a nominal output voltage indicated by `VOUT_COMMAND`. The user also has the option of configuring a channel to continuously trim the output of the DC/DC converter to the `VOUT_COMMAND` voltage, or the channel's `VDACn` output can be placed in a high impedance state thus allowing the DC/DC converter output voltage to go to its nominal value,

`VDCn(NOM)`. Refer to the `MFR_CONFIG_LTC2975` command for details on how to configure the output voltage servo.

### Servo Modes

The ADC, DAC and internal processor comprise a digital servo loop that can be configured to operate in several useful modes. The servo target refers to the desired output voltage.

Continuous/non-continuous trim mode: `MFR_CONFIG_LTC2975 b[7]`. In continuous trim mode, the servo will update the DAC in a closed loop fashion each time it takes a `VOUT` reading. The update rate is determined by the time it takes to step through the ADC MUX which is no more than `tUPDATE_ADC`. See Electrical Characteristics table Note 6. In non-continuous trim mode, the servo will drive the DAC until the ADC measures the output voltage desired and then stop updating the DAC.

As part of continuous/noncontinuous trim mode, fast servo mode can be used to speed up large output transitions, such as margin commands, or ON events. To use, set `Mfr_config_fast_servo_off = 0`. When enabled, fast servo is started by a change to the target voltage or a new softconnect. The DAC is ramped one lsb every `tS_VDAC` period until it is near the new target voltage, at which point slow servo mode is entered to avoid overshoot.

Non-continuous servo on warn mode: `MFR_CONFIG_LTC2975 b[7] = 0, b[6] = 1`. When in non-continuous mode, the LTC2975 will re-trim (re-servo) the output if the output drifts beyond the OV or UV warn limits.

### DAC Modes

The DACs that drive the `VDACn` pins can operate in several useful modes. See `MFR_CONFIG_LTC2975`.

- Soft-connect. Using the ADI patented soft-connect feature, the DAC output is driven to within 1 LSB of the voltage at the DC/DC's feedback node before connecting, to avoid introducing transients on the output. This mode is used when servoing the output voltage. During startup, the LTC2975 waits until `TON_RISE` has expired before connecting the DAC. This is the most common operating mode.
- Disconnected. DAC output is high Z.



## APPLICATIONS INFORMATION

- DAC manual with soft-connect. Non servo mode. The DAC soft connects to the feedback node. Soft-connect drives the DAC code to match the voltage at the feedback node. After connection, the DAC is moved by writing DAC codes to the MFR\_DAC.
- DAC manual with hard connect. Non servo mode. The DAC hard connects to the feedback node using the current value in MFR\_DAC. After connection, the DAC is moved by writing DAC codes to the MFR\_DAC.

### Margining

The LTC2975 margins and trims the output of a DC/DC converter by forcing a voltage across an external resistor connected between the DAC output and the feedback node or the trim pin. Preset limits for margining are stored in the VOUT\_MARGIN\_HIGH/LOW registers. Margining is actuated by writing the appropriate bits to the OPERATION register.

Margining requires the DAC to be connected. Margin requests that occur when the DAC is disconnected will be ignored.

### Off Sequencing

An off sequence is initiated using the CONTROL pin or the OPERATION command. The TOFF\_DELAY value determines the amount of time that elapses from the beginning of the off sequence until each channel's V<sub>OUT\_EN</sub> pin is pulled low, thus disabling its DC/DC converter.

### V<sub>OUT</sub> Off Threshold Voltage

The MFR\_VOUT\_DISCHARGE\_THRESHOLD command register allows the user to specify the OFF threshold that the output voltage must decay below before the channel can enter/re-enter the ON state. The OFF threshold voltage is specified by multiplying MFR\_VOUT\_DISCHARGE\_THRESHOLD and VOUT\_COMMAND. In the event that an output voltage has not decayed below its OFF threshold before attempting to enter the ON state, the channel will continue to be held off, the appropriate bit is set in the STATUS\_MFR\_SPECIFIC register, and the ALERTB pin will be asserted low. When the output voltage has decayed below its OFF threshold, the channel can enter the ON state.

### Automatic Restart via MFR\_RESTART\_DELAY Command and CONTROL Pin

An automatic restart sequence can be initiated by driving the CONTROL pin to the off state for >10 $\mu$ s and then releasing it. The automatic restart disables all V<sub>OUT\_EN</sub> pins that are mapped to a particular CONTROL pin for a time period = MFR\_RESTART\_DELAY and then starts all DC/DC Converters according to their respective TON\_DELAYS. (see Figure 30). V<sub>OUT\_EN</sub> pins are mapped to one of the CONTROL pins by the MFR\_CONFIG\_LTC2975 command. This feature allows a host that is about to reset to restart the power in a controlled manner after it has recovered.

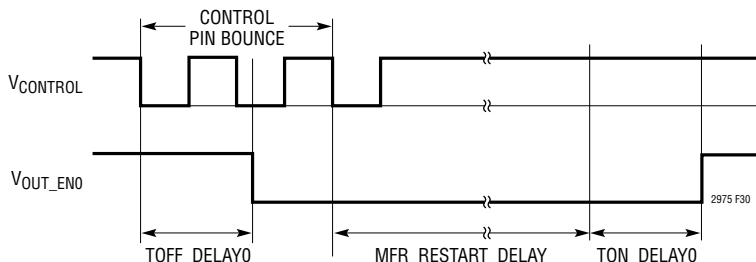


Figure 30. Off Sequence with Automatic Restart

## APPLICATIONS INFORMATION

### FAULT MANAGEMENT

#### Output Overvoltage, Undervoltage, Overcurrent and Undercurrent Faults

The high-speed voltage supervisor OV and UV fault thresholds are configured using the VOUT\_OV\_FAULT\_LIMIT and VOUT\_UV\_FAULT\_LIMIT commands, respectively. The VOUT\_OV\_FAULT\_RESPONSE and VOUT\_UV\_FAULT\_RESPONSE commands determine the responses to OV/UV faults. In addition, the high-speed current supervisor OC and UC fault thresholds are configured using the IOUT\_OC\_FAULT\_LIMIT and IOUT\_UC\_FAULT\_LIMIT commands, respectively. The IOUT\_OC\_FAULT\_RESPONSE and IOUT\_UC\_FAULT\_RESPONSE commands determine the responses to OC/UC faults. Fault responses can range from disabling the DC/DC converter immediately, waiting to see if the fault condition persists for some interval before disabling the DC/DC converter, or allowing the DC/DC converter to continue operating in spite of the fault. If a DC/DC converter is disabled, the LTC2975 can be configured to retry one to six times, retry continuously without limitation, or latch-off. The retry interval is specified using the MFR\_RETRY\_DELAY command. Latched faults are reset by toggling the CONTROL pin, using the OPERATION command, or removing and reapplying the bias voltage to the V<sub>IN\_SNS</sub> pin. All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR\_FAULTS command resets the contents of the status registers and de-asserts the ALERTB output.

#### Output Overvoltage, Undervoltage, and Overcurrent Warnings

OV, UV, and OC warning thresholds are processed by the LTC2975's ADC. These thresholds are set by the VOUT\_OV\_WARN\_LIMIT, VOUT\_UV\_WARN\_LIMIT, and IOUT\_OC\_WARN\_LIMIT commands, respectively. Note that there is no IOUT\_UC warning threshold. If a warning occurs, the corresponding bits are set in the status registers and the ALERTB output is asserted low. Note that a warning will never cause a V<sub>OUT\_EN</sub> output pin to disable a DC/DC converter.

#### Configuring the AUXFAULTB Output

The AUXFAULTB output may be used to indicate an output OV, OC, or UC fault. Use the MFR\_CONFIG2\_LTC2975 and MFR\_CONFIG3\_LTC2975 registers to configure the AUXFAULTB pin to assert low in response to VOUT\_OV, IOUT\_OC or IOUT\_UC fault conditions. The AUXFAULTB output will stop pulling low when the LTC2975 is commanded to re-enter the ON state following a faulted-off condition.

A charge-pumped 5 $\mu$ A pull-up to 12V is also available on the AUXFAULTB output. Refer to the MFR\_CONFIG\_ALL\_LTC2975 register description in the PMBUS COMMAND DESCRIPTION section for more information.

Figure 31 shows an application circuit where the AUXFAULTB output is used to trigger an SCR crowbar on the intermediate bus in order to protect the DC/DC converter's load from a catastrophic fault such as a stuck top gate. The stuck top gate causes an OV fault, which in turn causes the LTC2975 to pull AUXFAULTB low, thus deasserting the ON input to the LTC4210 hot-swap controller, which opens the switch Q1 that supplies the DC/DC converter input. In addition, when AUXFAULTB goes low it forces the S4010DS3 SCR device into the on-state via the 2N2907 PNP, thus quickly dropping the voltage on the V<sub>IN</sub> input to the DC/DC converter, preventing the stuck top gate from damaging components supplied by this converter. Note that the V<sub>PWR</sub> input to the LTC2975 bypasses switch Q1, keeping the LTC2975 fully powered throughout the above sequence.

#### Multi-Channel Fault Management

Multi-channel fault management is handled using the bidirectional FAULTB pins. Figure 32 illustrates the connections between channels and the FAULTB pins.

- The MFR\_FAULTB<sub>n</sub>\_PROPAGATE command acts like a programmable switch that allows faulted\_off conditions from a particular channel (PAGE) to propagate to either FAULTB output. The MFR\_FAULTB<sub>n</sub>\_RESPONSE command controls similar switches on the inputs to each channel that allow any channel to shut down in response to any combination of the FAULTB pins.

# APPLICATIONS INFORMATION

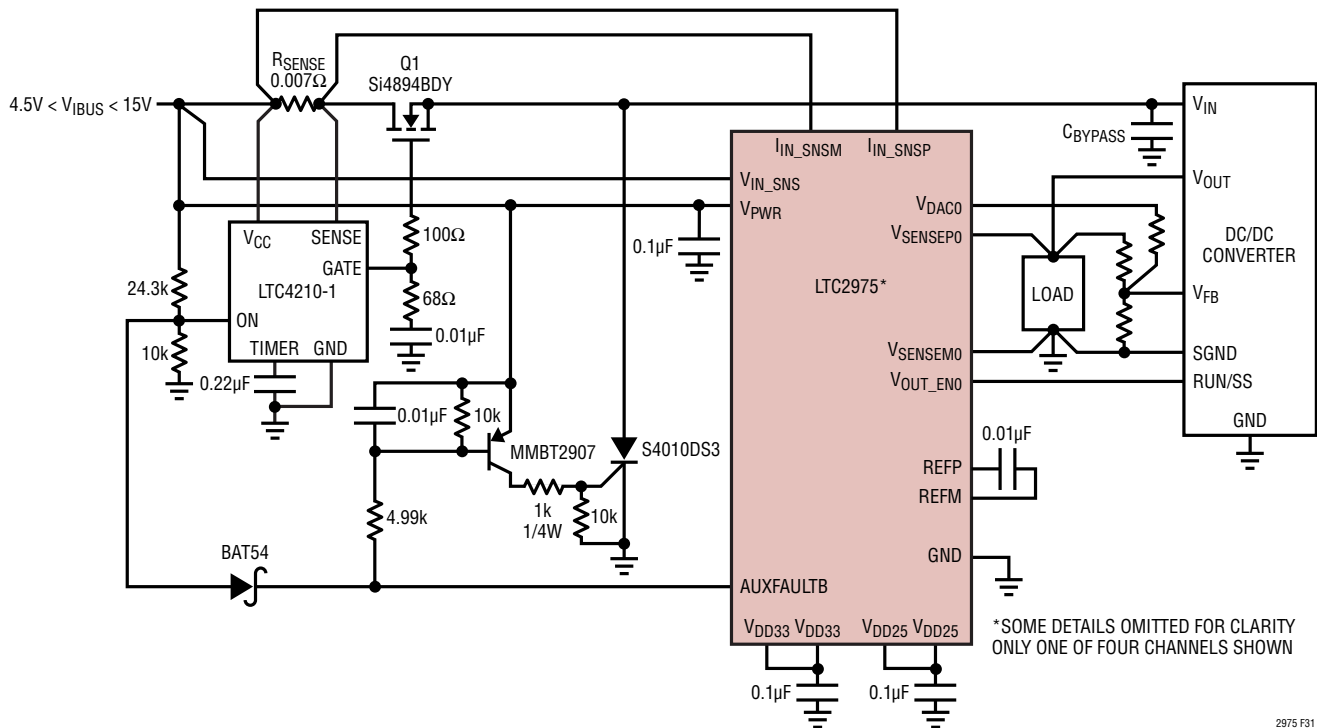


Figure 31. Application Circuit with Crowbar Protection on Intermediate Bus

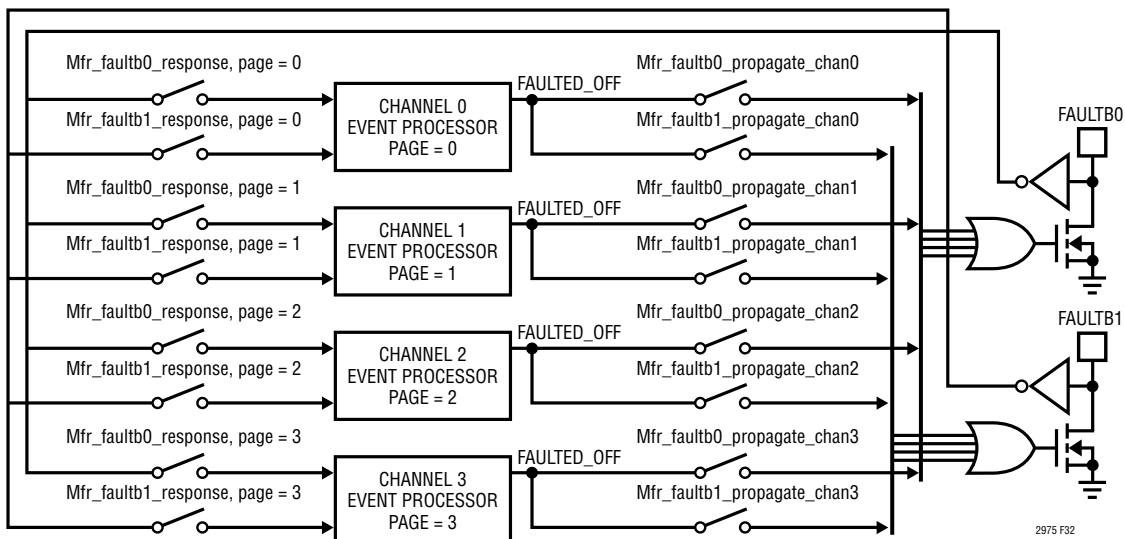


Figure 32. Channel Fault Management Block Diagram

## APPLICATIONS INFORMATION

Channels responding to a FAULTB pin pulling low will attempt a new start sequence when the FAULTB pin in question is released by the faulted channel.

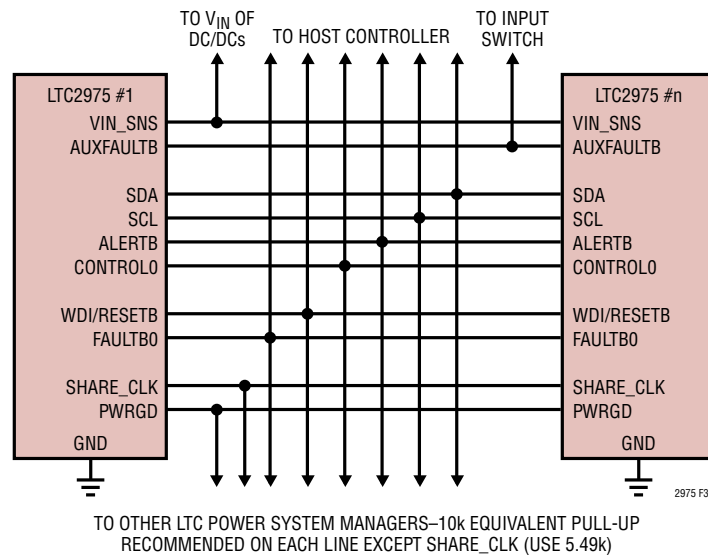
- A FAULTB pin can also be asserted low by an external driver in order to initiate an immediate off-sequence after a 10μs deglitch delay.

### INTERCONNECT BETWEEN MULTIPLE ADI POWER MANAGERS

Figure 33 shows how to interconnect the pins in a typical multi-LTC2975 array.

- All  $V_{IN\_SNS}$  lines should be tied together in a star type connection at the point where  $V_{IN}$  is to be sensed. This will minimize timing errors for the case where the ON\_OFF\_CONFIG is configured to start the LTC2975 based on  $V_{IN}$  and ignore the CONTROL line and the OPERATION command. In multi-part applications that are sensitive to timing differences, it is recommended that the Vin\_share\_enable bit of the MFR\_CONFIG\_ALL\_LTC2975 register be set high in order to allow SHARE\_CLK to synchronize on/off sequencing in response to the VIN\_ON and VIN\_OFF thresholds.

- Connecting all AUXFAULTB lines together will allow selected faults on any DC/DC converter's output in the array to shut off a common input switch.
- ALERTB is typically one line in an array of PMBus converters. The LTC2975 allows a rich combination of faults and warnings to be propagated to the ALERTB pin.
- WDI/RESETB can be used to put the LTC2975 in the power-on reset state. Pull WDI/RESETB low for at least  $t_{RESETB}$  to enter this state.
- The FAULTB lines can be connected together to create fault dependencies. Figure 33 shows a configuration where a fault on any FAULTB will pull all others low. This is useful for arrays where it is desired to abort a startup sequence in the event any channel does not come up (see Figure 34).
- PWRGD reflects the status of the outputs that are mapped to it by the MFR\_PWRGD\_EN command. Figure 33 shows all the PWRGD pins connected together, but any combination may be used.



**Figure 33. Typical Connections Between Multiple ADI Power System Managers**

## APPLICATIONS INFORMATION

### APPLICATION CIRCUITS

#### Trimming and Margining DC/DC Converters with External Feedback Resistors

Figure 35 shows a typical application circuit for trimming/margining a power supply with an external feedback

network. The  $V_{SENSE0}$  and  $V_{SENSEM0}$  differential inputs sense the load voltage directly, and a correction voltage is developed on the  $V_{DAC0}$  pin by the closed-loop servo algorithm. The  $V_{DAC0}$  output is connected to the DC/DC converter's feedback node through resistor R30. For this configuration, set  $Mfr\_config\_dac\_pol$  to 0.

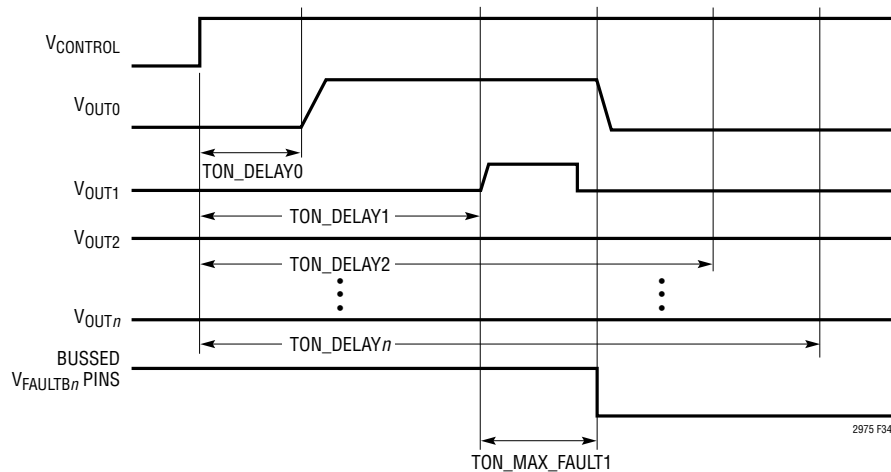
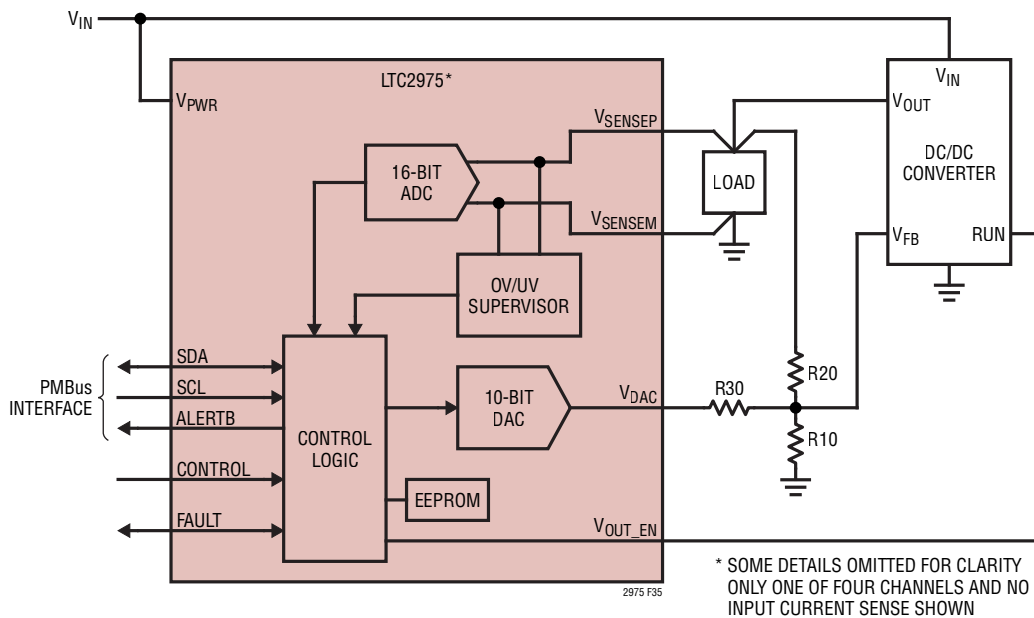


Figure 34. Aborted On-Sequence Due to Channel 1 Short



\* SOME DETAILS OMITTED FOR CLARITY  
ONLY ONE OF FOUR CHANNELS AND NO  
INPUT CURRENT SENSE SHOWN

Figure 35. Application Circuit for DC/DC Converters with External Feedback Resistors

## APPLICATIONS INFORMATION

### Four-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors

The following four-step procedure should be used to calculate the resistor values required for the application circuit shown in Figure 35.

1. Assume values for feedback resistor R20 and the nominal DC/DC converter output voltage  $V_{DC(NOM)}$ , and solve for R10.

$V_{DC(NOM)}$  is the output voltage of the DC/DC converter when the LTC2975's  $V_{DAC0}$  pin is in a high impedance state. R10 is a function of R20,  $V_{DC(NOM)}$ , the voltage at the feedback node ( $V_{FB}$ ) when the loop is in regulation, and the feedback node's input current ( $I_{FB}$ ).

$$R10 = \frac{R20 \cdot V_{FB}}{V_{DC(NOM)} - I_{FB} \cdot R20 - V_{FB}} \quad (1)$$

2. Solve for the value of R30 that yields the maximum required DC/DC converter output voltage  $V_{DC(MAX)}$ .

When  $V_{DAC0}$  is at 0V, the output of the DC/DC converter is at its maximum voltage.

$$R30 \leq \frac{R20 \cdot V_{FB}}{V_{DC(MAX)} - V_{DC(NOM)}} \quad (2)$$

3. Solve for the minimum value of  $V_{DAC0}$  that's needed to yield the minimum required DC/DC converter output voltage  $V_{DC(MIN)}$ .

The DAC has two full-scale settings, 1.38V and 2.65V. In order to select the appropriate full-scale setting, calculate the minimum required  $V_{FS\_VDAC}$  output voltage:

$$V_{FS\_VDAC} > (V_{DC(NOM)} - V_{DC(MIN)}) \cdot \frac{R30}{R20} + V_{FB} \quad (3)$$

4. Re-calculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

$$V_{DC(NOM)} = V_{FB} \cdot \left(1 + \frac{R20}{R10}\right) + I_{FB} \cdot R20 \quad (4)$$

$$V_{DC(MIN)} = V_{DC(NOM)} - \frac{R20}{R30} \cdot (V_{FS\_VDAC} - V_{FB}) \quad (5)$$

$$V_{DC(MAX)} = V_{DC(NOM)} + \frac{R20}{R30} \cdot V_{FB} \quad (6)$$

$$V_{RES} = \frac{\frac{R20}{R30} \cdot V_{FS\_VDAC}}{1023} \text{ V/DAC LSB} \quad (7)$$

### Trimming and Margining DC/DC Converters with a TRIM Pin

Figure 36 illustrates a typical application circuit for trimming/margining the output voltage of a DC/DC converter with a TRIM Pin. The LTC2975's  $V_{DAC0}$  pin connects to the TRIM pin through resistor R30. For this configuration, set the DAC polarity bit `Mfr_config_dac_pol` in `MFR_CONFIG_LTC2975` to 1.

DC/DC converters with a TRIM pin may be margined high or low by connecting an external resistor between the TRIM pin and either the  $V_{SENSEP}$  or  $V_{SENSEM}$  pin. The relationships between these resistors and the  $\Delta\%$  change in the output voltage of the DC/DC converter are typically expressed as:

$$R_{TRIM\_DOWN} = \frac{R_{TRIM} \cdot 50}{\Delta_{DOWN}\%} - R_{TRIM} \quad (8)$$

$$R_{TRIM\_UP} =$$

$$R_{TRIM} \cdot \left[ \frac{V_{DC} \cdot (100 + \Delta_{UP}\%)}{2 \cdot V_{REF} \cdot \Delta_{UP}\%} - \left( \frac{50}{\Delta_{UP}\%} \right) - 1 \right] \quad (9)$$

where  $R_{TRIM}$  is the resistance looking into the TRIM pin,  $V_{REF}$  is the TRIM pin's open-circuit output voltage and  $V_{DC}$  is the DC/DC converter's nominal output voltage.  $\Delta_{UP}\%$  and  $\Delta_{DOWN}\%$  denote the percentage change in the converter's output voltage when margining up or down, respectively.

## APPLICATIONS INFORMATION

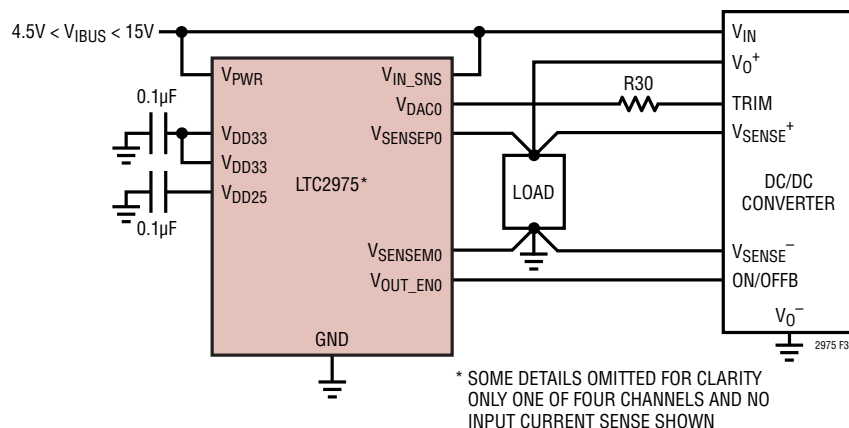


Figure 36. Application Circuit for DC/DC Converters with Trim Pin

### Two-Step Resistor and DAC Full-Scale Voltage Selection Procedure for DC/DC Converters with a TRIM Pin

The following two-step procedure should be used to calculate the resistor value for R<sub>30</sub> and the required full-scale DAC voltage (refer to Figure 36).

1. Solve for R<sub>30</sub>:

$$R_{30} \leq R_{\text{TRIM}} \cdot \left( \frac{50 - \Delta_{\text{DOWN}\%}}{\Delta_{\text{DOWN}\%}} \right) \quad (10)$$

2. Calculate the maximum required output voltage for V<sub>DAC0</sub>:

$$V_{\text{DAC0}} \geq \left( 1 + \frac{\Delta_{\text{UP}\%}}{\Delta_{\text{DOWN}\%}} \right) \cdot V_{\text{REF}} \quad (11)$$

Note: Not all DC/DC converters follow these trim equations, especially newer bricks. Consult ADI Field Application Engineering.

### Measuring Output with a Sense Resistor

A circuit for measuring current with a sense resistor is shown in Figure 37. The balanced filter rejects both common mode and differential mode noise from the output of the DC/DC converter. The filter is placed directly across the sense resistor in series with the DC/DC converter's inductor. Note that the current sense inputs must be limited to less than 6V with respect to ground. Select R<sub>CM</sub> and C<sub>CM</sub> such that the filter's corner frequency is < 1/10 the DC/DC converter's switching frequency. This will result in a current sense waveform that offers a good compromise

between the voltage ripple and the delay through the filter. A value 1kΩ for R<sub>CM</sub> is suggested in order to minimize gain errors due to the current sense inputs' internal resistance.

### Measuring Output with Inductor DCR

Figure 38 shows the circuit for applications that require DCR current sense. A second order R-C filter is required in these applications in order to minimize the ripple voltage seen at the current sense inputs. A value of 1kΩ is suggested for R<sub>CM1</sub> and R<sub>CM2</sub> in order to minimize gain errors due the current sense inputs' internal resistance. C<sub>CM1</sub> should be selected to provide cancellation of the zero created by the DCR and inductance, i.e. C<sub>CM1</sub> = L/(DCR • R<sub>CM1</sub>). C<sub>CM2</sub> should be selected to provide a second stage corner frequency at < 1/10 of the

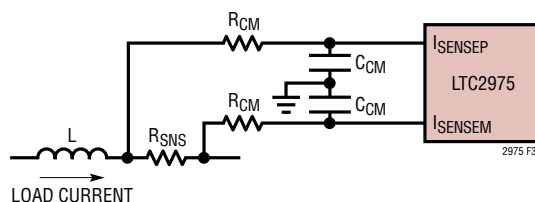


Figure 37. Sense Resistor Current Sensing Circuits

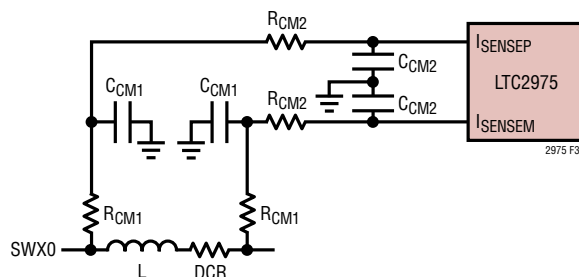


Figure 38. DCR Current Sensing Circuits

## APPLICATIONS INFORMATION

DC/DC converter's switching frequency. In addition,  $C_{CM2}$  needs to be much smaller than  $C_{CM1}$  in order to prevent significant loading of the filter's first stage.

### Single Phase Design Example

As a design example for a DCR current sense application, assume  $L = 2.2\mu\text{H}$ ,  $\text{DCR} = 10\text{m}\Omega$ , and  $F_{\text{SW}} = 500\text{kHz}$ .

Let  $R_{CM1} = 1\text{k}\Omega$  and solve for  $C_{CM1}$ :

$$C_{CM1} \geq \frac{2.2\mu\text{H}}{10\text{m}\Omega \cdot 1\text{k}\Omega} = 220\text{nF}$$

Let  $R_{CM2} = 1\text{k}\Omega$ . In order to get a second pole at  $F_{\text{SW}}/10 = 50\text{kHz}$ :

$$C_{CM2} \cong \frac{1}{2\pi \cdot 50\text{kHz} \cdot 1\text{k}\Omega} = 3.18\text{nF}$$

Let  $C_{CM2} = 3.3\text{nF}$ . Note that since  $C_{CM2}$  is much less than  $C_{CM1}$  the loading effects of the second stage filter on the matched first stage are not significant. Consequently, the delay time constant through the filter for the current sense waveform will be approximately  $3\mu\text{s}$ .

### Measuring Multiphase Currents

For current sense applications with more than one phase, R-C averaging may be employed. Figure 39 shows an example of this approach for a 3-phase system with DCR current sensing. The current sense waveforms are averaged

together prior to being applied to the second stage of the filter consisting of  $R_{CM2}$  and  $C_{CM2}$ . Because the  $R_{CM1}$  resistors for the three phases are in parallel, the value of  $R_{CM1}$  must be multiplied by the number of phases. Also note that since the DCRs are effectively in parallel, the value for  $\text{IOUT\_CAL\_GAIN}$  will be equal to the inductor's DCR divided by the number of phases. Care should be taken in the layout of the multiphase inductors to keep the PCB trace resistance from the DC side of each inductor to the summing node balanced in order to provide the most accurate results.

### Multiphase Design Example

Using the same values for inductance and DCR from the previous design example, the value for  $R_{CM1}$  will be  $3\text{k}\Omega$  for a three phase DC/DC converter if  $C_{CM1}$  is left at  $220\text{nF}$ . Similarly, the value for  $\text{IOUT\_CAL\_GAIN}$  will be  $\text{DCR}/3 = 3.33\text{m}\Omega$ .

### Anti-aliasing Filter Considerations

Noisy environments require an anti-aliasing filter on the input to the LTC2975's ADC. The R-C circuit shown in Figure 40 is adequate for most situations. Keep  $R_{40} = R_{50} \leq 200\Omega$  to minimize ADC gain errors, and select a value for capacitors  $C_{10}$  and  $C_{20}$  that doesn't add too much additional response time to the OV/UV supervisor, e.g.  $\tau = 10\mu\text{s}$  ( $R = 100\Omega$ ,  $C = 0.10\mu\text{F}$ ).

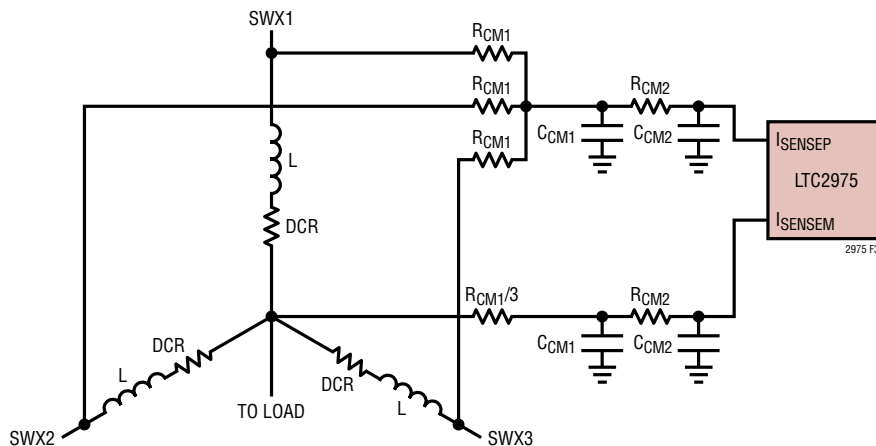


Figure 39. Multiphase DCR Current Sensing Circuits



## APPLICATIONS INFORMATION

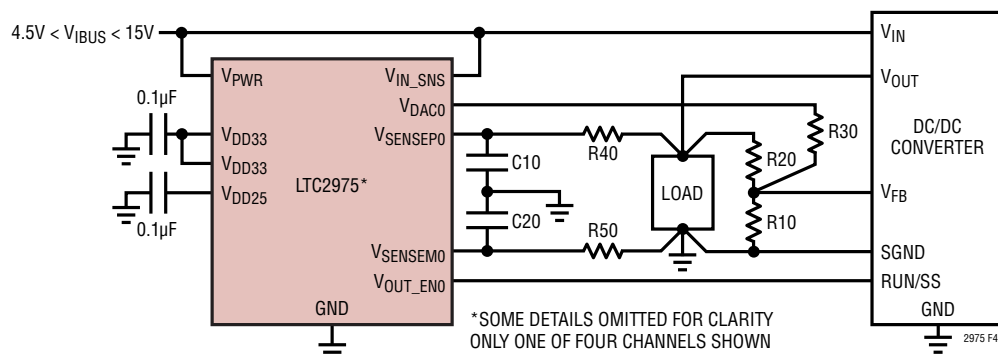


Figure 40. Anti-Aliasing Filter on VSENSE Lines

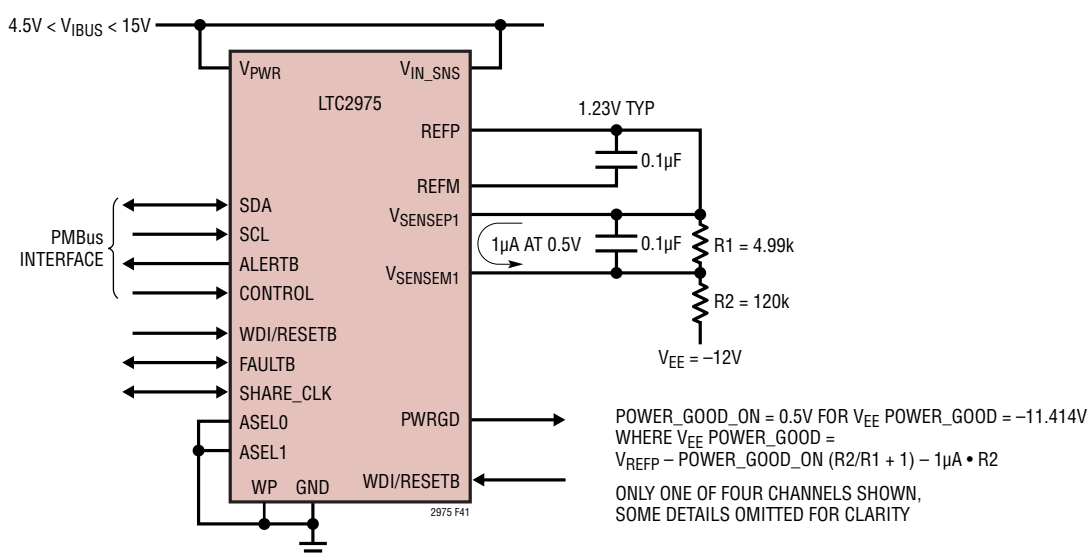


Figure 41. Sensing Negative Voltages

## Sensing Negative Voltages

Figure 41 shows the LTC2975 sensing a negative power supply ( $V_{EE}$ ). The R1/R2 resistor divider translates the negative supply voltage to the LTC2975's  $V_{SENSEM1}$  input while the  $V_{SENSEP1}$  input is tied to the REFP pin which has a typical output voltage of 1.23V. The voltage divider should be configured in order to present about 0.5V to the voltage sense inputs when the negative supply reaches its  $POWER\_GOOD\_ON$  threshold so that the current flowing out of the  $V_{SENSEMn}$  pin is minimized to  $\sim 1\mu A$ . The relationship between the  $POWER\_GOOD\_ON$  register value and the corresponding negative supply value can be expressed as:

$$V_{EE} = V_{REFP} - (\text{READ\_VOUT}) \cdot \left( \frac{R2}{R1} + 1 \right) - 1\mu A \cdot R2$$

where  $READ\_VOUT$  returns  $V_{SENSEP} - V_{SENSEM}$

Connecting the DC1613 USB to I<sup>2</sup>C/SMBus/PMBus Controller to the LTC2975 in System

The DC1613 USB to I<sup>2</sup>C/SMBus/PMBus Controller can be interfaced to the LTC2975s on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay software, provides a powerful way to debug an entire power system. Failures are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTC2975's EEPROM.

Rev. D

## APPLICATIONS INFORMATION

Figure 42 and Figure 43 illustrate application schematics for powering, programming and communicating with one or more LTC2975's via the ADI I<sup>2</sup>C/SMBus/PMBus controller regardless of whether or not system power is present.

Figure 42 shows the recommended schematic to use when the LTC2975 is powered by the system intermediate bus through its V<sub>PWR</sub> pin.

Figure 43 shows the recommended schematic to use when the LTC2975 is powered by the system 3.3V through its V<sub>DD33</sub> and V<sub>PWR</sub> pins. The LTC4412 ideal ORing circuit allows either the controller or system to power the LTC2975.

Because of the controller's limited current sourcing capability, only the LTC2975s, their associated pull-up resistors and the I<sup>2</sup>C/SMBus pull-up resistors should be powered from the ORed 3.3V supply. In addition, any device sharing I<sup>2</sup>C/SMBus bus connections with the LTC2975 should not have body diodes between the SDA/SCL pins and its V<sub>DD</sub> node because this will interfere with bus communication in the absence of system power.

The ADI controller's I<sup>2</sup>C/SMBus connections are opto-isolated from the PC's USB. The 3.3V from the controller and the LTC2975's V<sub>DD33</sub> pin can be paralleled because the ADI LDOs that generate these voltages can be back driven and draw <10μA. The controller's 3.3V current limit is 100mA.

## ACCURATE DCR TEMPERATURE COMPENSATION

Using the DC resistance of the inductor as a current shunt element has several advantages – no additional power loss, lower circuit complexity and cost. However, the strong temperature dependence of the inductor resistance and the difficulty in measuring the exact inductor core temperature introduce errors in the current measurement. For copper, a change of inductor temperature of only 1°C corresponds to approximately 0.39% current gain change. Figure 44 shows a sample layout using the integrated DC/DC converter LTC3601 (right) and its corresponding thermal image (left). The converter is providing 1.8V, 1.5A to the output load.

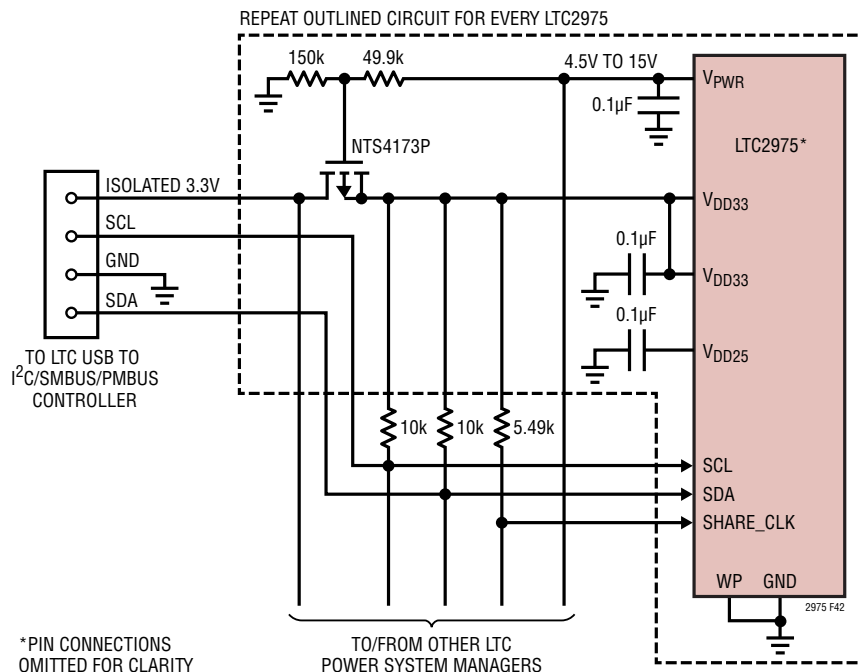


Figure 42. ADI Controller Connections When V<sub>PWR</sub> Is Used

# APPLICATIONS INFORMATION

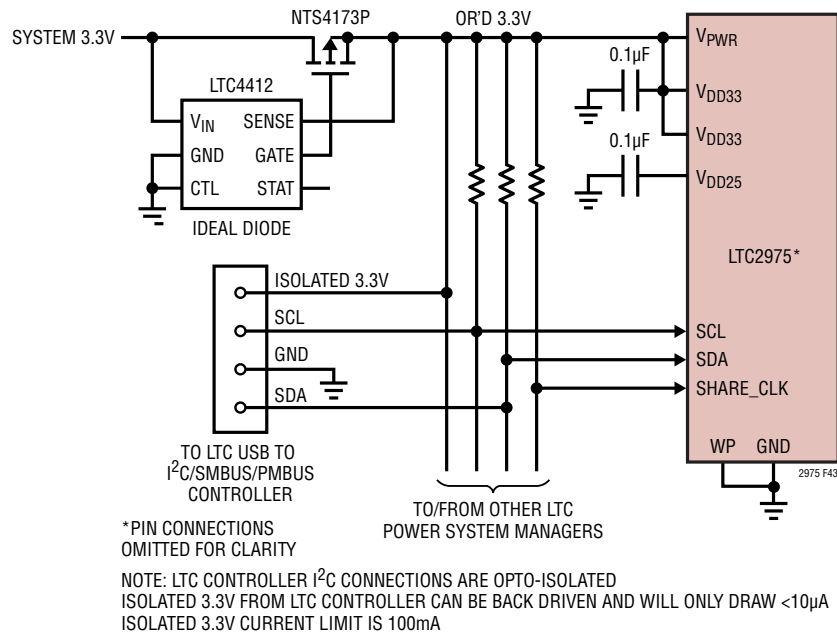


Figure 43. ADI Controller Connections When LTC2975 Is Powered Directly from 3.3V

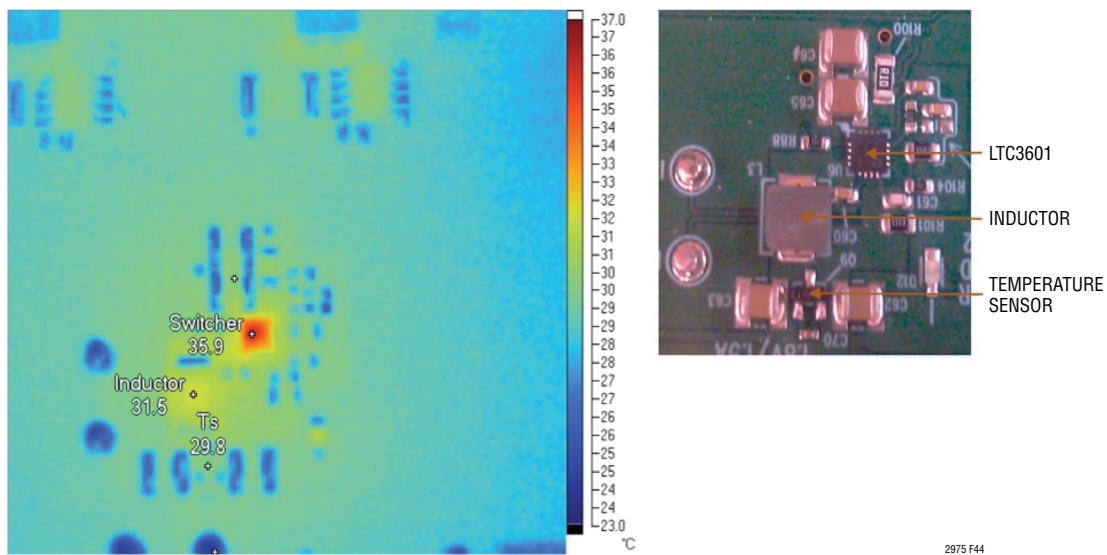


Figure 44. Thermal Image of a DC/DC Converter Showing the Difference Between the Actual Inductor Temperature and the Temperature Sensing Point

## APPLICATIONS INFORMATION

Heat dissipation in the inductor under high load conditions creates transient and steady state thermal gradients between the inductor and the temperature sensor, and the sensed temperature does not accurately represent the inductor core temperature. This temperature gradient is clearly visible in the thermal image of Figure 44. In addition, transient heating/cooling effects have to be accounted for in order to reduce the transient errors introduced when load current changes are faster than heat transfer time constants of the inductor. Both of these problems are addressed by introducing two additional parameters: the thermal resistance  $\theta_{IS}$  from the inductor core to the on-board temperature sensor, and the inductor thermal time constant  $\tau$ . The thermal resistance  $\theta_{IS}$  [ $^{\circ}\text{C}/\text{W}$ ], is used to calculate the steady state difference between the sensed temperature  $T_S$  and the internal inductor temperature  $T_I$  for a given power dissipated in the inductor  $P_I$ :

$$T_I - T_S = \theta_{IS} P_I = \theta_{IS} V_{DCR} I_{OUT} \quad (1.1)$$

The additional temperature rise is used for a more accurate estimate of the inductor DC resistance  $R_I$ :

$$R_I = R_0 (1 + \alpha [T_S - T_{REF} + \theta_{IS} V_{DCR} I_{OUT}]) \quad (1.2)$$

In these equations,  $V_{DCR}$  is the inductor DC voltage drop,  $I_{OUT}$  is the RMS value of the output current,  $R_0$  is the inductor DC resistance at the reference temperature  $T_{REF}$  and  $\alpha$  is the temperature coefficient of the resistance. Since most inductors are made of copper, we can expect a temperature coefficient close to  $\alpha_{CU} = 3900\text{ppm}/^{\circ}\text{C}$ . For a given  $\alpha$ , the remaining parameters  $\theta_{IS}$  and  $R_0$  can be calibrated at a single temperature using only two load currents:

$$R_0 = \frac{(R_2 - R_1)(P_2 + P_1) - (R_2 + R_1)(P_2 - P_1)}{\alpha(T_2 - T_1)(P_2 + P_1) - (P_2 - P_1)(2 + \alpha[T_1 + T_2 - 2T_{REF}])} \quad (1.3)$$

$$\theta_{IS} = \frac{1}{\alpha R_0} \frac{\alpha(R_1 + R_2)(T_2 - T_1) - (R_2 - R_1)(2 + \alpha[T_1 + T_2 - 2T_{REF}])}{\alpha(T_2 - T_1)(P_2 + P_1) - (P_2 - P_1)(2 + \alpha[T_1 + T_2 - 2T_{REF}])} \quad (1.4)$$

The inductor resistance,  $R_K = V_{DCR(K)}/I_{OUT(K)}$ , power dissipation  $P_K = V_{DCR(K)} I_{OUT(K)}$  and the sensed temperature  $T_K$ , ( $K = 1, 2$ ) are recorded for each load current. To increase the accuracy in calculating  $\theta_{IS}$ , the two load currents should be chosen around  $I_1 = 10\%$  and  $I_2 = 90\%$  of the current range of the system.

The inductor thermal time constant  $\tau$  models the first order thermal response of the inductor and allows accurate DCR compensation during load transients. During a transition from low to high load current, the inductor resistance increases due to the self-heating. If we apply a single load step from the low current  $I_1$  to the higher current  $I_2$ , the voltage across the inductor will change instantaneously from  $I_1 R_1$  to  $I_2 R_1$  and then slowly approach  $I_2 R_2$ . Here  $R_1$  is the steady state resistance at the given temperature and load current  $I_1$ , and  $R_2$  is the slightly higher DC resistance at  $I_2$ , due to the inductor self-heating. Note that the electrical time constant  $\tau_{EL} = L/R$  is several orders of magnitude shorter than the thermal one, and “instantaneous” is relative to the thermal time constant. The two settled regions give us the data sets ( $I_1, T_1, R_1, P_1$ ) and ( $I_2, T_2, R_2, P_2$ ) and the two-point calibration technique (1.3-1.4) is used to extract the steady-state parameters  $\theta_{IS}$  and  $R_0$  (given a previously characterized average  $\alpha$ ). The relative current error calculated using the steady-state expression (1.2) will peak immediately after the load step, and then decay to zero with the inductor thermal time constant  $\tau$ .

$$\frac{\Delta I}{I}(t) = \alpha \theta_{IS} (V_2 \cdot I_2 - V_1 \cdot I_1) e^{-t/\tau} \quad (1.5)$$

The time constant  $\tau$  is calculated from the slope of the best-fit line  $y = \ln(\Delta I/I) = a_1 + a_2 t$ :

$$\tau = -\frac{1}{a_2} \quad (1.6)$$

In summary, a single load current step is all that is needed to calibrate the DCR current measurement. The stable portions of the response give us the thermal resistance  $\theta_{IS}$  and nominal DC resistance  $R_0$ , and the settling characteristic is used to measure the inductor thermal time constant  $\tau$ .

To get the best performance, the temperature sensor has to be as close as possible to the inductor and away from other significant heat sources. For example in Figure 44, the bipolar sense transistor is close to the inductor and away from the switcher. Connect the collector of the PNP to the base. Route the base and emitter separately to the LTC2975. Connect base and collector to the signal ground close to LTC2975.

## APPLICATIONS INFORMATION

### LTpowerPlay: AN INTERACTIVE GUI FOR POWER MANAGERS

LTpowerPlay is a powerful Windows based development environment that supports Analog Devices power manager ICs with EEPROM, including the LTC2975. The software supports a variety of different tasks. You can use LTpowerPlay to evaluate Analog Devices ICs by connecting to a demo board system. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build a multi-chip configuration file that can be saved and re-loaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It

becomes a valuable diagnostic tool during board bring-up to program the power management scheme in a system. LTpowerPlay utilizes Analog Devices' DC1613 USB-to-I<sup>2</sup>C/SMBus/PMBus Controller to communicate with one of many potential targets including the DC2022 demo board set, the DC1508 socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the software current with the latest set of device drivers and documentation. A great deal of context sensitive help is available within LTpowerPlay along with several tutorial demos. [Complete information is available.](#)

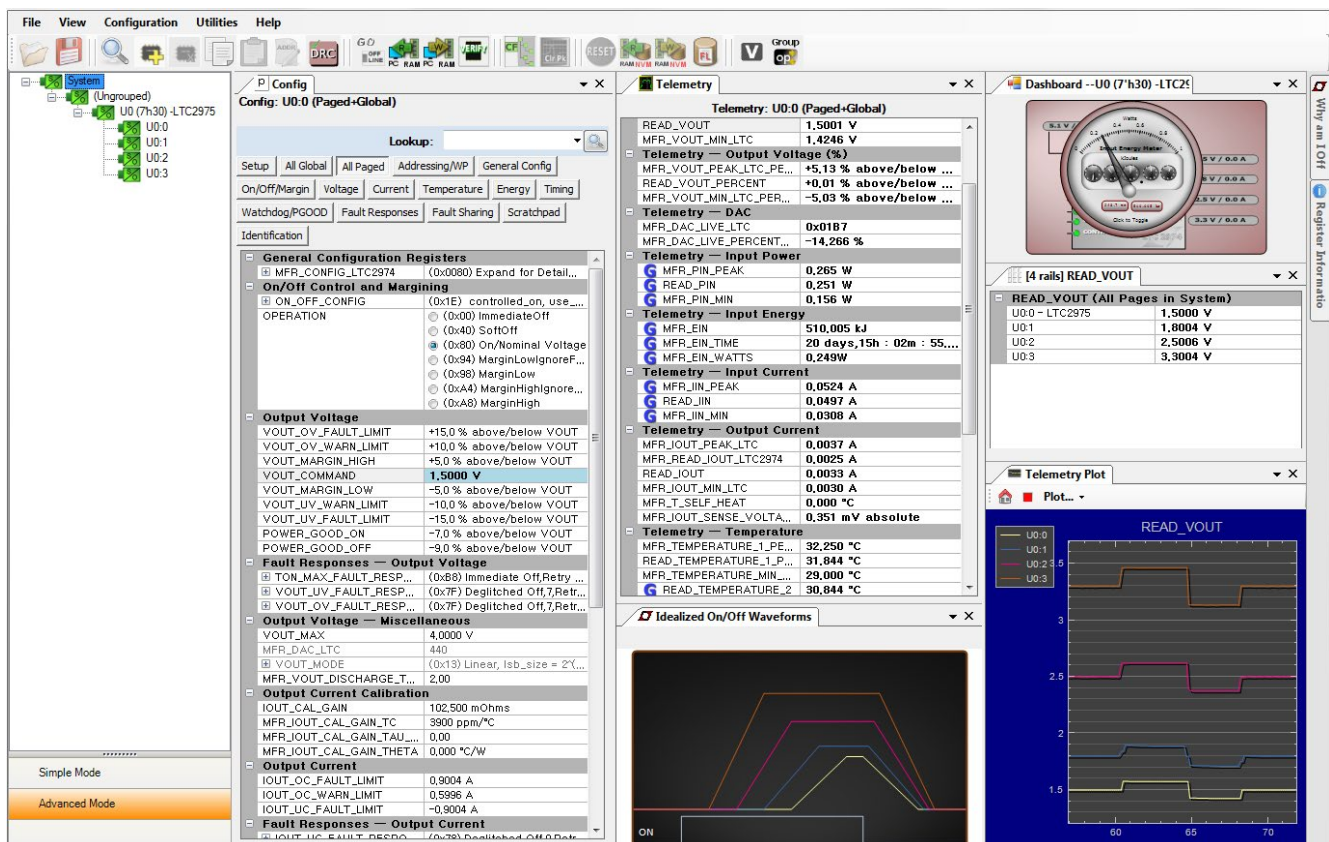


Figure 45. LTpowerPlay Snapshot

## APPLICATIONS INFORMATION

### PCB ASSEMBLY AND LAYOUT SUGGESTIONS

#### Bypass Capacitor Placement

The LTC2975 requires 0.1 $\mu$ F bypass capacitors between the  $V_{DD33}$  pins and GND, the  $V_{DD25}$  pin and GND, the REFP pin and REFM pin, and a 10nF capacitor between the VIN\_SNS\_CAP pin and GND. If the chip is being powered from the  $V_{PWR}$  input, then that pin should also be bypassed to GND by a 0.1 $\mu$ F capacitor. In order to be effective, these capacitors should be made of a high quality ceramic dielectric such as X5R or X7R and be placed as close to the chip as possible.

#### Exposed Pad Stencil Design

The LTC2975's package is thermally and electrically efficient. This is enabled by the exposed die attach pad on the under side of the package which must be soldered down to the PCB or mother board substrate. It is a good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination of voids is difficult, but the design of the exposed pad stencil is key. Figure 46 shows a suggested screen print pattern. The proposed stencil design enables out-gassing of the solder paste during reflow as well as regulating the finished solder thickness. See IPC7525A.

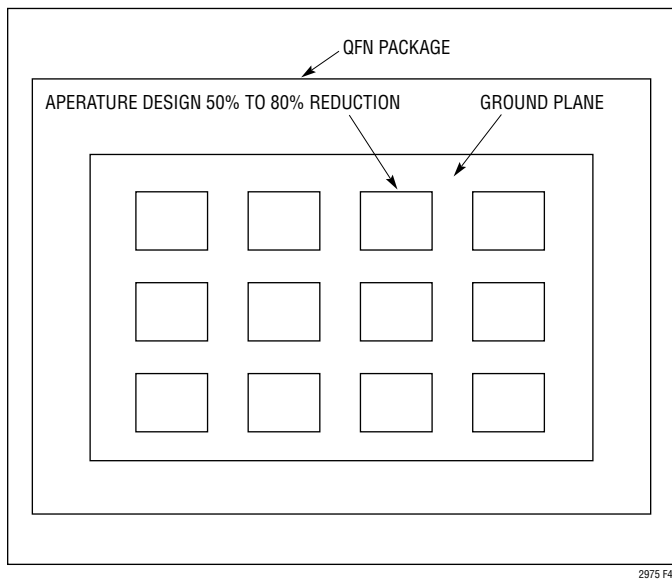


Figure 46. Suggested Screen Pattern for Die Attach Pad

#### PCB Board Layout

Mechanical stress on a PC board and soldering-induced stress can cause the LTC2975's reference voltage and the voltage drift to shift. A simple way to reduce the stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board acts as a stress boundary, or a region where the flexure of the board is minimal.

The LTC2975's READ\_IIN input current sense amplifier has very low offsets enabling accurate current, power, and energy readings. PC Board routing to current sense inputs may create a thermal voltage offset if differential routing paths cross dissimilar metal boundaries in the presence of a thermal gradient. To minimize thermal voltages, route differential current sense inputs as close together as possible, and minimize vias. If vias are necessary, make sure to place both positive and negative current sense path vias are close together to minimize the temperature difference.

#### Unused ADC Sense Inputs

Connect all unused ADC sense inputs ( $V_{SENSEPN}$ ,  $V_{SENSEMN}$ ,  $T_{SENSEn}$ ,  $I_{SENSEPN}$  or  $I_{SENSEMN}$ ) to GND. In a system where the inputs are connected to removable cards and may be left floating in certain situations, connect the inputs to GND using 100k resistors. Place the 100k resistors before any filter components, as shown in Figure 47, to prevent loading of the filter.

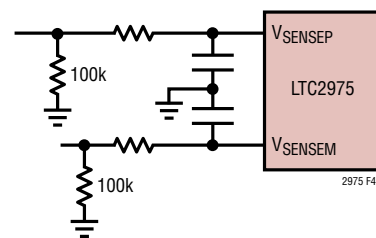


Figure 47. Connecting Unused Inputs to GND

## APPLICATIONS INFORMATION

### DESIGN CHECKLIST

#### I<sup>2</sup>C

- The LTC2975 must be configured for a unique address.
- The address select pins (ASEL<sub>n</sub>) are tri-level; Check Table 3.
- Check addresses for collision with other devices on the bus and any global addresses.

#### Output Enables

- Use appropriate pull-up resistors on all V<sub>OUT\_ENn</sub> pins.
- Verify that the absolute maximum ratings of the V<sub>OUT\_ENn</sub> pins are not exceeded.

#### V<sub>IN</sub> Sense

- No external resistive divider is required to sense V<sub>IN</sub>; V<sub>IN\_SNS</sub> already has an internal calibrated divider.

#### Input Current Sense

- Verify that I<sub>IN\_SNSP</sub> and I<sub>IN\_SNSM</sub> pins do not exceed absolute maximum ratings.
- Add a 10nF capacitor to VIN\_SNS\_CAP

#### External Temperature Sense

- Verify the PNP sense transistor is close to the inductor and away from other significant heat sources.
- Verify the PNP sense transistor emitter routes to the LTC2975, and the base and collector connect to signal ground near the LTC2975.

#### Logic Signals

- Verify the absolute maximum ratings of the digital pins (SCL, SDA, ALERTB, FAULTB<sub>n</sub>, CONTROL<sub>n</sub>, SHARE\_CLK, WDI, ASEL<sub>n</sub>, PWRGD) are not exceeded.
- Connect all SHARE\_CLK pins in the system together and pull up to 3.3V with a 5.49k resistor.
- Do not leave CONTROL<sub>n</sub> pins floating. Pull up to 3.3V with a 10k resistor.
- Tie WDI/RESETB to V<sub>DD33</sub> with a 10k resistor. Do not connect a capacitor to the WDI/RESETB pin.
- Tie WP to either V<sub>DD33</sub> or GND. Do not leave floating.

#### Unused Inputs

- Connect all unused V<sub>SENSEPN</sub>, V<sub>SENSEMn</sub>, I<sub>SENSEPN</sub>, I<sub>SENSEMn</sub>, and T<sub>SENSEn</sub> pins to GND. Do not float unused inputs. Refer to Unused ADC Sense Inputs in the Applications Information section.
- If not used, connect I<sub>IN\_SNSP</sub> and I<sub>IN\_SNSM</sub> pins to the V<sub>IN\_SNS</sub> pin.

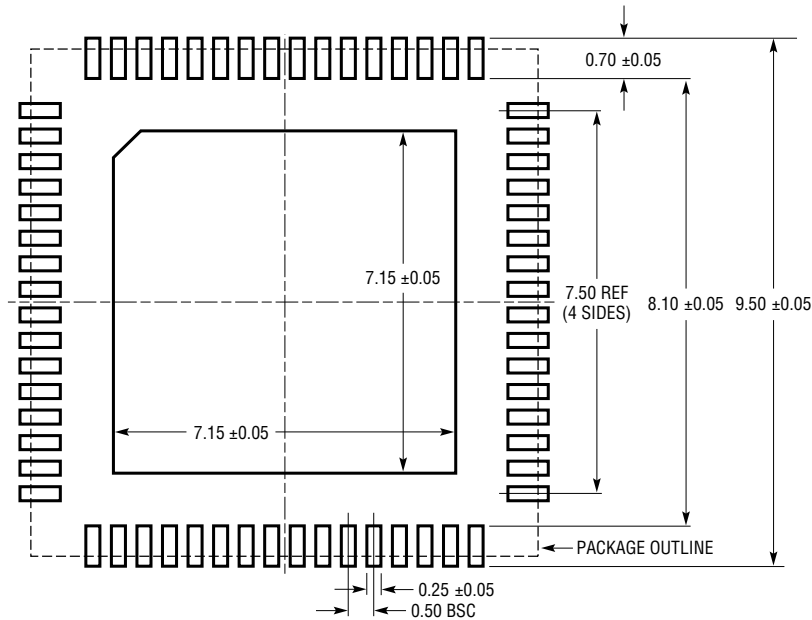
#### DAC Outputs

- Select appropriate resistor for desired margin range. Refer to the resistor selection tool in LTpowerPlay for assistance.

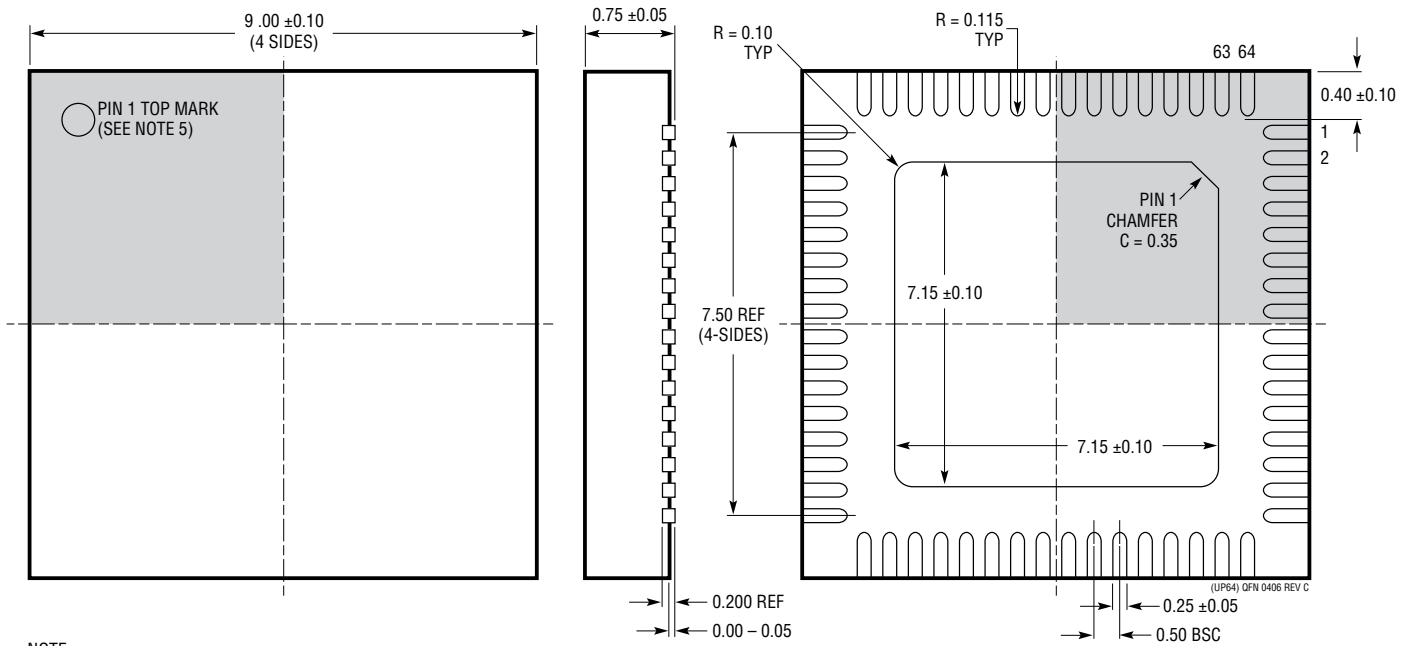
For a more complete list of design considerations and a schematic checklist, see the Design Checklist on the [LTC2975](#) product page.

**PACKAGE DESCRIPTION**

**UP Package**  
**64-Lead Plastic QFN (9mm × 9mm)**  
 (Reference LTC DWG # 05-08-1705 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



- NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
  4. EXPOSED PAD SHALL BE SOLDER PLATED
  5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
  6. DRAWING NOT TO SCALE

BOTTOM VIEW—EXPOSED PAD



## PACKAGE DESCRIPTION



PACKAGE ROW AND COLUMN LABELING MAY VARY  
AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE  
LAYOUT CAREFULLY.

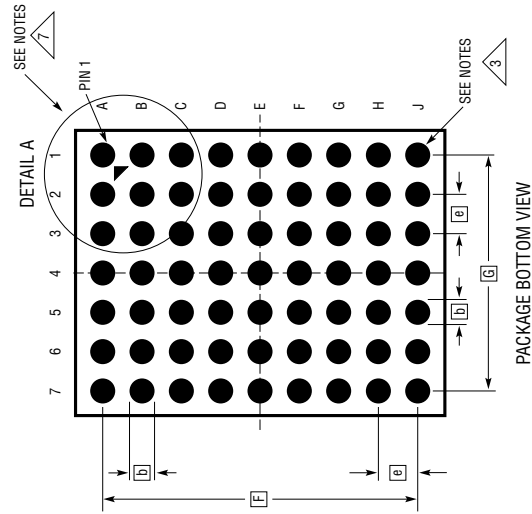
### LTC2975 Component BGA Pinout

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	V <sub>SENSEM1</sub>	B1	V <sub>SENSEM0</sub>	C1	V <sub>OUT_EN1</sub>	D1	V <sub>OUT_EN3</sub>	E1	DNC
A2	V <sub>SENSEP1</sub>	B2	V <sub>SENSEP0</sub>	C2	V <sub>OUT_EN0</sub>	D2	GND	E2	V <sub>IN_SNS</sub>
A3	V <sub>DAC3</sub>	B3	V <sub>SENSEP2</sub>	C3	V <sub>SENSEM2</sub>	D3	V <sub>OUT_EN2</sub>	E3	AUXFAULTB
A4	I <sub>IN_SNSM</sub>	B4	I <sub>IN_SNSP</sub>	C4	V <sub>DAC2</sub>	D4	GND	E4	GND
A5	V <sub>DAC0</sub>	B5	V <sub>DAC1</sub>	C5	GND	D5	I <sub>SENSEM0</sub>	E5	ASEL1
A6	V <sub>IN_SNS_CAP</sub>	B6	I <sub>SENSEM3</sub>	C6	I <sub>SENSEP3</sub>	D6	I <sub>SENSEM1</sub>	E6	I <sub>SENSEP0</sub>
A7	V <sub>SENSEM3</sub>	B7	V <sub>SENSEP3</sub>	C7	I <sub>SENSEM2</sub>	D7	I <sub>SENSEP2</sub>	E7	I <sub>SENSEP1</sub>

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
F1	V <sub>DD33</sub>	G1	V <sub>DD25</sub>	H1	V <sub>DD25</sub>	J1	PWRGD
F2	T <sub>SENSE0</sub>	G2	V <sub>PWR</sub>	H2	WDI/RESETB	J2	SHARE_CLK
F3	T <sub>SENSE1</sub>	G3	GND	H3	CONTROL2	J3	CONTROL3
F4	GND	G4	GND	H4	FAULTB0	J4	FAULTB1
F5	GND	G5	T <sub>SENSE2</sub>	H5	WP	J5	SDA
F6	REFP	G6	T <sub>SENSE3</sub>	H6	CONTROL1	J6	SCL
F7	REFM	G7	ASEL0	H7	CONTROL0	J7	ALERTB

# PACKAGE DESCRIPTION

**BGA Package**  
**63-Lead (7.5mm × 6.25mm × 1.52mm)**  
 (Reference LTC DWG # 05-08-1547 Rev 0)



NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

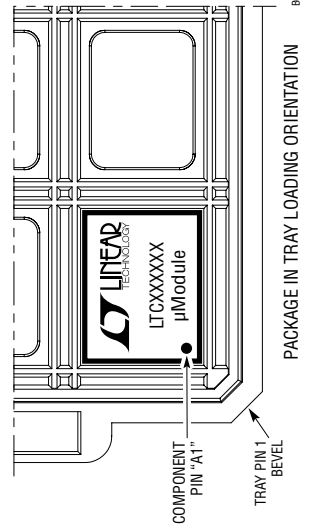
3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95

4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

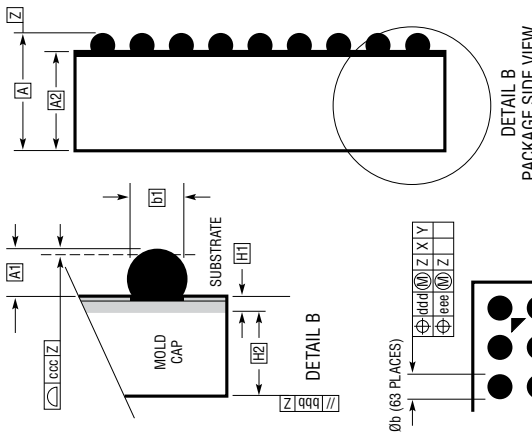
5. PRIMARY DATUM -Z- IS SEATING PLANE

6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu

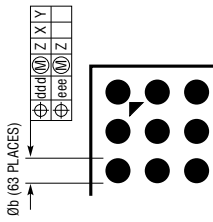
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG  $\mu$ Module PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



BGA 630516 REV 0

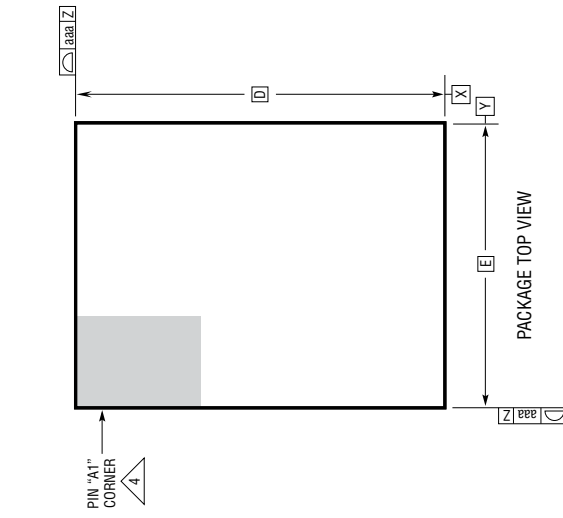


DETAIL B  
 PACKAGE SIDE VIEW

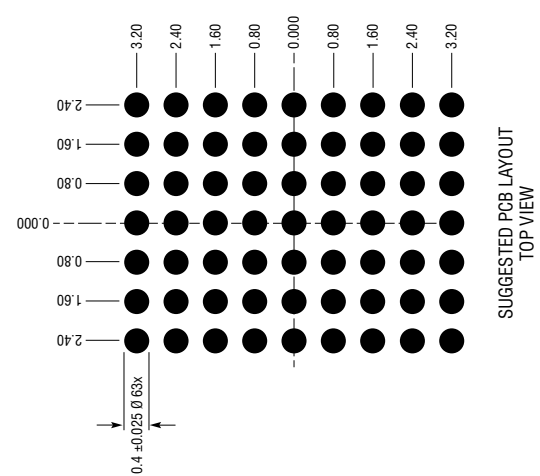


DETAIL A

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	1.32	1.52	1.72	
A1	0.30	0.40	0.50	
b	1.02	1.12	1.22	
b1	0.45	0.50	0.55	
D	0.37	0.40	0.43	
E		7.50		
e		6.25		
f		0.80		
F		6.40		
G		4.80		
H1	0.27	0.32	0.37	
H2	0.75	0.80	0.85	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 63				



PACKAGE TOP VIEW

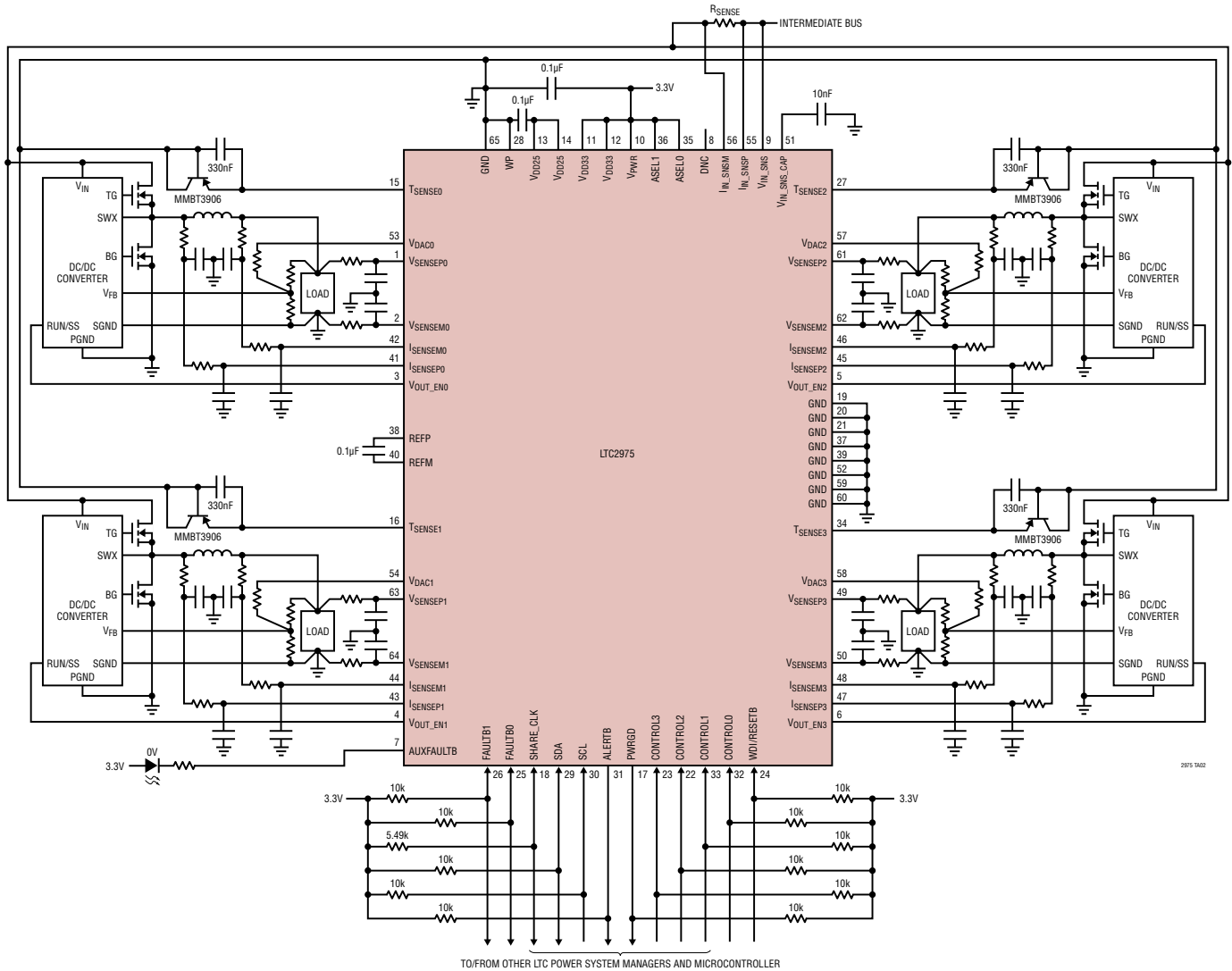


SUGGESTED PCB LAYOUT  
 TOP VIEW

## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/19	Updated Typical Application; added EEPROM ECC information.	1, 18, 19
		Updated DAC Output Update Rate ( $t_{S\_VDAC}$ ).	6
		Added $V_{VOUT\_VALID}$ specification.	8
		Added Note 3; Updated Note 5; Updated Note numbers.	9, 10
		Added graph: $V_{OUT\_EN[3:0]}$ Output Voltage vs $V_{DD33}$ .	14
		Updated $V_{DD33}$ and $V_{DD25}$ pin functions.	15
		Updated Figure 2.	22
		Updated READ_IIN, READ_PIN PAGED entries; added MFR_INFO.	26, 84
		Updated PAGED entries for MFR_IIN_PEAK, MFR_IIN_MIN, MFR_PIN_PEAK, MFR_PIN_MIN.	27
		Updated MFR_SPECIAL_ID value.	28, 84
		Added MFR_COMMAND_PLUS to Level 2 exception list; added write protection level table.	31
		Updated: b[1] symbol and operation for MFR_STATUS_PLUS $n$ registers.	33
		Updated: b[10] to reserved status, MFR_EE_DATA bits and symbol.	45, 48
		Updated: STATUS_WORD b[0], STATUS_VOUT b[3].	66, 67
Updated description: MFR_IIN_PEAK, MFR_IIN_MIN, MFR_PIN_PEAK, MFR_PIN_MIN, MFR_READ_IOUT, MFR_VIN_PEAK, MFR_VOUT_PEAK, MFR_IOUT_PEAK, MFR_TEMPERATURE_1_PEAK, MFR_VIN_MIN, MFR_VOUT_MIN, MFR_IOUT_MIN, MFR_TEMPERATURE_1_MIN.	72 to 75		
Updated section on Configuring the AUXFAULTB Output.	90		
Added BAT54 diode to Figure 31.	91		
Updated Design Checklist.	103		
B	02/20	Added BGA package option to Features bullets and Ordering Information table.	1, 4, 5
		Added TUE_IIN 0mV low range specification for BGA.	7
		Added BGA pin numbers to Pin Functions table.	15, 16
		Added BGA Package Description.	105, 106
C	04/21	Updated Typical Application .	1
		Updated $V_{DD33}$ and $V_{DD25}$ pin descriptions.	15
		Updated section on Processing Commands and associated command tables.	21
		Corrected MFR_PADS type from 'R/W Word' to 'R Word'.	28, 65
		Updated offset value in the example scenario in MFR_I2C_BASE_ADDRESS section.	32
		Updated text in Response When Part Is Busy section.	48
		Updated b[5] and b[6] Operation text in STATUS_MFR_SPECIFIC Data Contents table.	69
Updated ALERTB behavior described in MFR_COMMON section.	70		
Updated MFR_VOUT_MIN description.	74		
D	06/22	Added AEC-Q100 Qualification and 'W' part numbers.	1, 5
		Corrected Pin Functions table.	17

## TYPICAL APPLICATION



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC2970</a>	Dual I <sup>2</sup> C Power Supply Monitor and Margining Controller	5V to 15V, ±0.5% TUE 14-Bit ADC, 8-Bit DAC, Temperature Sensor
<a href="#">LTC2974</a>	4-Channel Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTC2977</a>	8-Channel Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
<a href="#">LTC2980</a>	16-Channel PMBus Power System Manager	Dual LTC2977
<a href="#">LTM2987</a>	16-Channel μModule PMBus Power System Manager	Dual LTC2977 with Integrated Passive Components
<a href="#">LTC3880</a>	Dual Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTC3883</a>	Single Output PolyPhase Step-Down DC/DC Controller	0.5% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
<a href="#">LTM4676</a>	Dual 13A or Single 26A μModule Regulator with Digital Power System Management	1% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision

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