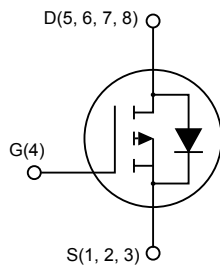
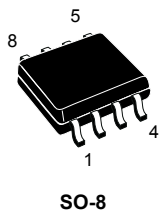


P-channel 30 V, 24 mΩ typ., 6 A, STripFET H6 Power MOSFET in an SO-8 package



AM01475v4

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STS6P3LLH6	30 V	30 mΩ	6 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.



Product status link

[STS6P3LLH6](#)

Product summary

Order code	STS6P3LLH6
Marking	6K3L
Package	SO-8
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	6	A
	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	4	
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total power dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.7	W
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	47	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10\text{ s}$.

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			10	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$		24	30	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 3\text{ A}$		38	50	

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 24\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1450	-	pF
C_{oss}	Output capacitance		-	178	-	pF
C_{rSS}	Reverse transfer capacitance		-	120	-	pF
Q_g	Total gate charge	$V_{DD} = 24\text{ V}$, $I_D = 6\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 13. Gate charge test circuit)	-	12	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	nC
Q_{gd}	Gate-drain charge		-	5	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Switching times test circuit for resistive load)	-	24	-	ns
t_f	Fall time		-	21	-	ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	15		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 16\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	6.5		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	0.9		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

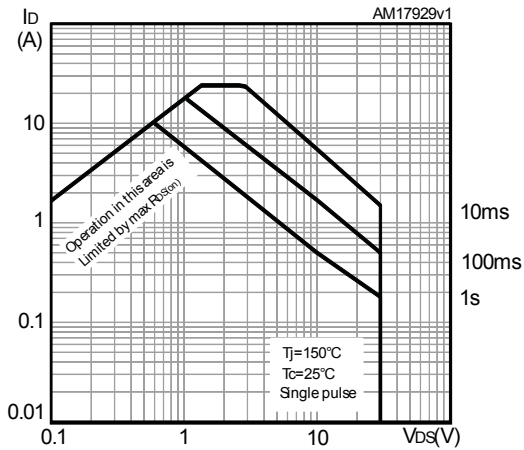


Figure 2. Thermal impedance

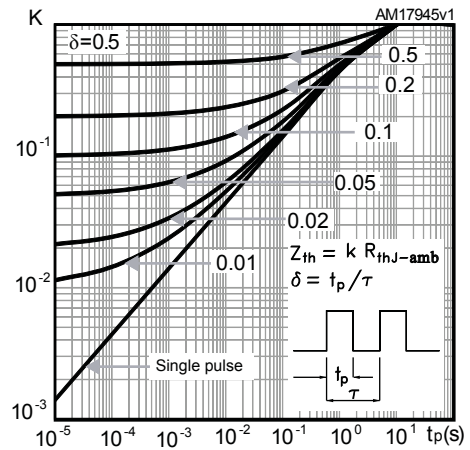


Figure 3. Output characteristics

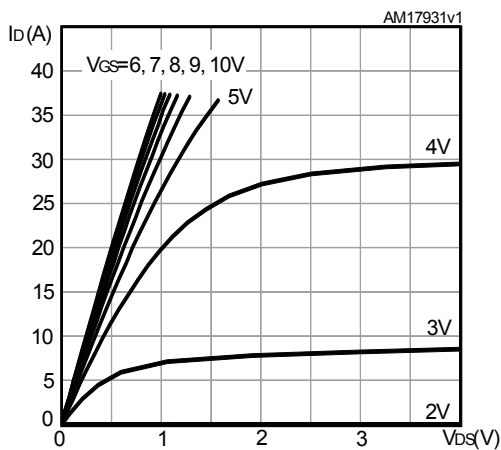


Figure 4. Transfer characteristics

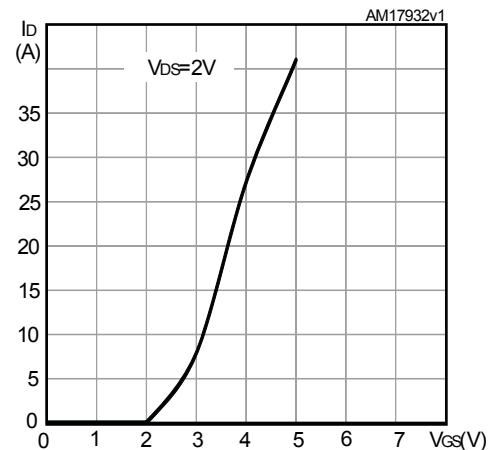


Figure 5. Gate charge vs gate-source voltage

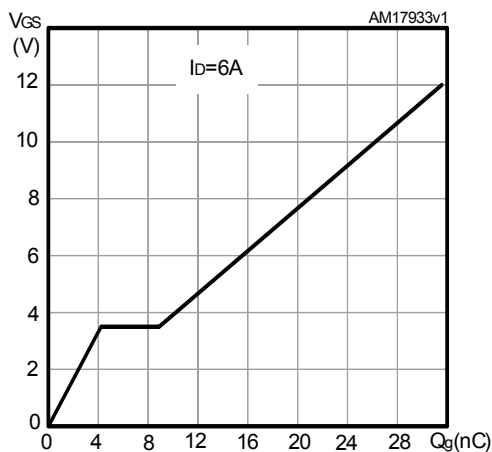


Figure 6. Static drain-source on-resistance

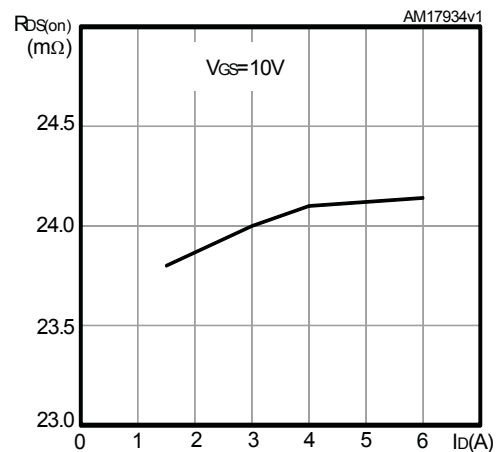


Figure 7. Capacitance variations

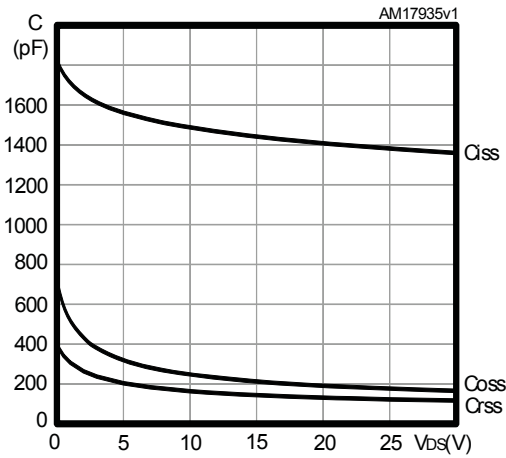


Figure 8. Normalized gate threshold voltage vs temperature

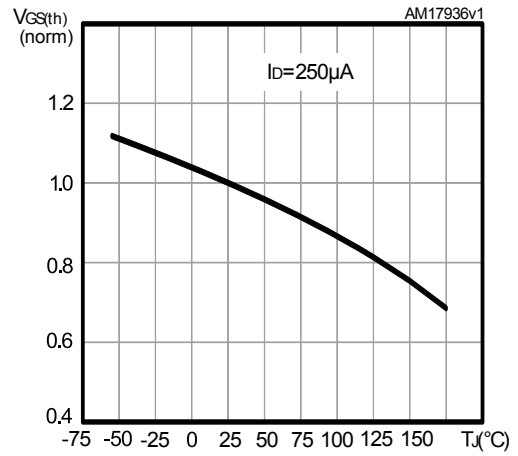


Figure 9. Normalized on-resistance vs temperature

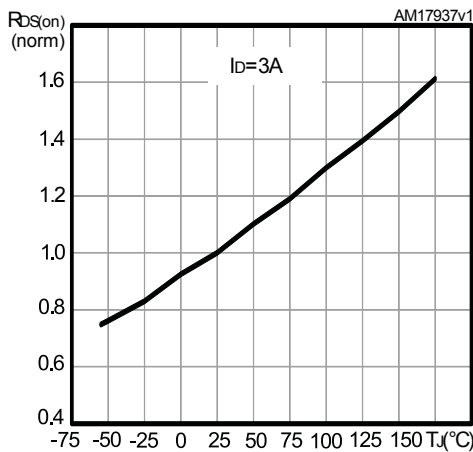


Figure 10. Normalized V_{DS} vs temperature

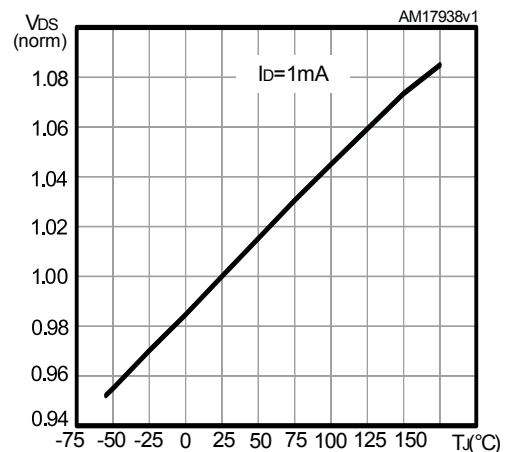
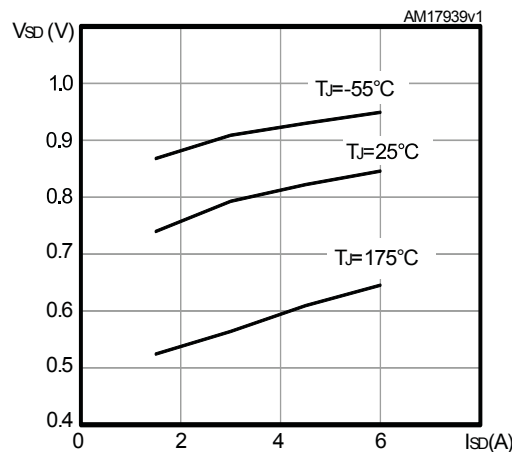


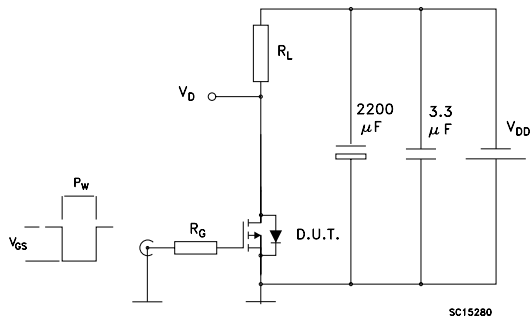
Figure 11. Source-drain diode forward characteristics



Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

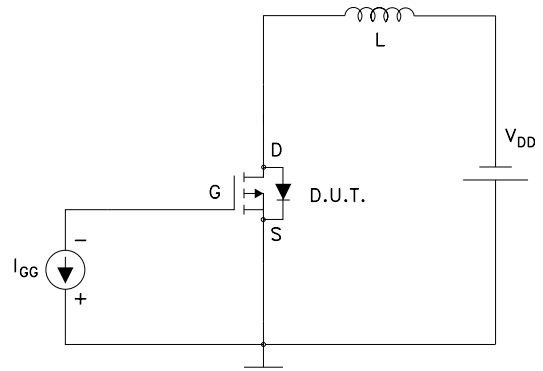
3 Test circuits

Figure 12. Switching times test circuit for resistive load



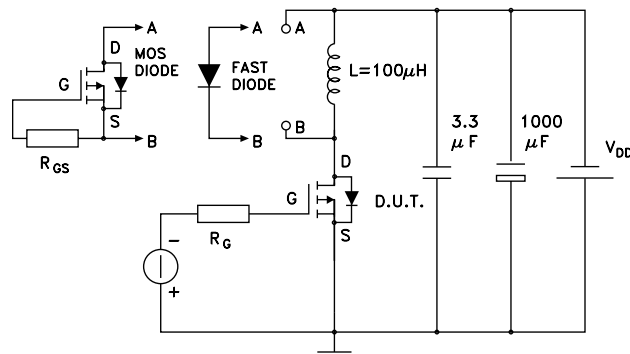
SC15280

Figure 13. Gate charge test circuit



SC15290

Figure 14. Test circuit for inductive load switching and diode recovery times



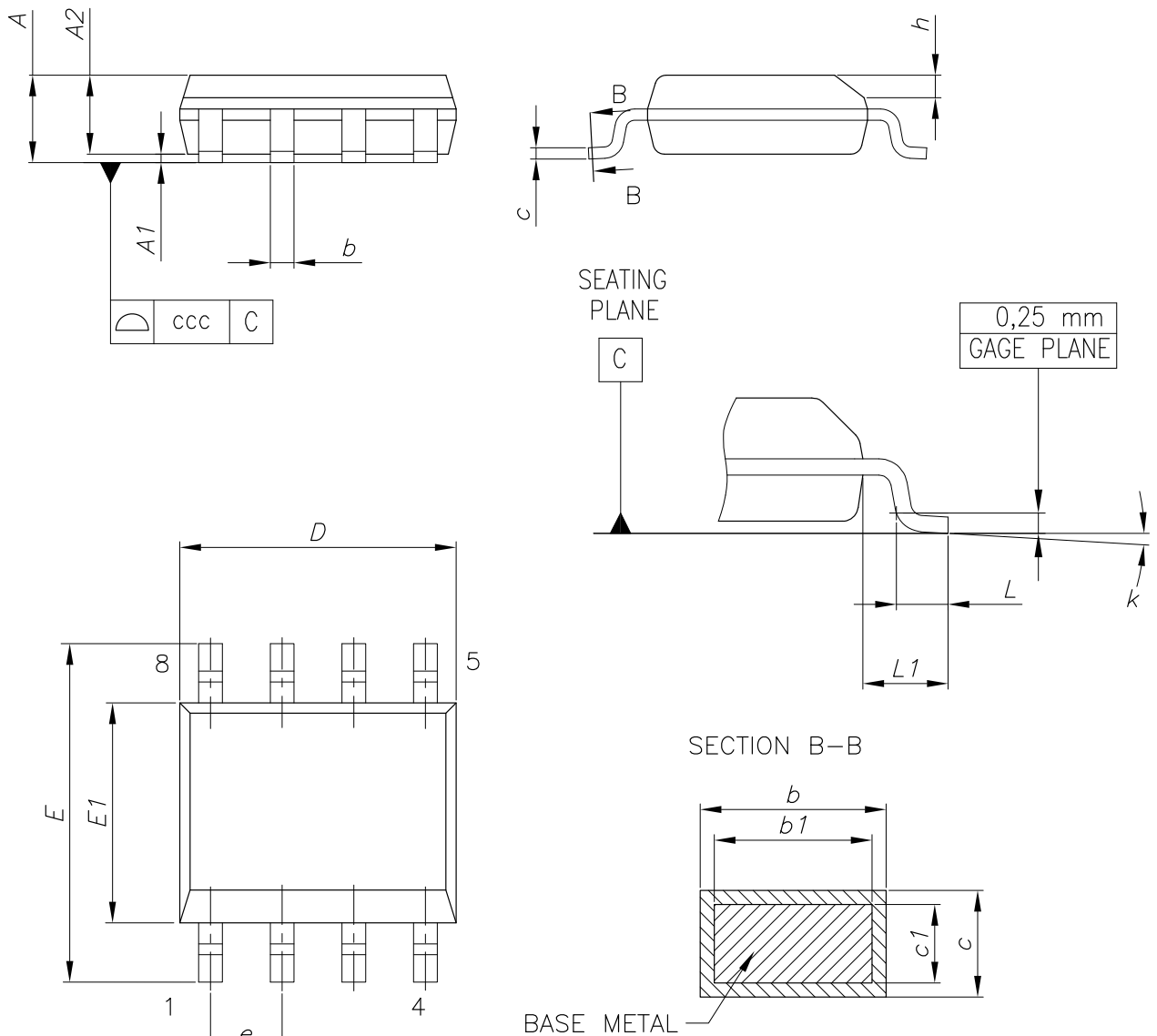
SC15300

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 15. SO-8 package outline

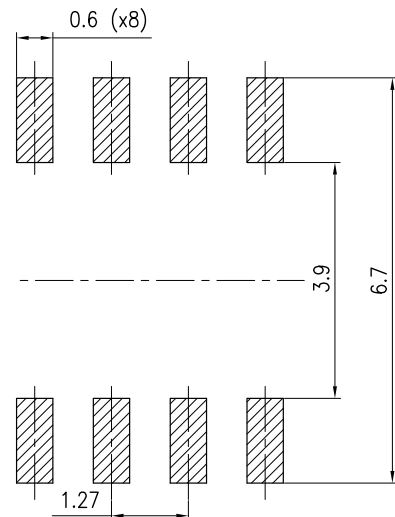


0016023_So-807_fig2_Rev10

Table 7. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 16. SO-8 recommended footprint (dimensions are in mm)



0016023_So-807_footprint_Rev10

4.2 SO-8 packing information

Figure 17. SO-8 tape and reel dimensions

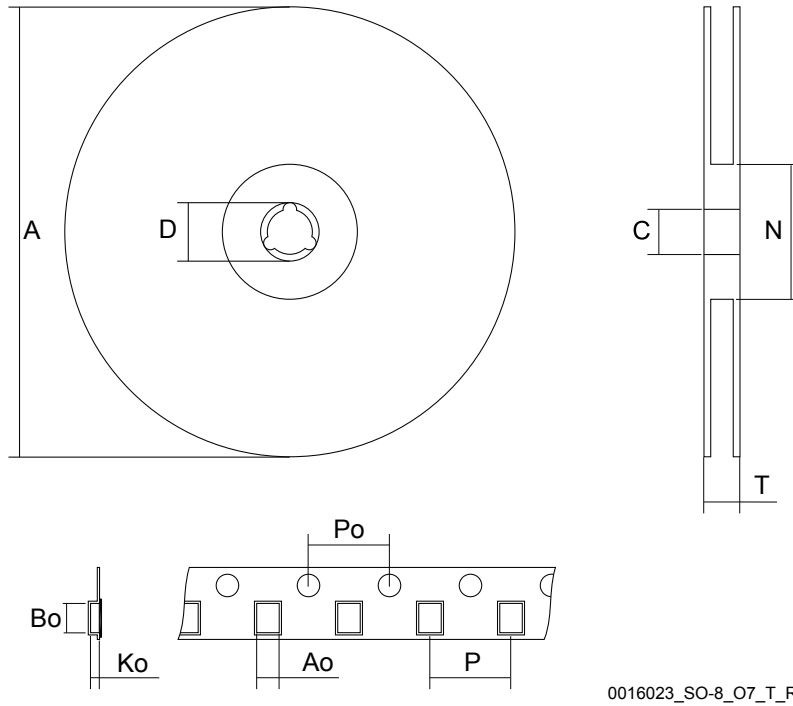


Figure 18. Tape orientation

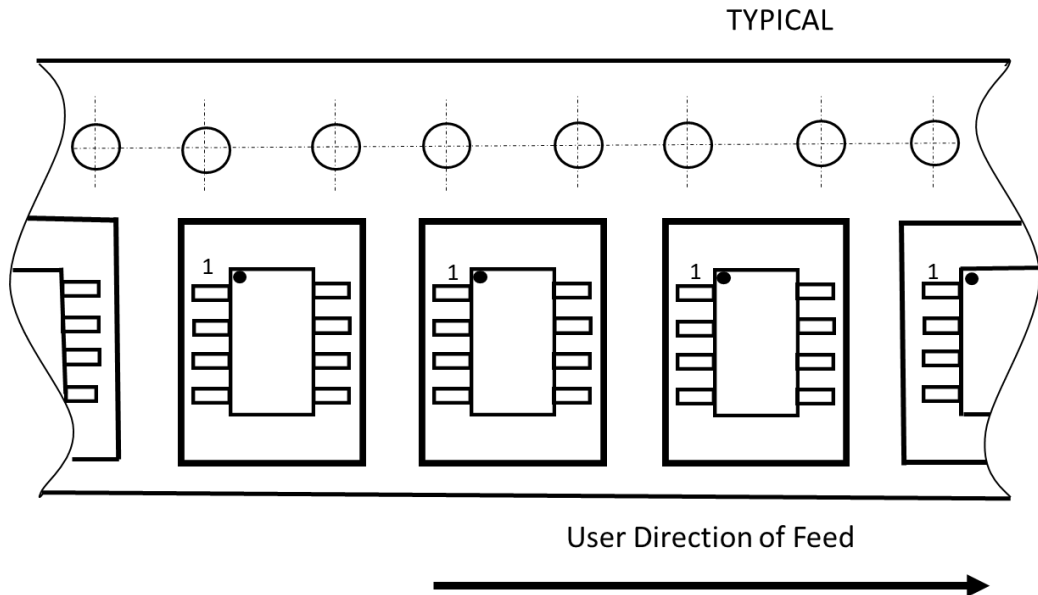


Table 8. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5	-	6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 9. Document revision history

Date	Version	Changes
01-Feb-2013	1	First revision.
28-Nov-2013	2	<ul style="list-style-type: none"> – Modified: $R_{DS(on)}$ value in cover page – Modified: V_{GS} value in <i>Table 2</i> – Modified: I_{GSS} test conditions value in <i>Table 4</i> – Modified: Q_g typical value in <i>Table 5</i> – Added: <i>Section 2.1: Electrical characteristics (curves)</i> – Minor text changes.
17-Feb-2021	3	<p>Updated title and Internal schematic in cover page.</p> <p>Updated Section 4.2 SO-8 packing information.</p> <p>Minor text changes.</p>

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