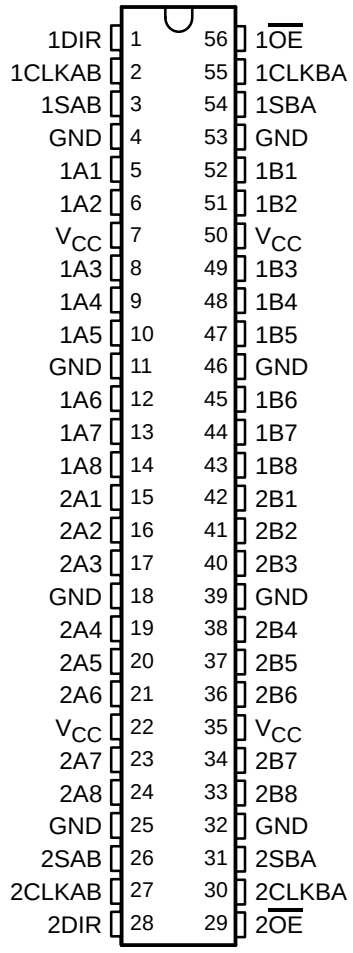
- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 5.7 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16646A can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16646A.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVC16646ADL	LVC16646A
		Tape and reel	SN74LVC16646ADLR	
	TSSOP – DGG	Tape and reel	SN74LVC16646ADGGR	LVC16646A
	TVSOP – DGV	Tape and reel	SN74LVC16646ADGVR	LD646A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

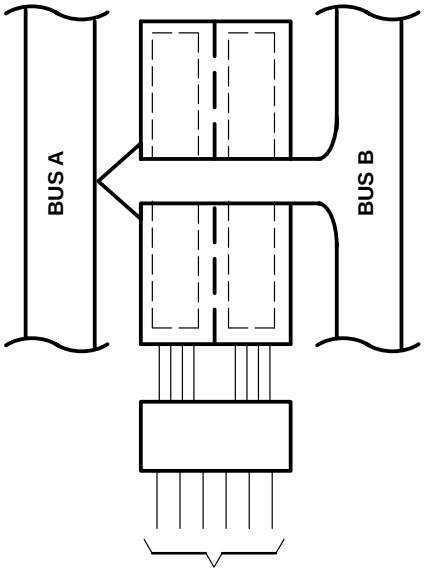
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

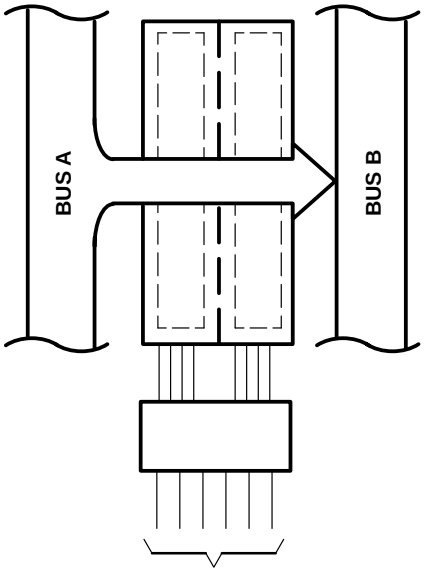
INPUTS						DATA I/O†		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

† The data-output functions can be enabled or disabled by various signals at $\overline{OE}$ or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



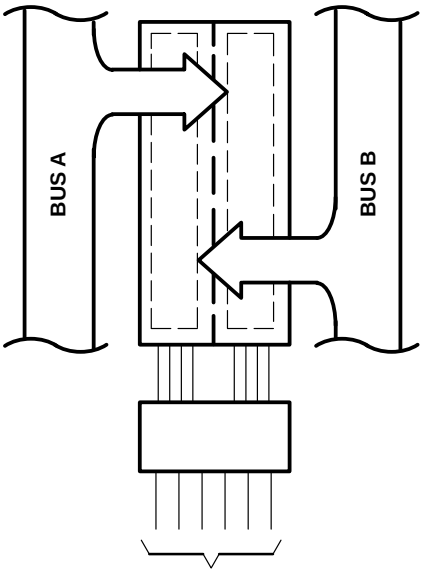
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



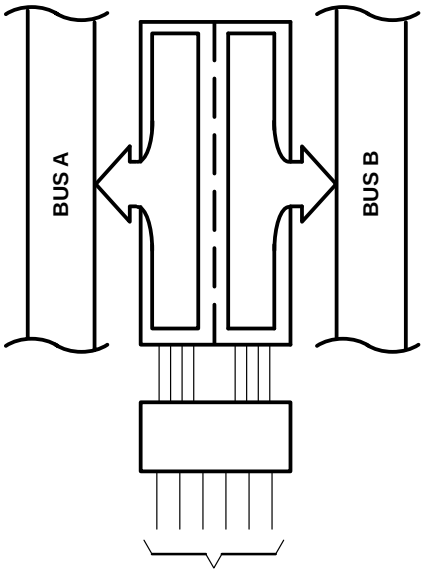
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

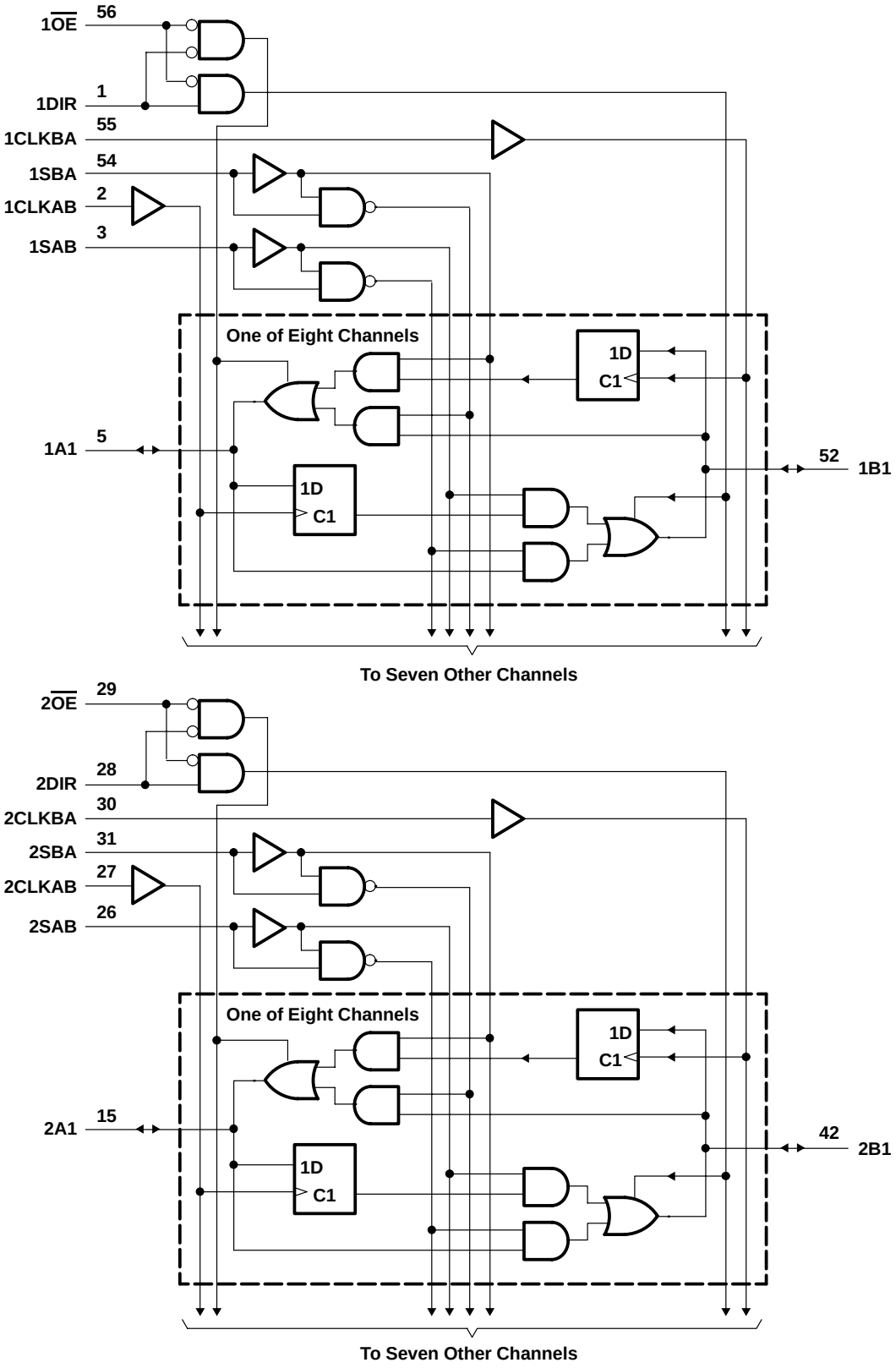


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 64°C/W
DGV package . . . . . 48°C/W
DL package . . . . . 56°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		1.65 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.7			
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2.2			
V_{OL}		I_{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.7	
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±5	μA
I_{off}		V_I or V_O = 5.5 V		0			±10	μA
I_{OZ}‡		V_O = 0 to 5.5 V		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			20	μA
		3.6 V ≤ V_I ≤ 5.5 V§					20	
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		5		pF
C_{io}	A or B ports	V_O = V_{CC} or GND		3.3 V		8.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current, but not $I_{I(hold)}$.
§ This applies in the disabled state only.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		85		125		150		150	MHz
t_w	Pulse duration, CLK high or low	5		4		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	6.5		4		3.2		2.9		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	0		0		0		0.3		ns

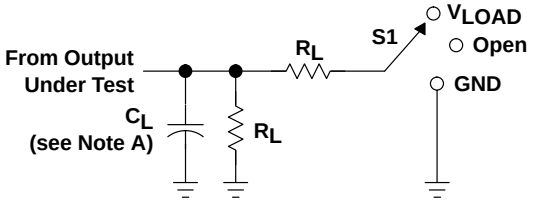
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			85		125		150		150		MHz
t_{pd}	A or B	B or A		11.3		7.8		6.8	0.5	5.7	ns
	CLKAB or CLKBA	A or B		12.4		8.9		7.9	1.8	6.7	
	SAB or SBA			13.5		10		9.2	1.7	7.7	
t_{en}	$\overline{OE}$	A or B		13		9.5		8.5	1.3	6.9	ns
t_{dis}				12		8.5		7.7	2.1	6.9	
t_{en}	DIR	A or B		13		9.5		8.5	1.4	7.2	ns
t_{dis}				12		8.5		7.8	2	7	

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	f = 10 MHz	53	55	60	pF
		Outputs disabled		9	10	12	

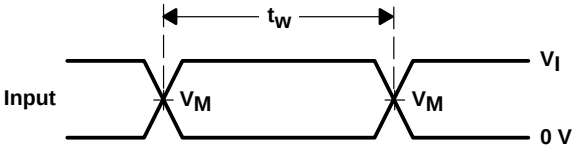
PARAMETER MEASUREMENT INFORMATION



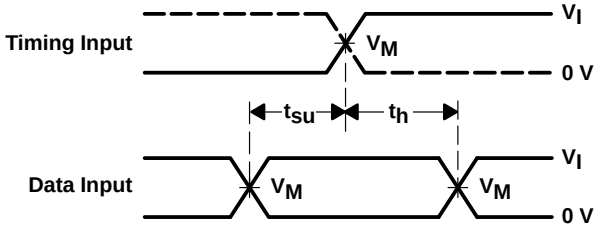
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

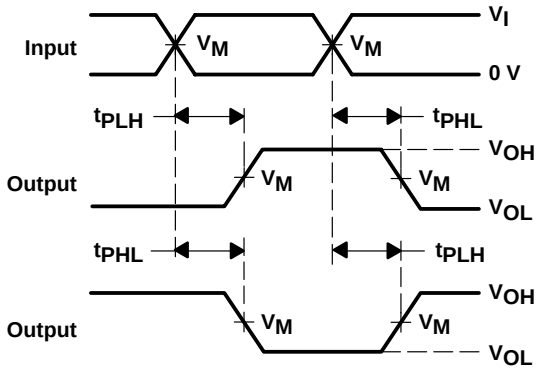
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



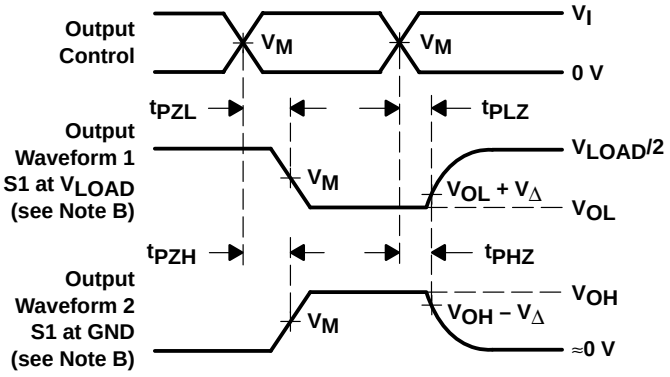
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



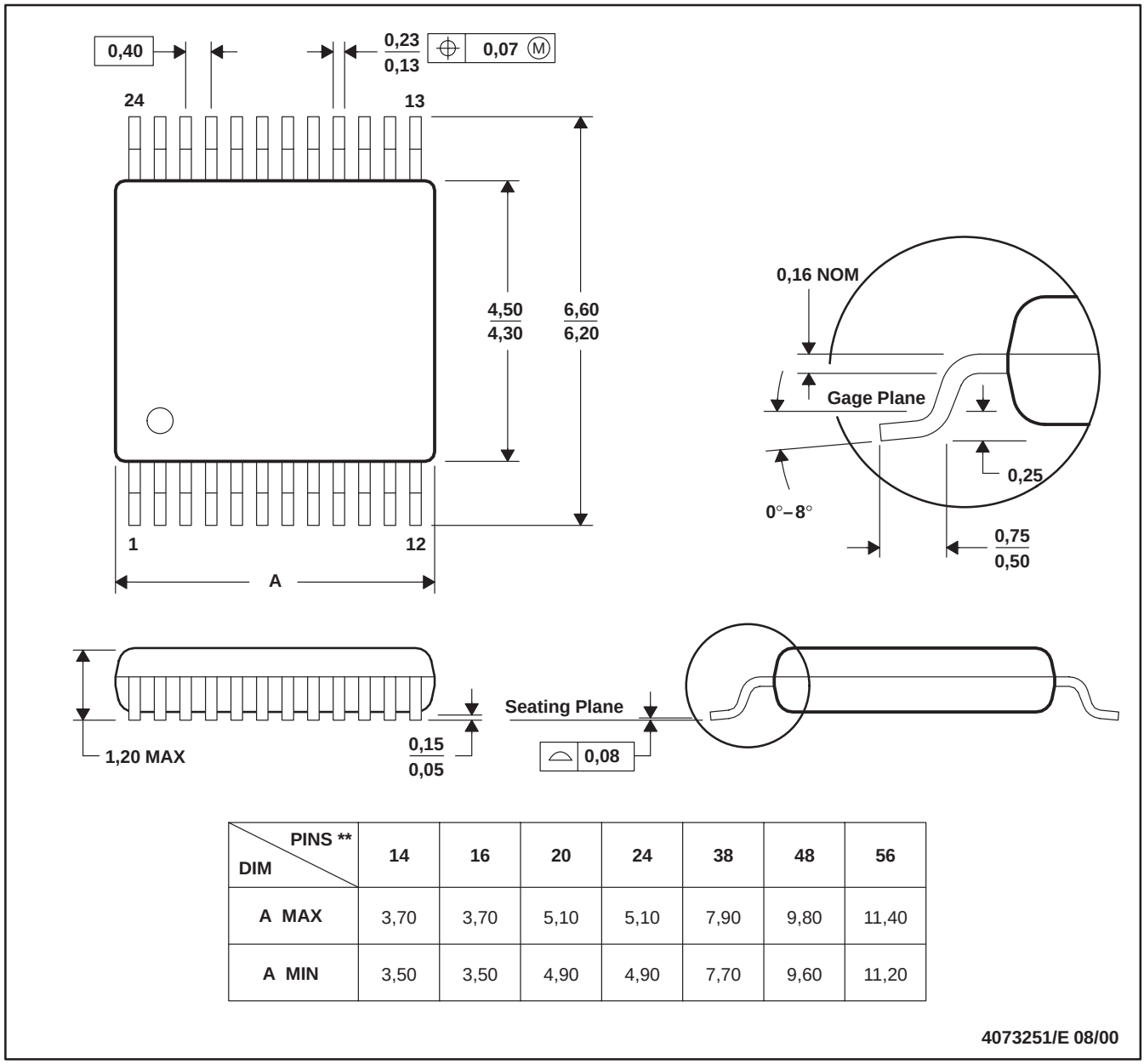
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

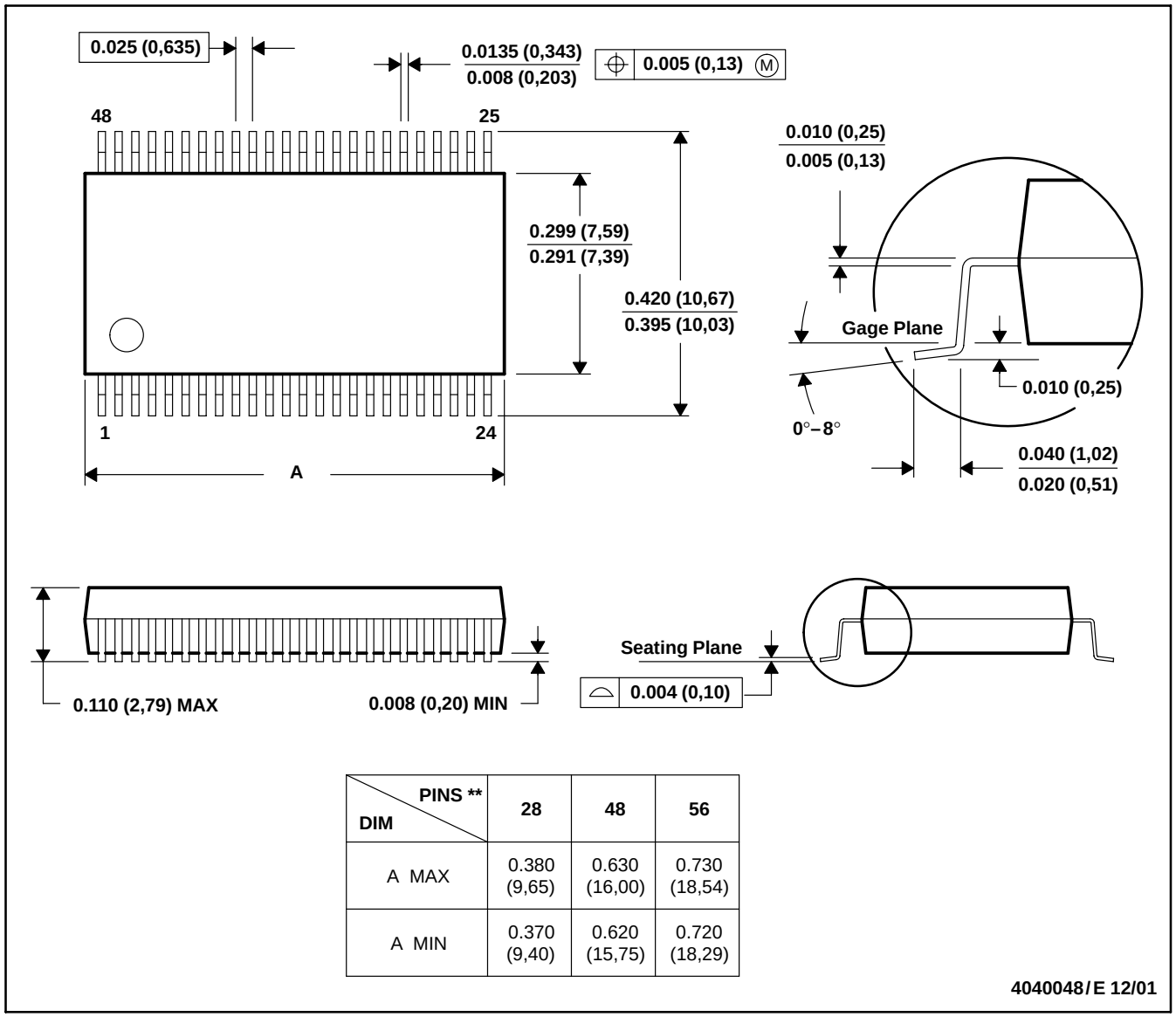
4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



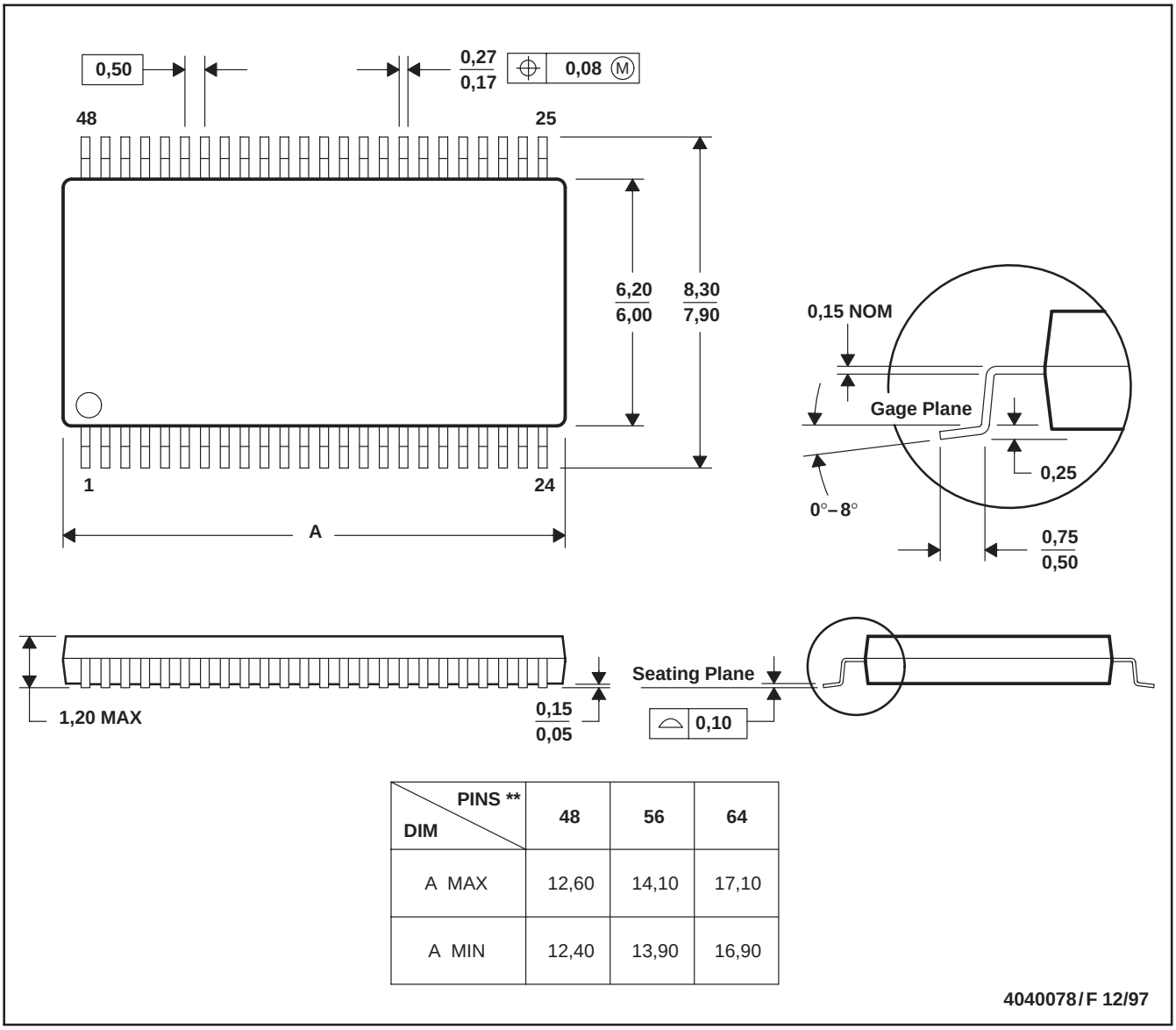
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

SN74LVC16646A, 16-Bit Bus Transceiver And Register With 3-State Outputs
DEVICE STATUS: **ACTIVE**

PARAMETER NAME	LVC16646A-1.8V	LVC16646A-2.5V	LVC16646A-2.7V	LVC16646A-3.3V
Voltage Nodes (V)	1.8	2.5	2.7	3.3
Vcc range (V)	1.65 to 3.6	1.65 to 3.6	1.65 to 3.6	1.65 to 3.6
Output Drive (mA)	-4/4	-8/8	-12/12	-24/24
No. of Outputs	16	16	16	16
Logic	True	True	True	True
Static Current	20 uA	20 uA	20 uA	20 uA
th (ns)	0	0	0	0.3
tpd max (ns)	11.3	7.8	6.8	5.7
tsu (ns)	6.5	4	3.3	3.3

FEATURES

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- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.7 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce)
  <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
  >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

DESCRIPTION

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This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVC16646A can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVC16646A.

Output-enable (OE)\ and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during

the transition between stored and real-time data. DIR determines which bus receives data when OE\ is low. In the isolation mode (OE\ high), A data can be stored in one register and/or B data can be stored in the other register.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74lvc16646a.pdf (205 KB,Rev.A) (Updated: 08/14/2002)

APPLICATION NOTES

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View Application Notes for Digital Logic

- 16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) (SZZA029B - Updated: 05/22/2002)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVC Characterization Information (SCBA011 - Updated: 12/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Low Voltage Logic Families (Rev. A) (SCVAE01A - Updated: 06/01/1998)
- Migration From 3.3-V To 2.5-V Power Supplies For Logic Devices (SCEA005 - Updated: 12/01/1997)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Selecting the Right Texas Instruments Signal Switch (SZZA030 - Updated: 09/07/2001)
- TI IBIS File Creation, Validation, and Distribution Processes (SZZA034 - Updated: 08/29/2002)
- Texas Instruments Little Logic Application Report (SCEA029 - Updated: 11/01/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)
- Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh (Rev. A) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- Enhanced Plastic Portfolio Brochure (SGZB004, 387 KB - Updated: 08/19/2002)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Military Low Voltage Solutions (SGYN139, 103 KB - Updated: 04/04/2001)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- Palladium Lead Finish User's Manual (SDYV001, 2041 KB - Updated: 11/01/1996)
- QML Class V Space Products Military Brief (Rev. A) (SGZN001A, 257 KB - Updated: 10/07/2002)
- STANDARD LINEAR AND LOGIC FOR DVD/VCD PLAYERS (SCYM001, 5872 KB - Updated: 03/27/2002)
- Standard Linear & Logic for PCs, Servers & Motherboards (SCYB005, 3997 KB - Updated: 06/13/2002)

USER GUIDES

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- 5-pin NanoStar(TM) Design Summary (Rev. A) (SCET006A, 934 KB - Updated: 11/20/2001)
- LOGIC Pocket Data Book (SCYD013, 4837 KB - Updated: 12/05/2002)
- LVC and LV Low-Voltage CMOS Logic Data Book (Rev. B) (SCBD152B, 13291 KB - Updated: 12/18/2002)

Product Folder: SN74LVC16646A, 16-Bit Bus Transceiver And Register With 3-State Outputs

- Low-Voltage Logic (LVC) Designer's Guide (SCBA010 - Updated: 09/01/1996)
- Signal Switch Data Book (SCDD003, 10259 KB - Updated: 03/19/2001)

SAMPLES Back to Top

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74LVC16646ADGGR	TSSOP (DGG)	56	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74LVC16646ADGVR	TVSOP (DGV)	56	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74LVC16646ADLR	SSOP (DL)	56	-40 TO 85	ACTIVE	View Product Content	Request Samples

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DEVICE INFORMATION
Updated Daily

ORDERABLE DEVICE	STATUS	PACKAGE TYPE | PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY
SN74LVC16646ADGG	PREVIEW	TSSOP (DGG) | 56	-40 TO 85	View Contents	1KU |	
SN74LVC16646ADGGR	ACTIVE	TSSOP (DGG) | 56	-40 TO 85	View Contents	1KU | 2.64	2000
SN74LVC16646ADGVR	ACTIVE	TVSOP (DGV) | 56	-40 TO 85	View Contents	1KU | 2.64	2000
SN74LVC16646ADL	ACTIVE	SSOP (DL) | 56	-40 TO 85	View Contents	1KU | 2.64	20
SN74LVC16646ADLR	ACTIVE	SSOP (DL) | 56	-40 TO 85	View Contents	1KU | 2.64	1000

TI INVENTORY STATUS
As Of 09:00 AM GMT, 17 Apr 2003

IN STOCK	IN PROGRESS QTY | DATE	LEAD TIME
0*		Call**
0*	1176 | 21 Apr	6 WKS
	>10k | 08 May	
0*	1055 | 21 Apr	6 WKS
	>10k | 08 May	
0*	>10k | 12 May	6 WKS
2000*	581 | 21 Apr	6 WKS
	>10k | 12 May	

REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

DISTRIBUTOR COMPANY | REGION	IN STOCK	PURCHASE
None Reported View Distributors		
DigiKey | Americas	>1k	BUY NOW
DigiKey | Americas	>1k	BUY NOW
None Reported View Distributors		
DigiKey | Americas	940	BUY NOW

MODELS Back to Top

- IBIS Model of SN74LVC16646A (SCEM276, 300 KB - Updated: 09/09/2002)
  IBIS Model of SN74LVC16646A (SCEM276, 43 KB, ZIP - Updated: 09/09/2002)

Table Data Updated on: 4/17/2003