



# ST2329A

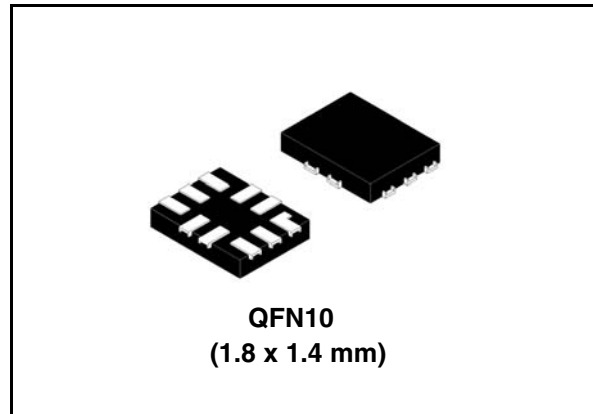
## 2-bit dual supply level translator without direction control pin

### Features

- 18 Mbps (max) data rate when driven by a totem pole driver
- 6.8 Mbps (max) data rate when driven by an open drain pole driver
- Bidirectional level translation without direction control pin
- Wide  $V_L$  voltage range of 1.65 to 3.6 V
- Wide  $V_{CC}$  voltage range of 1.80 to 5.5 V
- Power down mode feature – when either supply is off, all I/Os are in high impedance
- Low quiescent current (max 4  $\mu$ A)
- Able to be driven by totem pole and open drain drivers
- 5.5 V tolerant enable pin
- ESD performance on all pins:  $\pm 2$  kV HBM
- Small package and footprint:  
QFN10L (1.8 x 1.4 mm) package

### Applications

- Low voltage system level translation
- Mobile phones and other mobile devices
- I<sup>2</sup>C level translation
- UART level translation



### Description

The ST2329A is a 2-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic levels on either side of the device. It utilizes transmission gate-based design that allows bidirectional level translation without a control pin.

The ST2329A accepts a  $V_L$  from 1.65 to 3.6 V and  $V_{CC}$  from 1.80 to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all I/Os.

The ST2329A supports power down mode when  $V_{CC}$  is grounded/floating and the device is disabled via the OE pin.

Table 1. Device summary

Order code	Package	Packaging
ST2329AQTR	QFN10 (1.8 x 1.4 mm)	Tape and reel (3000 parts per reel)

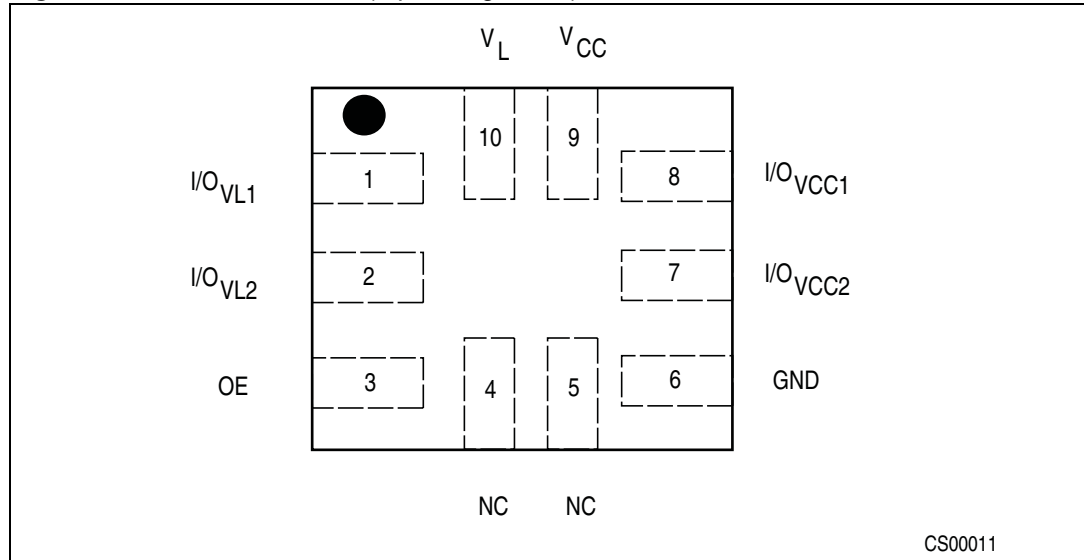
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# 1 Pin settings

## 1.1 Pin connection

Figure 1. Pin connection (top through view)



## 1.2 Pin description

Table 2. Pin description

Pin number	Symbol	Name and function
1	I/O <sub>VL1</sub>	Data input/output
2	I/O <sub>VL2</sub>	Data input/output
3	OE	Output enable
4	NC	No connection
5	NC	No connection
6	GND	Ground
7	I/O <sub>VCC2</sub>	Data input/output
8	I/O <sub>VCC1</sub>	Data input/output
9	V <sub>CC</sub>	Supply voltage
10	V <sub>L</sub>	Supply voltage

## 2 Device block diagrams

Figure 2. ST2329A block diagram

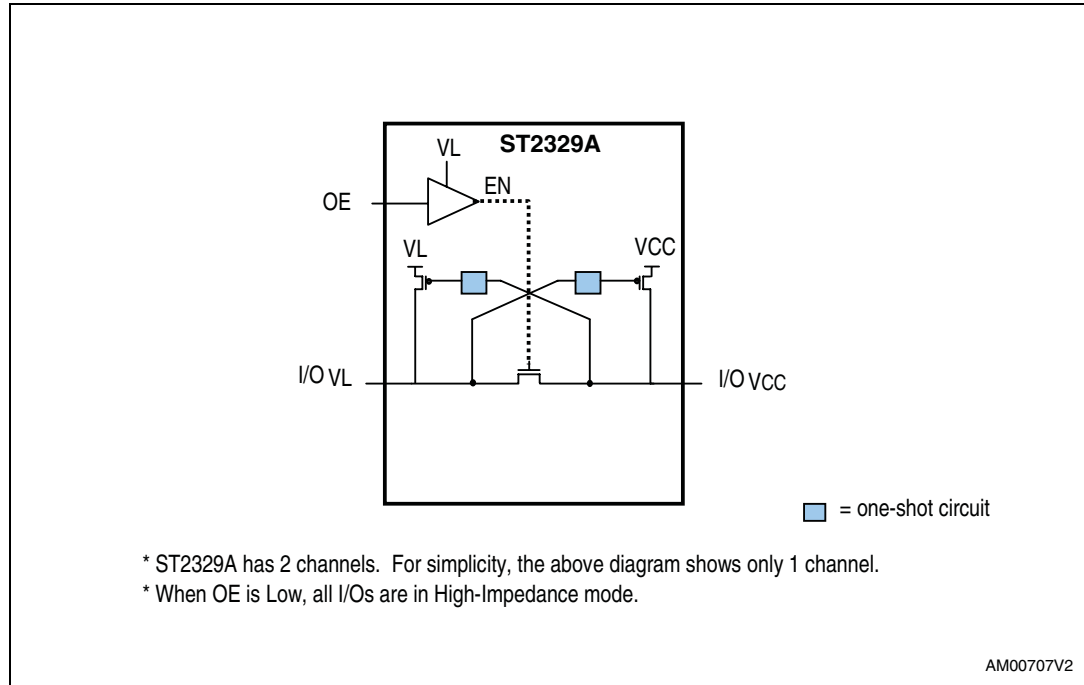
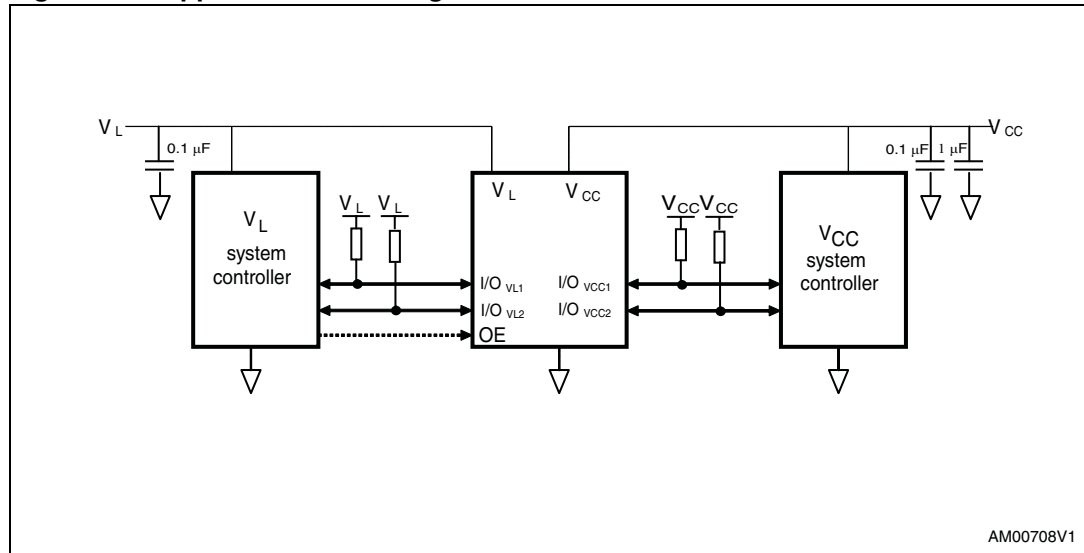


Figure 3. Application block diagram



## 3 Supplementary notes

### 3.1 Driver requirement

The ST2329A may be driven by an open drain or totem pole driver and the nature of the device's output is "open drain". It must not be used to drive a pull-down resistor since the impedance of the output at HIGH state depends on the pull-up resistor placed at the I/Os.

As the device has pull-up resistors on both the  $I/O_{VCC}$  and  $I/O_{VL}$  ports, the user needs to ensure that the driver is able to sink the required amount of current. For example, if the settings are  $V_{CC} = 5.5\text{ V}$ ,  $V_L = 4.3\text{ V}$  and the pull-up resistor is  $10\text{ k}\Omega$  then the driver must be able to sink at least  $(5.5\text{ V}/10\text{ k}\Omega) + (4.3\text{ V}/10\text{ k}\Omega) = 1\text{ mA}$  and still meet the  $V_{IL}$  requirements of the ST2329A.

### 3.2 Load driving capability

To support the open drain system, the one-shot transistor is turned on only during high transition at the output side. When it drives a high state, after the one-shot transistor is turned off, only the pull-up resistor is able to maintain the state. In this case, the resistive load is not recommended.

### 3.3 Power off feature

In some applications where it might be required to turn off one of the power supplies powering up the level translator, the user may turn off the  $V_{CC}$  only when the OE pin is low (device is disabled). There will be no current consumption in  $V_L$  due to floating gates or other causes, and the I/Os are in a high-impedance state in this mode.

### 3.4 Truth table

Table 3. Truth table

Enable	Bidirectional Input/Output	
OE	$I/O_{VCC}$	$I/O_{VL}$
H <sup>(1)</sup>	H <sup>(2)</sup>	H <sup>(1)</sup>
H <sup>(1)</sup>	L	L
L	Z <sup>(3)</sup>	Z <sup>(3)</sup>

1. High level  $V_L$  power supply referred
2. High level  $V_{CC}$  power supply referred
3. Z = high impedance

## 4 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_L$	Supply voltage	-0.3 to 4.6	V
$V_{CC}$	Supply voltage	-0.3 to 6.5	V
$V_{OE}$	DC control input voltage	-0.3 to 6.5	V
$V_{I/OVL}$	DC I/O <sub>VL</sub> input voltage (OE = GND or $V_L$ )	-0.3 to $V_L + 0.3$	V
$V_{I/OVCC}$	DC I/O <sub>VCC</sub> input voltage (OE = GND or $V_L$ )	-0.3 to $V_{CC} + 0.3$	V
$I_{IK}$	DC input diode current	-20	mA
$I_{I/OVL}$	DC output current	±25	mA
$I_{I/OVCC}$	DC output current	±258	mA
$I_{SCTOUT}$	Short circuit duration, continuous	40	mA
$P_D$	Power dissipation <sup>(1)</sup>	500	mW
$T_{STG}$	Storage temperature	-65 to 150	°C
TL	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	kV

1. 500 mW: 65 °C derated to 300 mW by 10W/°C: 65 °C to 85 °C

### 4.1 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Min	Typ	Max	Unit
$V_L$	Supply voltage	1.65	–	3.6	V
$V_{CC}^{(1)}$	Supply voltage	1.8	–	5.5	V
$V_{OE}$	Input voltage (OE output enable pin, $V_L$ power supply referred)	0	–	3.6	V
$V_{I/OVL}$	I/O <sub>VL</sub> voltage	0	–	$V_L$	V
$V_{I/OVCC}$	I/O <sub>VCC</sub> voltage	0	–	$V_{CC}$	V
$T_{op}$	Operating temperature	-40	–	85	°C
dt/dV	Input rise and fall time	0	–	1	ns/V

1.  $V_{CC}$  must be greater than  $V_L$ .

## 5 Electrical characteristics

### 5.1 DC characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25\text{ °C}$ .

**Table 6. DC characteristics**

Symbol	Parameter	$V_L$	$V_{CC}$	Test conditions	Value					Unit
					TA = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
$V_{IHL}$	High level input voltage ( $I/O_{VL}$ )	1.65	$V_L$ to 5.5	—	1.4	—	—	1.4	—	V
		2.0			1.6	—	—	1.6	—	
		2.5			2.0	—	—	2.0	—	
		3.0			2.4	—	—	2.4	—	
		3.6			2.8	—	—	2.8	—	
$V_{ILL}$	Low level input voltage ( $I/O_{VL}$ )	1.65	$V_L$ to 5.5	—	—	—	0.3	—	0.3	V
		2.0			—	—	0.4	—	0.4	
		2.5			—	—	0.5	—	0.5	
		3.0			—	—	0.6	—	0.6	
		3.6			—	—	0.8	—	0.8	
$V_{IHC}$	High level input voltage ( $I/O_{VCC}$ )	1.65 to $V_{CC}$	1.8	—	1.6	—	—	1.6	—	V
			2.5		2.3	—	—	2.3	—	
			3.0		2.7	—	—	2.7	—	
			3.6		3.3	—	—	3.3	—	
			4.3		3.5	—	—	3.5	—	
			5.5		4.2	—	—	4.2	—	
$V_{ILC}$	Low level input voltage ( $I/O_{VCC}$ )	1.65 - 2.5	3 - 5.5	—	—	—	—	0.3	—	V
		2.7 - 3.6	3.6 - 5.5	—	—	—	—	0.5	—	
$V_{IH-OE}$	High level input voltage (OE)	1.65	$V_L$ to 5.5	—	1.0	—	—	1.0	—	V
		2.0			1.2	—	—	1.2	—	
		2.5			1.4	—	—	1.4	—	
		3.0			1.6	—	—	1.6	—	
		3.6			2.0	—	—	2.0	—	

Table 6. DC characteristics (continued)

Symbol	Parameter	V <sub>L</sub>	V <sub>CC</sub>	Test conditions	Value					Unit
					TA = 25 °C			-40 to 85 °C		
					Min	Typ	Max	Min	Max	
V <sub>IL-OE</sub>	Low level input voltage (OE)	1.65	V <sub>L</sub> to 5.5		–	–	0.33	–	0.33	V
		2.0			–	–	0.40	–	0.40	
		2.5			–	–	0.50	–	0.50	
		3.0			–	–	0.60	–	0.60	
		3.6			–	–	0.75	–	0.75	
V <sub>OLL</sub>	Low level output voltage (I/O <sub>VL</sub> )	1.65 to 3.6	V <sub>L</sub> to 5.5	IO = 1.0 mA I/O <sub>VCC</sub> ≤ 0.15 V	–	–	0.40	–	0.40	V
V <sub>OLC</sub>	Low level output voltage (I/O <sub>VCC</sub> )	1.65 to 3.6	V <sub>L</sub> to 5.5	IO = 1.0 mA I/O <sub>VL</sub> ≤ 0.15 V	–	–	0.40	–	0.40	V
I <sub>OE</sub>	Control input leakage current (OE)	1.65 to 3.6	V <sub>L</sub> to 5.5	V <sub>OE</sub> = GND or V <sub>L</sub>	–	–	±0.1	–	±0.1	µA
I <sub>IO_LKG</sub>	High impedance leakage current (I/O <sub>VL</sub> , I/O <sub>VCC</sub> )	1.65 to 3.6	V <sub>L</sub> to 5.5	OE = GND	–	–	±0.1	–	±0.1	µA
I <sub>QVCC</sub>	Quiescent supply current V <sub>CC</sub>	1.65 to 3.6	V <sub>L</sub> to 5.5	Only pull-up resistor connected to I/O	–	3	3.5	–	4	µA
I <sub>QVL</sub>	Quiescent supply current V <sub>L</sub>	1.65 to 3.6	V <sub>L</sub> to 5.5	only pull-up resistor connected to I/O	–	0.01	0.1	–	1	µA
I <sub>Z-VCC</sub>	High impedance quiescent supply current V <sub>CC</sub>	1.65 to 3.6	V <sub>L</sub> to 5.5	OE = GND; only pull-up resistor connected to I/O	–	3	3.5	–	4	µA
I <sub>Z-VL</sub>	High impedance quiescent supply current V <sub>L</sub>	1.65 to 3.6	V <sub>L</sub> to 5.5	OE = GND; only pull-up resistor connected to I/O	–	0.01	0.1	–	1	µA



## 5.2 AC characteristics

### 5.2.1 Device driven by open drain driver

Load  $C_L = 15 \text{ pF}$ ;  $R_{up} = 4.7 \text{ k}\Omega$ ; driver  $t_r = t_f \leq 2 \text{ ns}$  over temperature range  $-40 \text{ }^\circ\text{C}$  to  $85 \text{ }^\circ\text{C}$ .

**Table 7. AC characteristics - test conditions:  $V_L = 1.65 - 1.8 \text{ V}$**

Symbol	Parameter	$V_{CC} = 1.8 - 2.5 \text{ V}$		$V_{CC} = 2.7 - 3.6 \text{ V}$		$V_{CC} = 4.3 - 5.5 \text{ V}$		Unit	
		Min	Max	Min	Max	Min	Max		
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	80.0	–	60.0	–	45.0	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	23.2	–	33.9	–	53.3	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	–	60.0	–	45.0	–	35.0	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	–	16.4	–	17.6	–	16.9	ns	
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	3.4	–	2.0	–	2.0	ns
		$t_{PHL}$	–	13.9	–	19.1	–	30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-LH}$	$t_{PLH}$	–	2.0	–	2.0	–	2.6	ns
		$t_{PHL}$	–	8.6	–	9.0	–	9.5	ns
$t_{PZL}$ $t_{PZH}$ $t_{PLZ}$ $t_{PHZ}$	Output enable and disable time	En	–	10	–	10	–	10	ns
		Dis	–	40	–	40	–	40	ns
$D_R$	Data rate <sup>(1)</sup>	–	1.8	–	2.2	–	3.4	MHz	

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

**Table 8. AC characteristics - test conditions:  $V_L = 2.5 - 2.7 \text{ V}$**

Symbol	Parameter	$V_{CC} = 2.7 - 3.6 \text{ V}$		$V_{CC} = 4.3 - 5.5 \text{ V}$		Unit	
		Min	Max	Min	Max		
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	70.0	–	50.0	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	14.8	–	19.1	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	–	50.0	–	35.0	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	–	9.8	–	10.0	ns	
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	2.0	–	2.0	ns
		$t_{PHL}$	–	8.2	–	11.6	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-LH}$	$t_{PLH}$	–	2.0	–	2.0	ns
		$t_{PHL}$	–	5.3	–	5.9	ns

**Table 8. AC characteristics - test conditions:  $V_L = 2.5 - 2.7 V$  (continued)**

Symbol	Parameter	$V_{CC} = 2.7 - 3.6 V$		$V_{CC} = 4.3 - 5.5 V$		Unit	
		Min	Max	Min	Max		
$t_{PZL} t_{PZH}$ $t_{PLZ} t_{PHZ}$	Output enable and disable time	En	–	6	–	6	ns
		Dis	–	40	–	40	ns
$D_R$	Data rate <sup>(1)</sup>	–	2.2	–	3.0	MHz	

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

**Table 9. AC characteristics - test conditions:  $V_L = 2.7 - 3.6 V$**

Symbol	Parameter	$V_{CC} = 4.3 - 5.5 V$		Unit	
		Min	Max		
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	55.0	ns	
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	17.2	ns	
$t_{RVL}$	Rise time $I/O_{VL}$	–	40.0	ns	
$t_{FVL}$	Fall time $I/O_{VL}$	–	9.7	ns	
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	2.0	ns
		$t_{PHL}$	–	10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	2.0	ns
		$t_{PHL}$	–	4.8	ns
$t_{PZL} t_{PZH}$ $t_{PLZ} t_{PHZ}$	Output enable and disable time	En	–	6	ns
		Dis	–	40	ns
$D_R$	Data rate <sup>(1)</sup>	–	–	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

### 5.2.2 Device driven by totem pole driver

Load  $C_L = 15 pF$ ;  $R_{up} = 10 k\Omega$ ; driver  $t_r=t_f \leq 2 ns$  over temperature range  $-40^\circ C$  to  $85^\circ C$

**Table 10. AC characteristics - test conditions:  $V_L = 1.65 - 1.8 V$**

Symbol	Parameter	$V_{CCB} = 1.8 - 2.5 V$		$V_{CCB} = 2.7 - 3.6 V$		$V_{CCB} = 4.3 - 5.5 V$		Unit
		Min	Max	Min	Max	Min	Max	
$t_{RVCC}$	Rise time $I/O_{VCC}$	–	7.2	–	4.6	–	1.4	ns
$t_{FVCC}$	Fall time $I/O_{VCC}$	–	23.2	–	33.9	–	53.3	ns
$t_{RVL}$	Rise time $I/O_{VL}$	–	5.9	–	5.7	–	5.5	ns
$t_{FVL}$	Fall time $I/O_{VL}$	–	16.4	–	17.6	–	16.9	ns

**Table 10. AC characteristics - test conditions:  $V_L = 1.65 - 1.8$  V**

$t_{i/OVL-VCC}$	Propagation delay time I/O <sub>VL-LH</sub> to I/O <sub>VCC-LH</sub> I/O <sub>VL-HL</sub> to I/O <sub>VCC-HL</sub>	$t_{PLH}$	–	5.5	–	4.1	–	3.6	ns
		$t_{PHL}$	–	13.9	–	19.1	–	30.2	ns
$t_{i/OVCC-VL}$	Propagation delay time I/O <sub>VCC-LH</sub> to I/O <sub>VL-LH</sub> I/O <sub>VCC-HL</sub> to I/O <sub>VL-HL</sub>	$t_{PLH}$	–	4.5	–	3.9	–	3.6	ns
		$t_{PHL}$	–	8.6	–	9.0	–	9.5	ns
$t_{pZL}$ $t_{pZH}$ $t_{pLZ}$ $t_{pHZ}$	Output enable and disable time	En	–	10	–	10	–	10	ns
		Dis	–	40	–	40	–	40	ns
$D_R$	Data rate <sup>(1)</sup>	–	–	6.4	–	4.5	–	3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

**Table 11. AC characteristics - test conditions:  $V_L = 2.5 - 2.7 V$**

Symbol	Parameter		$V_{CC} = 2.7 - 3.6 V$		$V_{CC} = 4.3 - 5.5 V$		Unit
			Min	Max	Min	Max	
$t_{RVCC}$	Rise time $I/O_{VCC}$		–	3.8	–	2.8	ns
$t_{FVCC}$	Fall time $I/O_{VCC}$		–	14.8	–	19.1	ns
$t_{RVL}$	Rise time $I/O_{VL}$		–	3.3	–	3.2	ns
$t_{FVL}$	Fall time $I/O_{VL}$		–	9.8	–	10.0	ns
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	3.2	–	2.8	ns
		$t_{PHL}$	–	8.2	–	11.6	
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	2.6	–	2.0	ns
			ns				
		$t_{PHL}$	–	5.3	–	5.9	ns
			ns				
$t_{PZL} t_{PZH}$ $t_{PLZ} t_{PHZ}$	Output enable and disable time	En	–	6	–	6	ns
		Dis	–	40	–	40	ns
$D_R$	Data rate <sup>(1)</sup>		–	9	–	6.8	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

**Table 12. AC characteristics - test conditions:  $V_L = 2.7 - 3.6 V$**

Symbol	Parameter		$V_{CC} = 4.3 - 5.5 V$		Unit
			Min	Max	
$t_{RVCC}$	Rise time $I/O_{VCC}$		–	2.9	ns
$t_{FVCC}$	Fall time $I/O_{VCC}$		–	17.2	ns
$t_{RVL}$	Rise time $I/O_{VL}$		–	3.0	ns
$t_{FVL}$	Fall time $I/O_{VL}$		–	9.7	ns
$t_{I/OVL-VCC}$	Propagation delay time $I/O_{VL-LH}$ to $I/O_{VCC-LH}$ $I/O_{VL-HL}$ to $I/O_{VCC-HL}$	$t_{PLH}$	–	2.7	ns
		$t_{PHL}$	–	10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time $I/O_{VCC-LH}$ to $I/O_{VL-LH}$ $I/O_{VCC-HL}$ to $I/O_{VL-HL}$	$t_{PLH}$	–	1.9	ns
			ns		
		$t_{PHL}$	–	4.8	ns
			ns		
$t_{PZL} t_{PZH}$ $t_{PLZ} t_{PHZ}$	Output enable and time	En	–	6	ns
		Dis	–	40	ns
$D_R$	Data rate <sup>(1)</sup>		–	7.2	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation not less than 30%.

Figure 4. Test circuit

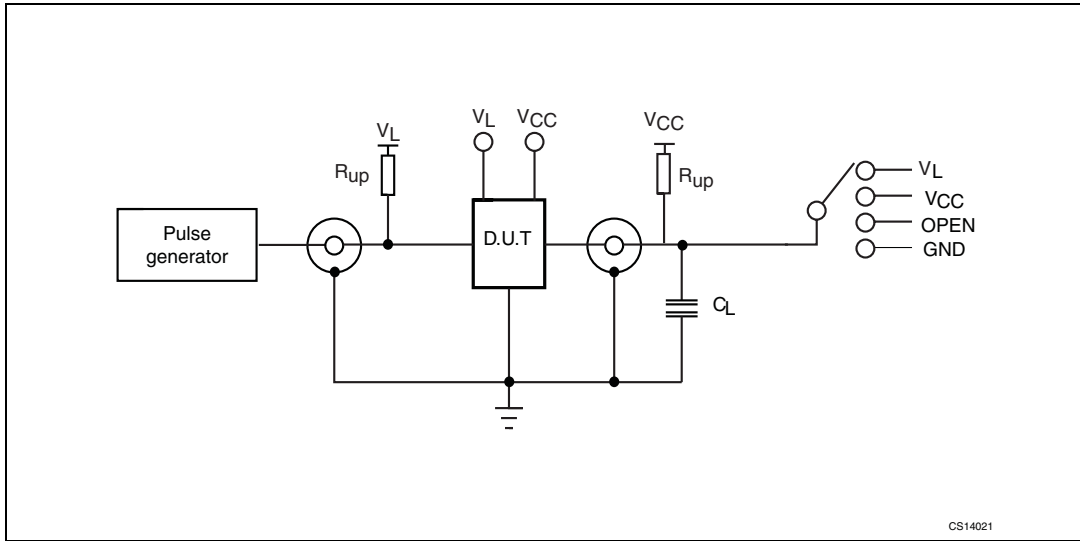


Table 13. Test circuit switches

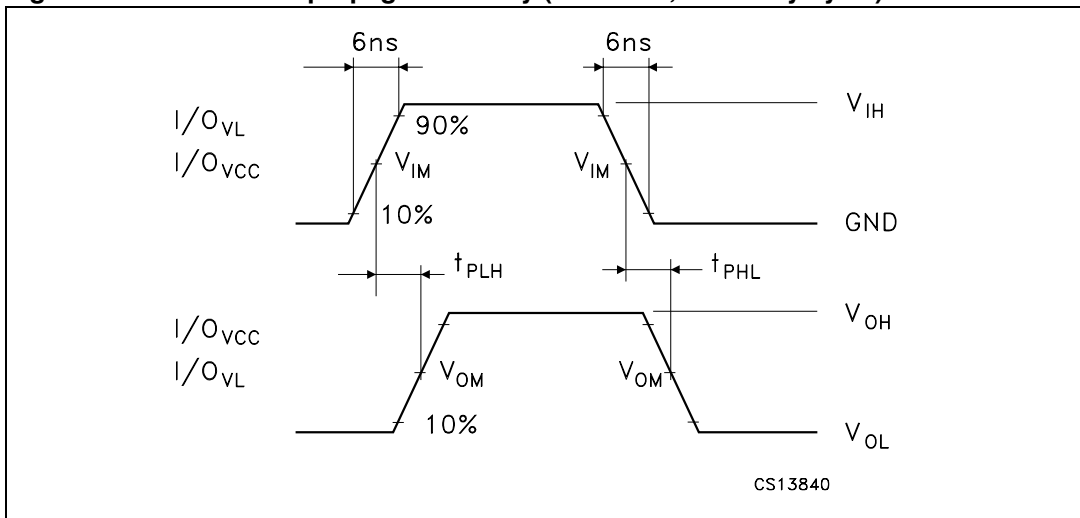
Test	Switch		
	Driving I/O <sub>V<sub>L</sub></sub>	Driving I/O <sub>V<sub>CC</sub></sub>	Open drain driving
t <sub>PLH</sub> , t <sub>PHL</sub>	Open	Open	Open

# 6 Waveforms

**Table 14. Waveform symbol value**

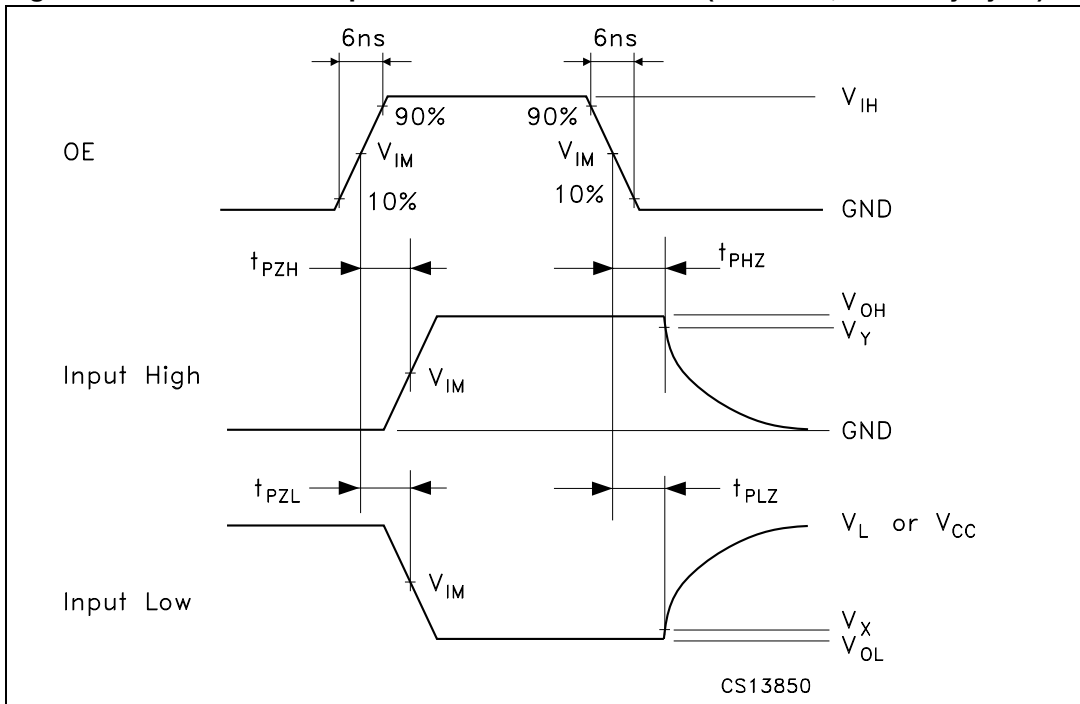
Symbol	Driving I/O <sub>VL</sub>		Driving I/O <sub>VCC</sub>	
	$1.8\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.0\text{ V}$	$1.8\text{ V} \leq V_L \leq V_{CC} \leq 2.5\text{ V}$	$3.3\text{ V} \leq V_L \leq V_{CC} \leq 5.0\text{ V}$
V <sub>IH</sub>	V <sub>L</sub>	V <sub>L</sub>	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>IM</sub>	50% V <sub>L</sub>	50% V <sub>L</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>
V <sub>OM</sub>	50% V <sub>CC</sub>	50% V <sub>CC</sub>	50% V <sub>L</sub>	50% V <sub>L</sub>
V <sub>X</sub>	V <sub>OL</sub> + 0.15V	V <sub>OL</sub> + 0.3V	V <sub>OL</sub> + 0.15V	V <sub>OL</sub> + 0.3V
V <sub>Y</sub>	V <sub>OH</sub> - 0.15V	V <sub>OH</sub> - 0.3V	V <sub>OH</sub> - 0.15V	V <sub>OH</sub> - 0.3V

**Figure 5. Waveform - propagation delay (f = 1 MHz; 50% duty cycle)**



CS13840

Figure 6. Waveform - output enable and disable time (f = 1 MHz; 50% duty cycle)



# 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Figure 7. Package outline for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch**

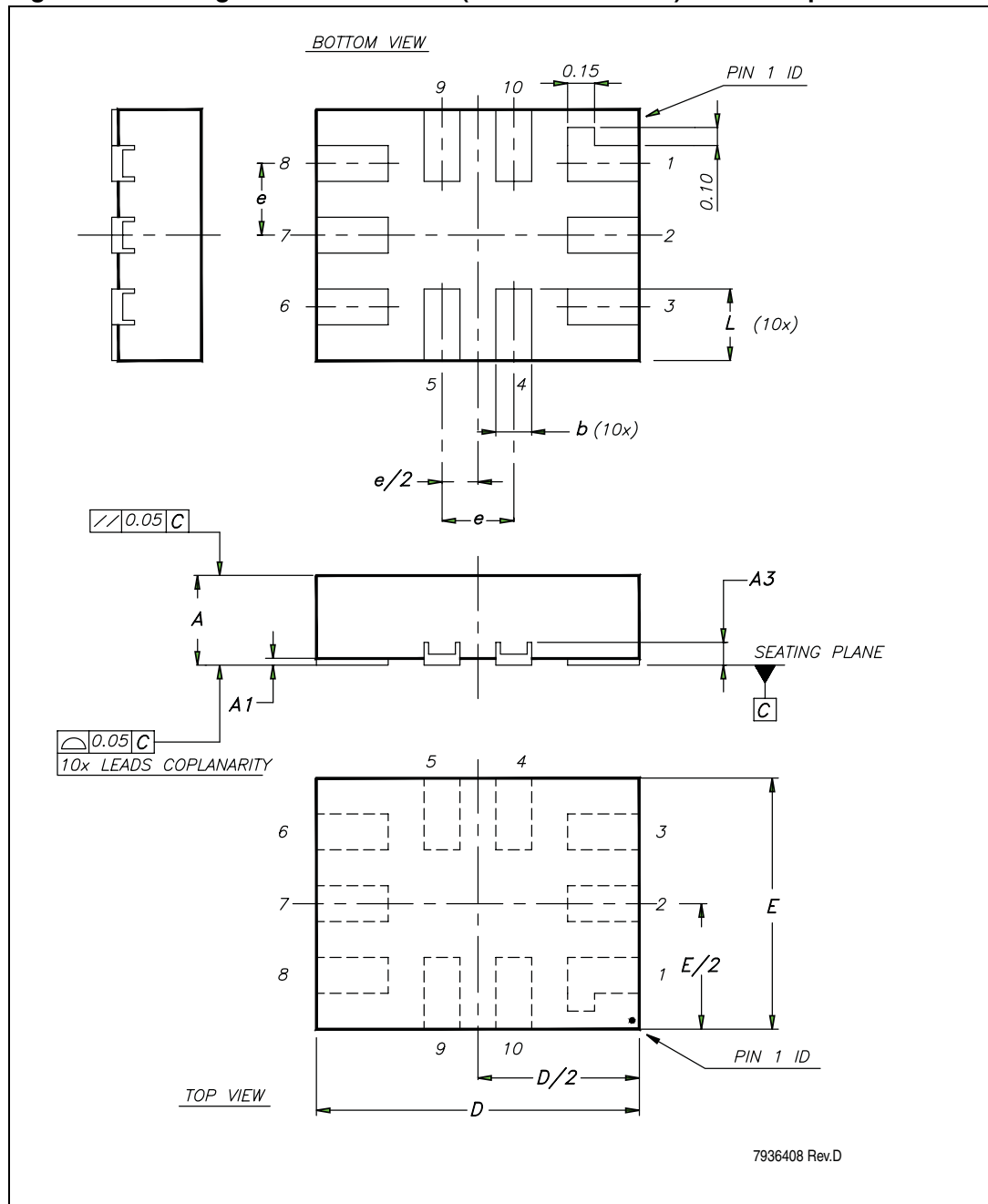




Table 15. Mechanical data for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

Symbol	Millimeters		
	Typ	Min	Max
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127		
b	0.20	0.15	0.25
D	1.80	1.75	1.85
E	1.40	1.35	1.45
e	0.40		
L	0.40	0.35	0.45

Figure 8. Footprint recommendation for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

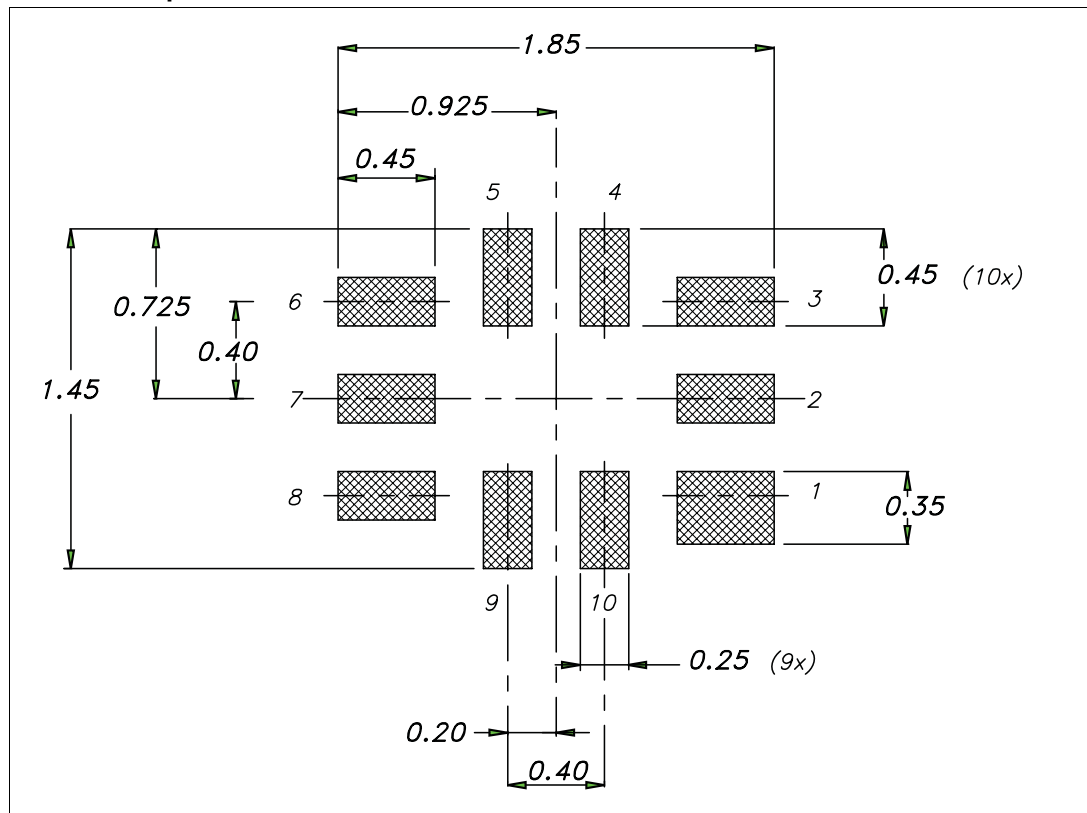


Figure 9. Carrier tape for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

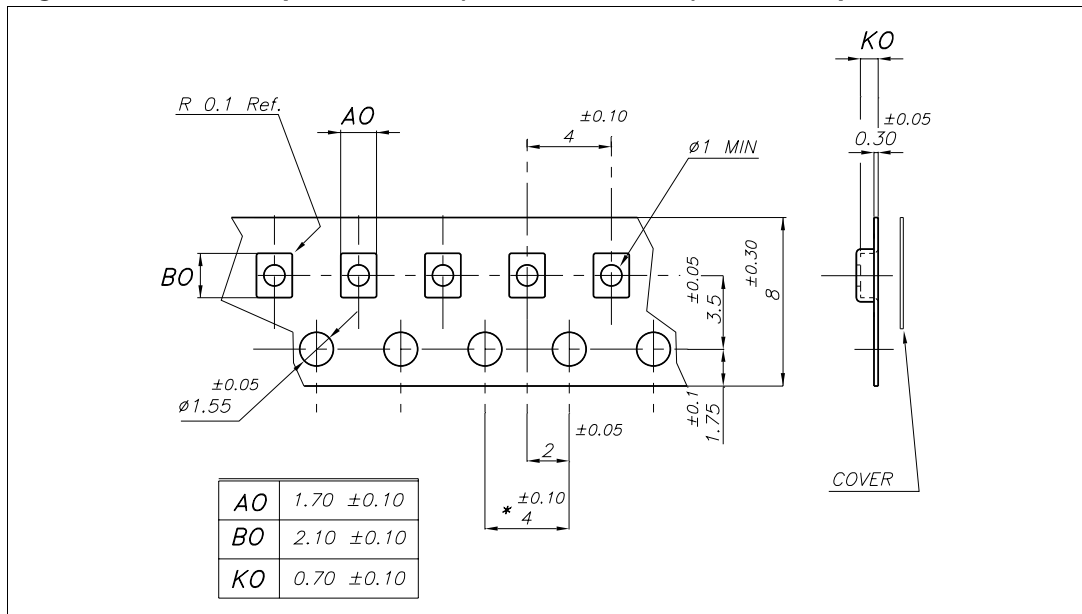


Figure 10. Reel information for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

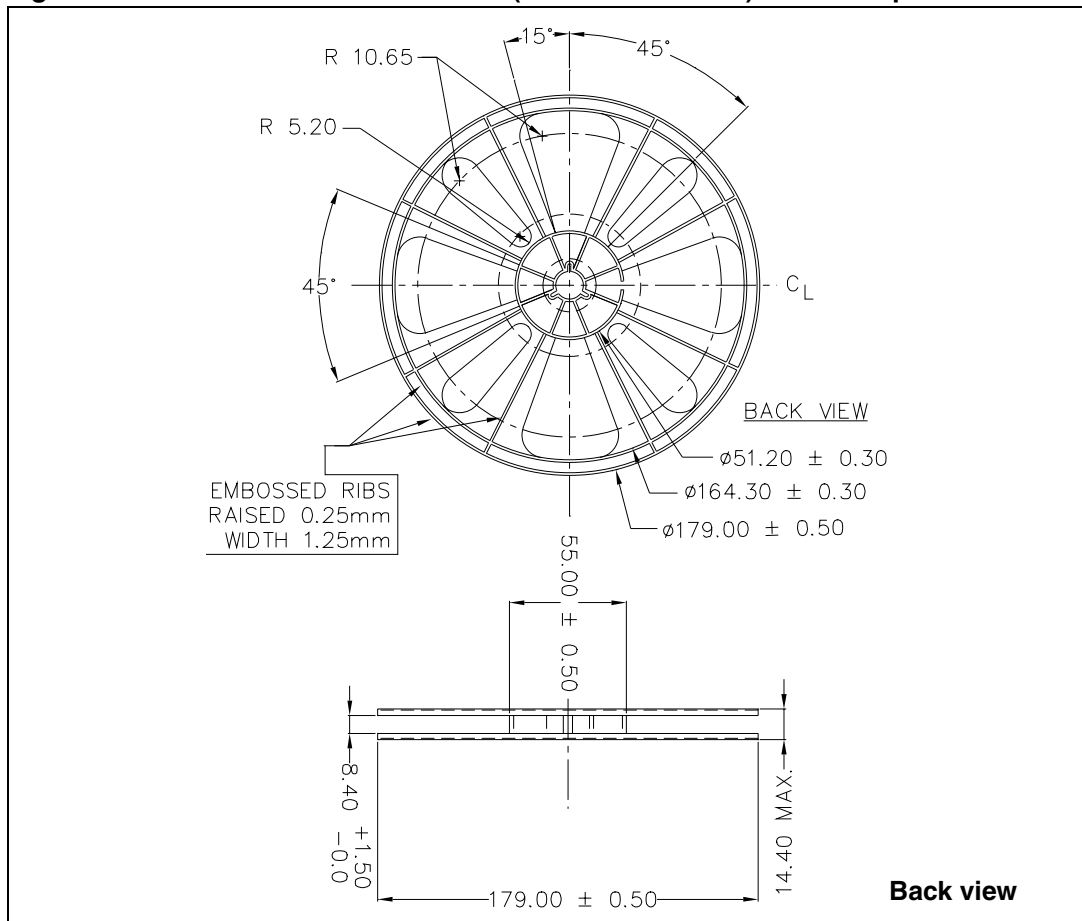
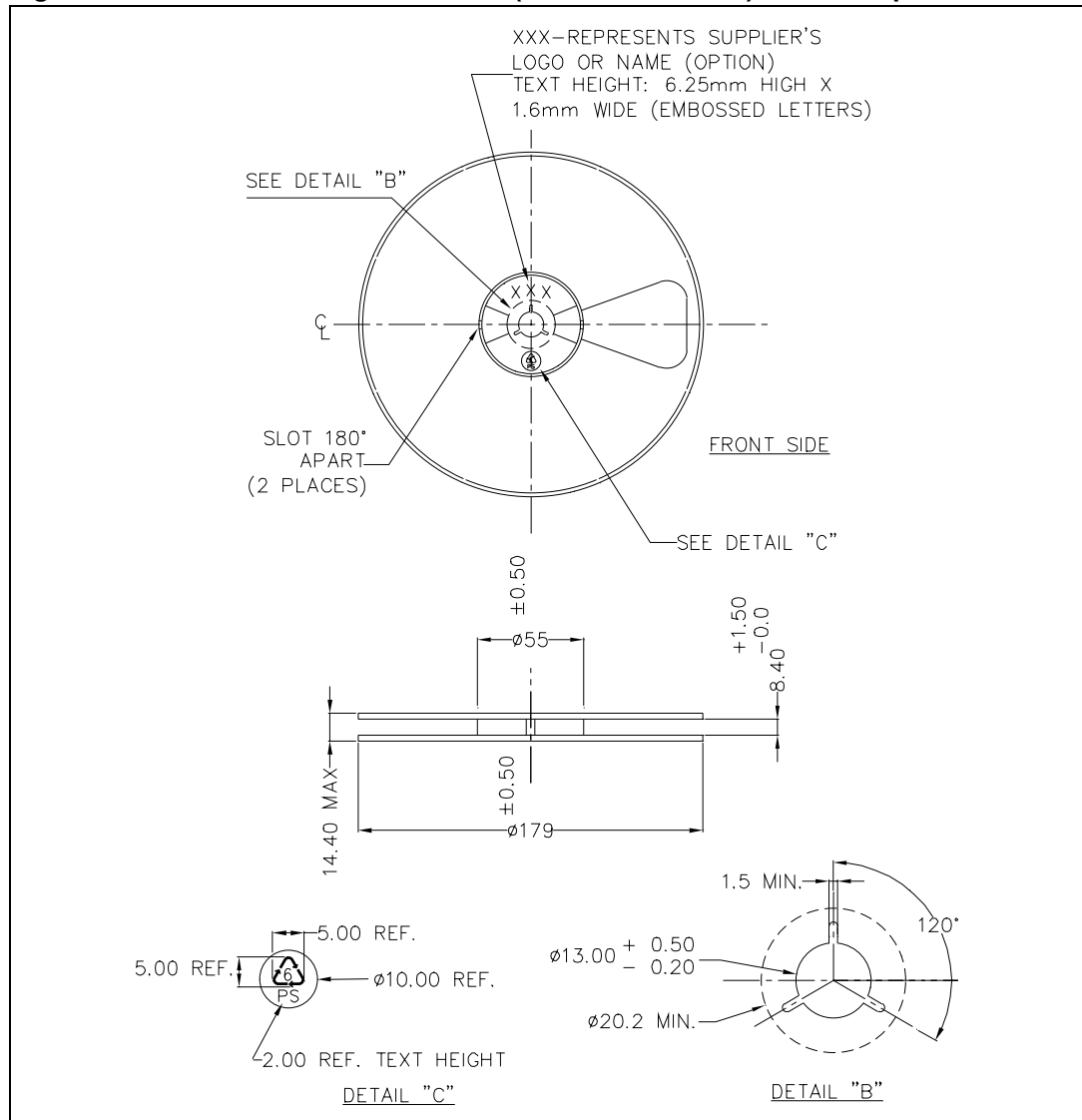


Figure 11. Reel information for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch



## 8 Revision history

**Table 16. Document revision history**

Date	Revision	Changes
16-Jul-2008	1	Initial release.
22-Jun-2009	2	Document status promoted from Preliminary data to datasheet. Updated: Features section and <i>Chapter 5: Electrical characteristics</i> . Modified: <i>Section 7</i> .

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