- **Members of the Texas Instruments**
  **Widebus™ Family**

- **State-of-the-Art _EPIC_-II_B_™ BiCMOS Design**
  **Significantly Reduces Power Dissipation**

- **Latch-Up Performance Exceeds 500 mA Per**
  **JEDEC Standard JESD-17**

- **Typical $V_{OLP}$ (Output Ground Bounce) < 1 V**
  **at $V_{CC}$ = 5 V, $T_A$ = 25°C**

- **Distributed $V_{CC}$ and GND Pin Configuration**
  **Minimizes High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB**
  **Layout**

- **High-Drive Outputs (–32-mA $I_{OH}$, 64-mA $I_{OL}$)**

- **Package Options Include Plastic 300-mil**
  **Shrink Small-Outline (DL) and Thin Shrink**
  **Small-Outline (DGG) Packages and 380-mil**
  **Fine-Pitch Ceramic Flat (WD) Package**
  **Using 25-mil Center-to-Center Spacings**

**SN54ABT16543 . . . WD PACKAGE**
**SN74ABT16543 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| 1$\overline{OEAB}$ | 1 | 56 | 1$\overline{OEBA}$ |
| 1$\overline{LEAB}$ | 2 | 55 | 1$\overline{LEBA}$ |
| 1$\overline{CEAB}$ | 3 | 54 | 1$\overline{CEBA}$ |
| GND | 4 | 53 | GND |
| 1A1 | 5 | 52 | 1B1 |
| 1A2 | 6 | 51 | 1B2 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| 1A3 | 8 | 49 | 1B3 |
| 1A4 | 9 | 48 | 1B4 |
| 1A5 | 10 | 47 | 1B5 |
| GND | 11 | 46 | GND |
| 1A6 | 12 | 45 | 1B6 |
| 1A7 | 13 | 44 | 1B7 |
| 1A8 | 14 | 43 | 1B8 |
| 2A1 | 15 | 42 | 2B1 |
| 2A2 | 16 | 41 | 2B2 |
| 2A3 | 17 | 40 | 2B3 |
| GND | 18 | 39 | GND |
| 2A4 | 19 | 38 | 2B4 |
| 2A5 | 20 | 37 | 2B5 |
| 2A6 | 21 | 36 | 2B6 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| 2A7 | 23 | 34 | 2B7 |
| 2A8 | 24 | 33 | 2B8 |
| GND | 25 | 32 | GND |
| 2$\overline{CEAB}$ | 26 | 31 | 2$\overline{CEBA}$ |
| 2$\overline{LEAB}$ | 27 | 30 | 2$\overline{LEBA}$ |
| 2$\overline{OEAB}$ | 28 | 29 | 2$\overline{OEBA}$ |
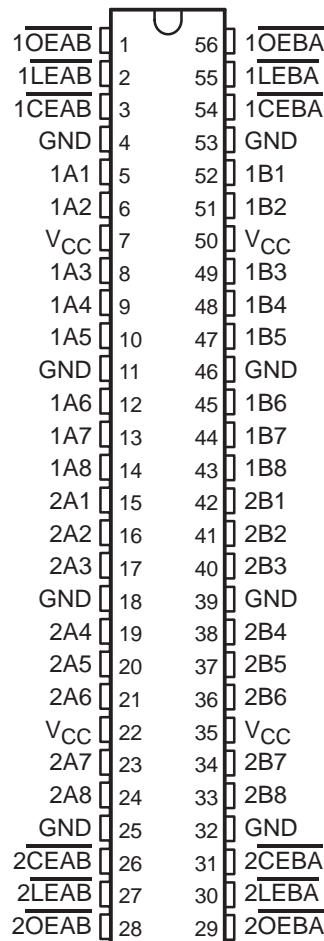
**description**

The 'ABT16543 16-bit registered transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. The 'ABT16543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16543 is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**TEXAS INSTRUMENTS**

**FUNCTION TABLE†**
**(each 8-bit section)**

| INPUTS | | | | OUTPUT B |
|---|---|---|---|---|
| $\overline{\text{CEAB}}$ | $\overline{\text{LEAB}}$ | $\overline{\text{OEAB}}$ | A | |
| H | X | X | X | Z |
| X | X | H | X | Z |
| L | H | L | X | $B_0$‡ |
| L | L | L | L | L |
| L | L | L | H | H |

† A-to-B data flow is shown; B-to-A flow control is the
  same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.
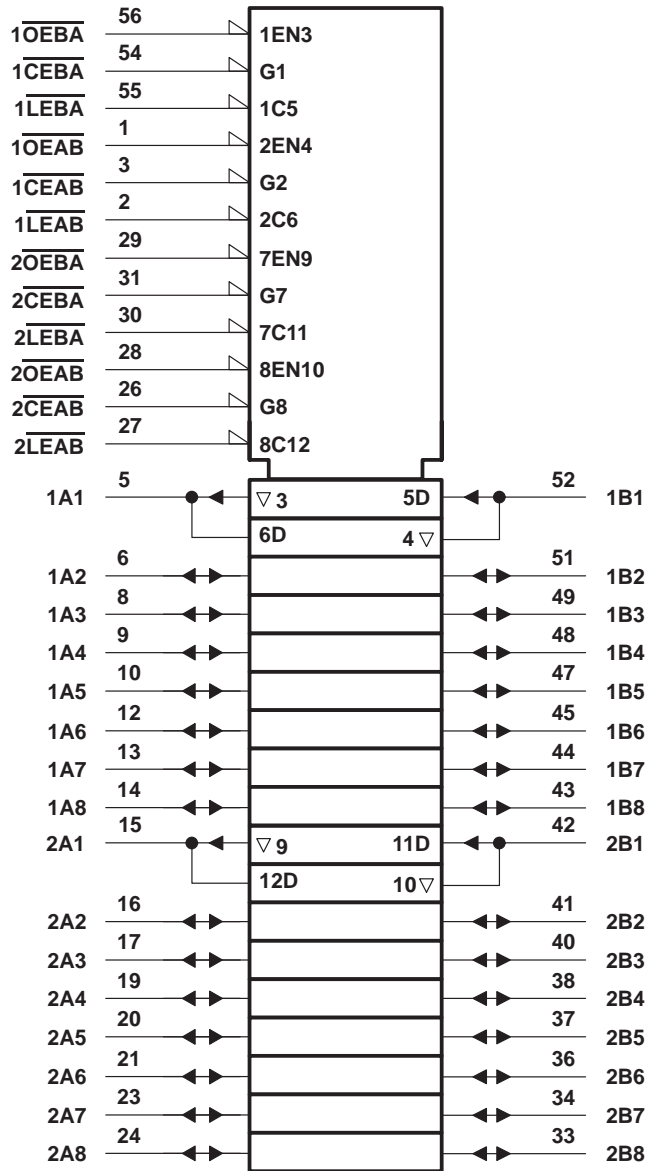‡ Output level before the indicated steady-state input
  conditions were established

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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)
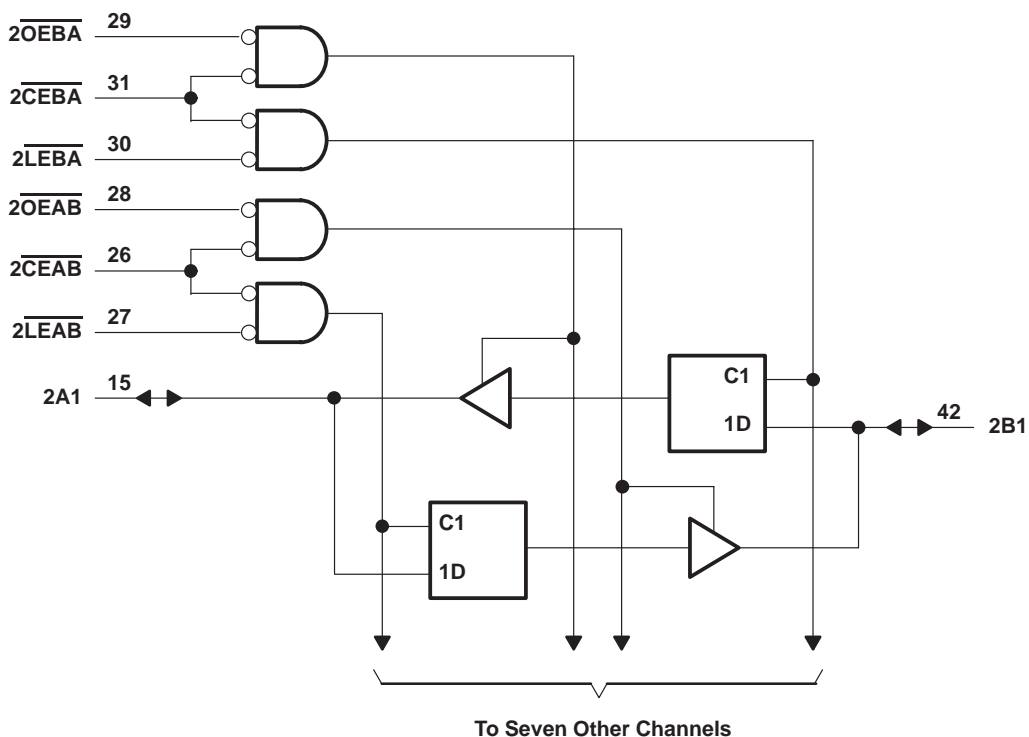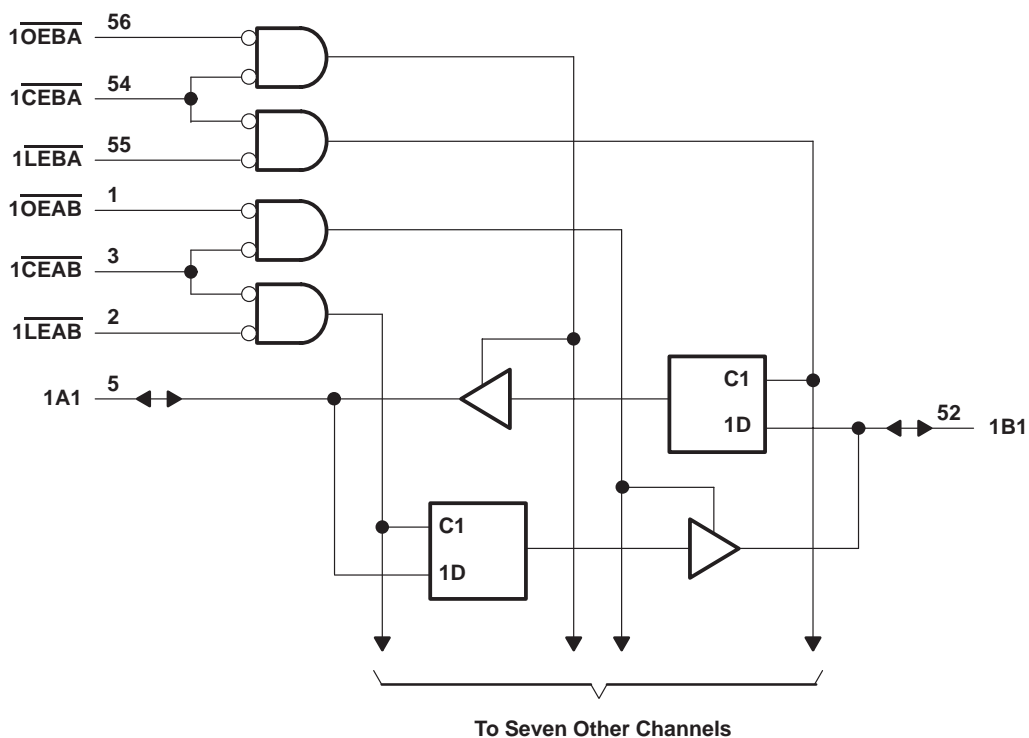


To Seven Other Channels



To Seven Other Channels

![Texas Instruments logo]

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ . . . . . . . . . . . . . . . . . . . –0.5 V to 5.5 V
Current into any output in the low state, $I_O$: SN54ABT16543 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 96 mA
                                               SN74ABT16543 . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 128 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –18 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 81°C/W
                                                    DL package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 74°C/W
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

**recommended operating conditions (see Note 3)**

| | | | SN54ABT16543 | | SN74ABT16543 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

**TEXAS**
**INSTRUMENTS**

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A = 25°C$ | | | SN54ABT16543 | | SN74ABT16543 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| $V_{IK}$ | | $V_{CC} = 4.5$ V, | $I_I = -18$ mA | | | −1.2 | | −1.2 | | −1.2 | V |
| $V_{OH}$ | | $V_{CC} = 4.5$ V, | $I_{OH} = -3$ mA | 2.5 | | | 2.5 | | 2.5 | | V |
| | | $V_{CC} = 5$ V, | $I_{OH} = -3$ mA | 3 | | | 3 | | 3 | | |
| | | $V_{CC} = 4.5$ V | $I_{OH} = -24$ mA | 2 | | | 2 | | | | |
| | | | $I_{OH} = -32$ mA | 2* | | | | | 2 | | |
| $V_{OL}$ | | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | | 0.55 | | 0.55 | | | V |
| | | | $I_{OL} = 64$ mA | | | 0.55* | | | | 0.55 | |
| $V_{hys}$ | | | | | 100 | | | | | | mV |
| $I_I$ | Control inputs | $V_{CC} = 5.5$ V, | $V_I = V_{CC}$ or GND | | | ±1 | | ±1 | | ±1 | µA |
| | A or B ports | | | | | ±100 | | ±100 | | ±100 | |
| $I_{OZH}$‡ | | $V_{CC} = 5.5$ V, | $V_O = 2.7$ V | | | 50** | | 10 | | 50 | µA |
| $I_{OZL}$‡ | | $V_{CC} = 5.5$ V, | $V_O = 0.5$ V | | | −50** | | −10 | | −50 | µA |
| $I_{off}$ | | $V_{CC} = 0$, | $V_I$ or $V_O ≤ 4.5$ V | | | ±100 | | | | ±100 | µA |
| $I_{CEX}$ | | $V_{CC} = 5.5$ V, $V_O = 5.5$ V | Outputs high | | | 50 | | 50 | | 50 | µA |
| $I_O$§ | | $V_{CC} = 5.5$ V, | $V_O = 2.5$ V | −50 | −100 | −200 | −50 | −200 | −50 | −200 | mA |
| $I_{CC}$ | A or B ports | $V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | | 2 | | 2 | | 2 | mA |
| | | | Outputs low | | | 35 | | 35 | | 35 | |
| | | | Outputs disabled | | | 2 | | 2 | | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | | 0.5 | | 0.5 | mA |
| $C_i$ | Control inputs | $V_I = 2.5$ V or 0.5 V | | | 3 | | | | | | pF |
| $C_{io}$ | A or B ports | $V_O = 2.5$ V or 0.5 V | | | 8.5 | | | | | | pF |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.
\*\* These limits apply only to the SN74ABT16543.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters $I_{OZH}$ and $I_{OZL}$ include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | | $V_{CC} = 5$ V, $T_A = 25°C$ | | SN54ABT16543 | | SN74ABT16543 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low | | 4 | | 4 | | 4 | | ns |
| $t_{su}$ | Setup time, data before $\overline{LEAB}$↑ or $\overline{LEBA}$↑ | High | 1.5 | | 1.5 | | 1.5 | | ns |
| | | Low | 3.5 | | 3.5 | | 3.5 | | |
| $t_h$ | Hold time, data after $\overline{LEAB}$↑ or $\overline{LEBA}$↑ | High | 1.5 | | 1.5 | | 1.5 | | ns |
| | | Low | 2 | | 2 | | 2 | | |

TEXAS
INSTRUMENTS

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT16543 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 0.8 | 2.5 | 3.3 | 0.8 | 3.9 | ns |
| $t_{PHL}$ | | | 0.9 | 2.7 | 4.4 | 0.9 | 5.2 | |
| $t_{PLH}$ | $\overline{LE}$ | A or B | 1 | 3.1 | 4.3 | 1 | 5.3 | ns |
| $t_{PHL}$ | | | 1.2 | 3.3 | 4.8 | 1.2 | 5.7 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 0.8 | 3.4 | 4.3 | 0.8 | 5.3 | ns |
| $t_{PZL}$ | | | 1.1 | 3.8 | 7 | 1.1 | 7.9 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.9 | 4 | 6.3 | 1.9 | 7.2 | ns |
| $t_{PLZ}$ | | | 1.6 | 3.3 | 4.6 | 1.6 | 5 | |
| $t_{PZH}$ | $\overline{CE}$ | A or B | 0.9 | 3.8 | 4.9 | 0.9 | 6.3 | ns |
| $t_{PZL}$ | | | 1.2 | 4.2 | 6.8 | 1.2 | 7.9 | |
| $t_{PHZ}$ | $\overline{CE}$ | A or B | 2 | 4.5 | 6.4 | 2 | 7.3 | ns |
| $t_{PLZ}$ | | | 1.7 | 3.9 | 5.1 | 1.7 | 5.6 | |

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT16543 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 1 | 2.5 | 3.3 | 1 | 3.8 | ns |
| $t_{PHL}$ | | | 1 | 2.7 | 4.4 | 1 | 5.1 | |
| $t_{PLH}$ | $\overline{LE}$ | A or B | 1 | 3.1 | 4.3 | 1 | 5.2 | ns |
| $t_{PHL}$ | | | 1.2 | 3.3 | 4.8 | 1.2 | 5.6 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 3.4 | 4.3 | 1 | 5.2 | ns |
| $t_{PZL}$ | | | 1.1 | 3.8 | 5.9 | 1.1 | 7 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 1.9 | 4 | 5 | 1.9 | 5.7 | ns |
| $t_{PLZ}$ | | | 1.6 | 3.3 | 4.2 | 1.6 | 4.6 | |
| $t_{PZH}$ | $\overline{CE}$ | A or B | 1 | 3.8 | 4.9 | 1 | 6.2 | ns |
| $t_{PZL}$ | | | 1.2 | 4.2 | 6.5 | 1.2 | 7.8 | |
| $t_{PHZ}$ | $\overline{CE}$ | A or B | 2 | 4.5 | 5.6 | 2 | 6.6 | ns |
| $t_{PLZ}$ | | | 1.7 | 3.9 | 5.1 | 1.7 | 5.4 | |

TEXAS
INSTRUMENTS

## PARAMETER MEASUREMENT INFORMATION

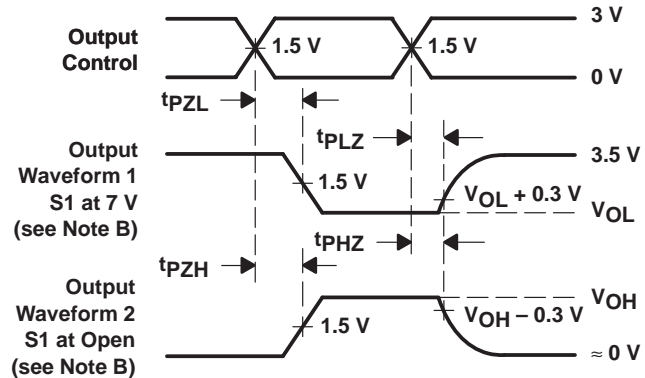| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

**LOAD CIRCUIT**
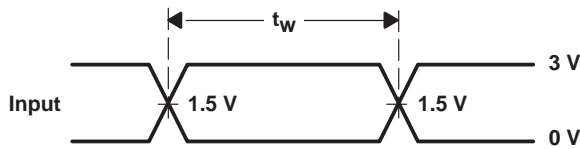
**VOLTAGE WAVEFORMS**
**PULSE DURATION**
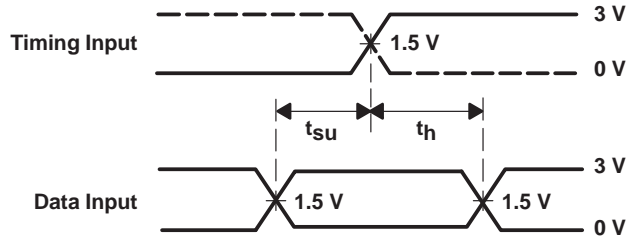
**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
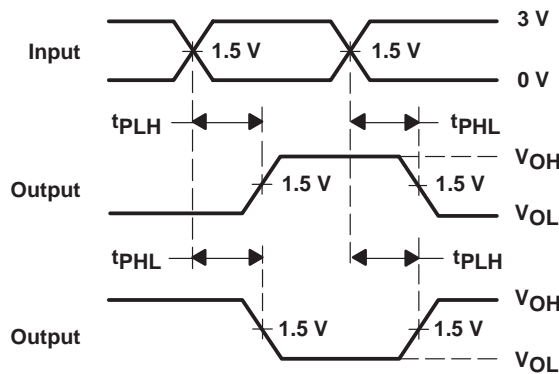
**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9324101MXA | ACTIVE | CFP | WD | 56 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9324101MX A SNJ54ABT16543W D | Samples |
| 74ABT16543DGGRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16543 | Samples |
| SN74ABT16543DGGR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16543 | Samples |
| SN74ABT16543DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16543 | Samples |
| SN74ABT16543DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16543 | Samples |
| SNJ54ABT16543WD | ACTIVE | CFP | WD | 56 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9324101MX A SNJ54ABT16543W D | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABT16543, SN74ABT16543 :**

● Catalog: SN74ABT16543

● Military: SN54ABT16543

NOTE: Qualified Version Definitions:

   ● Catalog - TI's standard catalog product

   ● Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | | |
|---|---|---|
| A0 | Dimension designed to accommodate the component width | |
| B0 | Dimension designed to accommodate the component length | |
| K0 | Dimension designed to accommodate the component thickness | |
| W | Overall width of the carrier tape | |
| P1 | Pitch between successive cavity centers | |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ABT16543DGGR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74ABT16543DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ABT16543DGGR | TSSOP | DGG | 56 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74ABT16543DLR | SSOP | DL | 56 | 1000 | 367.0 | 367.0 | 55.0 |

**WD (R-GDFP-F\*\*)**                                               **CERAMIC DUAL FLATPACK**

**48 LEADS SHOWN**



| NO. OF LEADS\*\* | 48 | 56 |
|---|---|---|
| A MAX | 0.640 (16,26) | 0.740 (18,80) |
| A MIN | 0.610 (15,49) | 0.710 (18,03) |

4040176 / D 10/97

NOTES:  A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.
C.  This package can be hermetically sealed with a ceramic lid using glass frit.
D.  Index point is provided on cap for terminal identification only
E.  Falls within MIL STD 1835:  GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

DL (R−PDSO−G56)                                   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343) / 0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56                                                        29

0.420 (10,67) / 0.395 (10,03)

0.299 (7,59) / 0.291 (7,39)

0.010 (0,25) / 0.005 (0,13)

Gage Plane

0°−8°

0.010 (0,25)

0.040 (1,02) / 0.020 (0,51)

1                                                        28

0.730 (18,54) / 0.720 (18,29)

0.110 (2,79) MAX

0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−4/F  05/13

NOTES:   A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

PowerPAD is a trademark of Texas Instruments.

**TEXAS INSTRUMENTS**
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8.3
7.9 TYP

A

PIN 1 ID
AREA

54X [0.5]

56

1

C

SEATING PLANE

[ ⌒ | 0.1 | C ]

14.1
13.9
NOTE 3

2X
[13.5]

28

29

6.2
6.0

B

56X 0.27
0.17

[ ⊕ | 0.08 Ⓜ | C | AⓈ | BⓈ ]

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4222167/A   07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
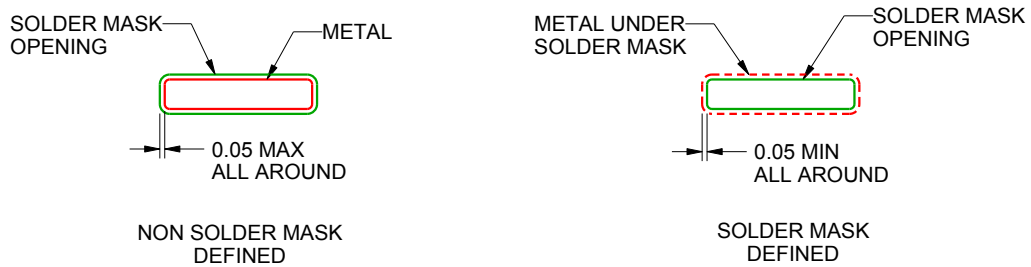4. Reference JEDEC registration MO-153.

56X (1.5)

1

56X (0.3)

54X (0.5)

(R0.05)
TYP

SYMM
℄

56

SYMM
℄

28

29

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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