87C51/87C52T2

8-Bit CMOS Microcontrollers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Software- and pin-compatible with 80C51
- Beneficial for prototyping and initial production
- All 80C51BH and 80C52T2 features retained
- Flashrite™ EPROM programming
- Two-level Program Memory Lock
- 32-Byte Encryption Array
- In-Circuit Test Mode facilitates testing

	RAM (bytes)	EPROM (bytes)
87C51	128	4K
87C52T2	256	8K

87C51 = User-programmable 80C51BH
87C52T2 = User-programmable 80C52T2

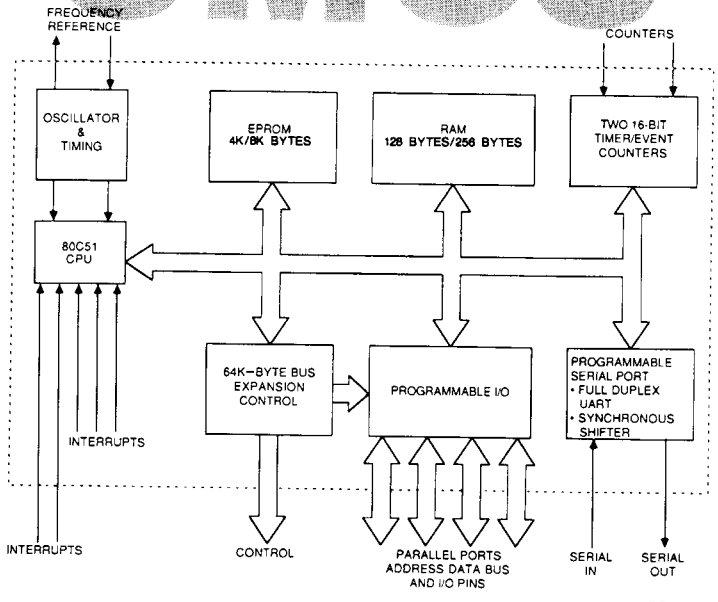
GENERAL DESCRIPTION

The 87C51 and 87C52T2 are CMOS EPROM versions of the 80C51BH and 80C52T2, respectively. The 87C51 includes 4K bytes of on-chip EPROM, and the 87C52T2 includes 8K bytes of EPROM.

These user-programmable products are software- and pin-compatible with their ROM-based counterparts. All of the 80C52BH and 80C52T2 features are retained. For more information consult the 80C51/80C31BH/80C52T2/80C32T2 data sheet (order #04815).

Additionally, several new features are offered on the EPROM versions. The 87C51 and 87C52T2 EPROM array support the Flashrite programming algorithm that allows a 4K-byte EPROM array to be programmed in approximately 12 seconds. A two-level programmable lock structure prevents externally fetched code from accessing internal Program Memory and can disable EPROM verification and programming. A 32-byte Encryption Array can be used to encode the program code bytes during EPROM verification.

BLOCK DIAGRAM



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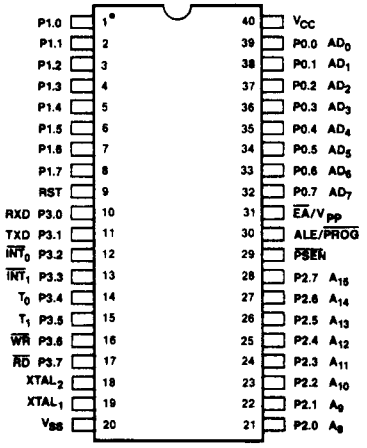
Issue Date: October 1989

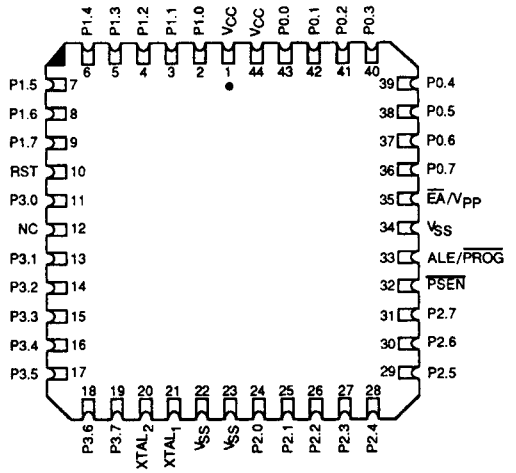
CONNECTION DIAGRAMS
Top View

DIP



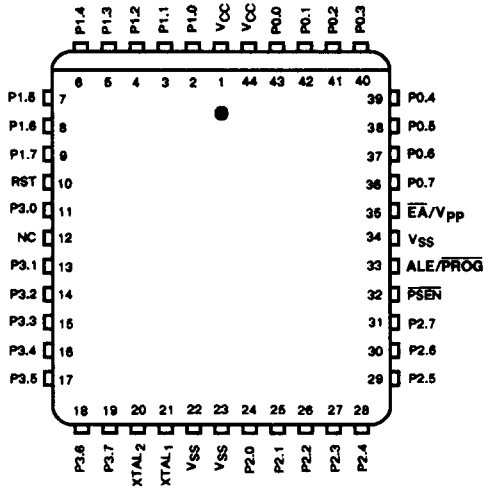
CD005553

LCC



CD010873

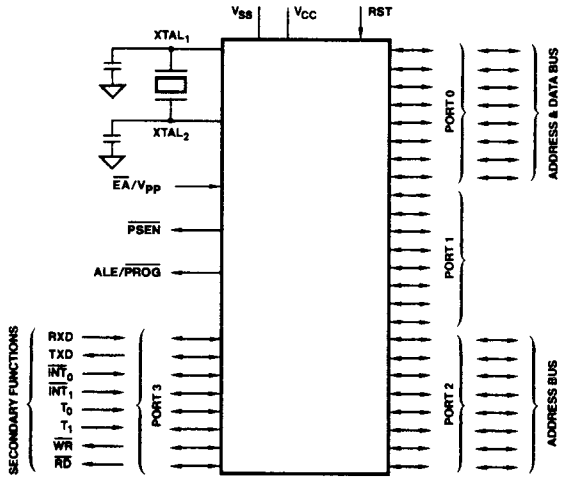
PLCC



CD009442

Notes: Pin 1 is marked for orientation.
NC pins on the PLCC and LCC packages have been utilized as additional V_{CC} and V_{SS} connections to improve noise immunity. It is recommended that these pins (1, 23, and 37) be connected appropriately; however, they may be left floating to insure second source compatibility.

LOGIC SYMBOL



LS001326

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Temperature Range
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing

D 87C51 — —

e. OPTIONAL PROCESSING
Blank = Standard processing

d. SPEED OPTION
Blank = 3.5 to 12 MHz
-1 = 3.5 to 16 MHz

c. DEVICE NUMBER/DESCRIPTION
87C51/87C52T2
8-Bit CMOS Microcontrollers
87C51 — 4K EPROM
87C52T2 — 8K EPROM

b. PACKAGE TYPE
D = 40-Pin Ceramic DIP (CDV040)
R = 44-Pin Ceramic Leadless Chip Carrier (CLV044)
P = 40-Pin Plastic DIP (PD 040)
N = 44-Pin Plastic Leadless Chip Carrier (PL 044)

a. TEMPERATURE RANGE
Blank = Commercial (0 to +70°C)
I = Industrial (-40 to +85°C)

Valid Combinations	
D, R, P, N ID, IR, IP, IN	87C51
	87C51-1
	87C52T2
	87C52T2-1

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Port 0 (Bidirectional; Open Drain)

Port 0 is an open-drain I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C51/87C52T2. External pullups are required during program verification.

Port 1 (Bidirectional)

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four LS TTL inputs. Port 1 pins that have 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 1 pins that are externally being pulled Low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during program verification.

Port 2 (Bidirectional)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four LS TTL inputs. Port 2 pins having 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 2 pins externally being pulled Low will source current (I_{IL}) because of internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function register.

Port 2 also receives the high-order address bits during the programming of the EPROM and during program verification of the EPROM, as well as some control signals.

Port 3 (Bidirectional)

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four LS TTL inputs. Port 3 pins having 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 3 pins externally being pulled Low will source current (I_{IL}) because of the pullups. Port 3 also receives some control signals for EPROM programming and program verification.

Port 3 also serves the functions of various special features as listed below:

Port Pin	Alternate Function
$P_{3.0}$	RxD (Serial Input Port)
$P_{3.1}$	TxD (Serial Output Port)
$P_{3.2}$	$\overline{INT_0}$ (External Interrupt 0)
$P_{3.3}$	$\overline{INT_1}$ (External Interrupt 1)
$P_{3.4}$	T_0 (Timer 0 External Input)
$P_{3.5}$	T_1 (Timer 1 External Input)
$P_{3.6}$	$\overline{WR}$ (External Data Memory Write Strobe)
$P_{3.7}$	$\overline{RD}$ (External Data Memory Read Strobe)

RST Reset (Input; Active High)

This pin is used to reset the device when held High for two machine cycles while the oscillator is running. A small internal resistor permits power-on reset using only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$ Address Latch Enable/$\overline{Program\ Pulse}$ (Input/Output)

Address Latch Enable is the output pulse for latching the low byte of the address during accesses to external memory. ALE can drive eight LS TTL inputs.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, allowing use for external-timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. This pin also accepts the program pulse input ($\overline{PROG}$) when programming the EPROM.

$\overline{PSEN}$ Program Store Enable (Output; Active Low)

$\overline{PSEN}$ is the read strobe to external Program Memory. $\overline{PSEN}$ can drive eight LS TTL inputs. When the device is executing code from an external program memory, $\overline{PSEN}$ is activated twice each machine cycle—except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal Program Memory.

$\overline{EA}$/V_{PP} External Access Enable/Programming Voltage (Input; Active Low)

$\overline{EA}$ must be externally held Low to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. If $\overline{EA}$ is held High, the 87C51/87C52T2 executes from internal Program Memory unless the program counter contains an address greater than 0FFFH.

This pin also receives the 12.75-V programming supply voltage during programming of the EPROM.

$XTAL_1$ Crystal (Input)

Input to the inverting-oscillator amplifier, and input to the internal clock-generator circuits.

$XTAL_2$ Crystal (Output)

Output of the inverting-oscillator amplifier.

V_{CC} Power Supply

Power supply during normal, idle, and power-down operations.

V_{SS} Circuit Ground

PROGRAMMING

The 87C51/87C52T2 can be programmed with the Flashrite algorithm. It differs from other methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

To program the EPROM, either the internal or external oscillator must be running between 4 and 6 MHz, since the internal bus is used to transfer address and program data to the appropriate internal registers. Table 1 shows the various EPROM programming modes.

TABLE 1. EPROM PROGRAMMING MODES FOR THE 87C51/87C52T2

Mode	RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Program Code	H	L	L*	V_{PP}	H	L	H	H
Verify Code	H	L	H	V_{PPX}	L	L	H	H
Pgm Encryption Table	H	L	L*	V_{PP}	H	L	H	L
Pgm Lock Bit 1	H	L	L*	V_{PP}	H	H	H	H
Pgm Lock Bit 2	H	L	L*	V_{PP}	H	H	L	L
Read Silicon Signature	H	L	H	H	L	L	L	L

Key: H = Logic High for that pin
L = Logic Low for that pin
V_{PP} = 12.75 V ±0.25 V
V_{CC} = 5 V ±10% during programming and verification
2.0 V < V_{PPX} < 13.0 V

*ALE/$\overline{PROG}$ receives 25 programming pulses while V_{PP} is held at 12.75 V. Each programming pulse is low for 100 μs (±10% μs) and high for a minimum of 10 μs.

Programming

The programming configuration is shown in Figure 1. The address of the EPROM location to be programmed is applied to Ports 1 and 2 as shown in the figure. The programming configuration of the 87C52T2 is identical except that P2.4 is also used as an address input. The code byte to be programmed into that location is applied to Port 0. Once RST, $\overline{PSEN}$, Port 2, and Port 3 are held to the levels indicated in Figure 1, ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 2.

The maximum voltage applied to the $\overline{EA}$/V_{PP} pin must not exceed 13 V at any time as specified for V_{PP}. Even a slight spike can cause permanent damage to the device. The V_{PP} source should thus be well regulated and glitch-free.

When programming, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious transients which may damage the device.

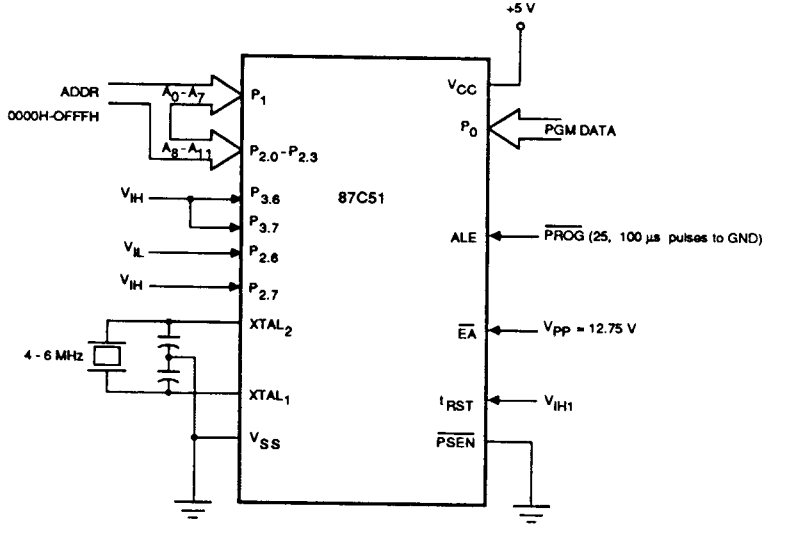


Figure 1. 87C51 Programming Configuration

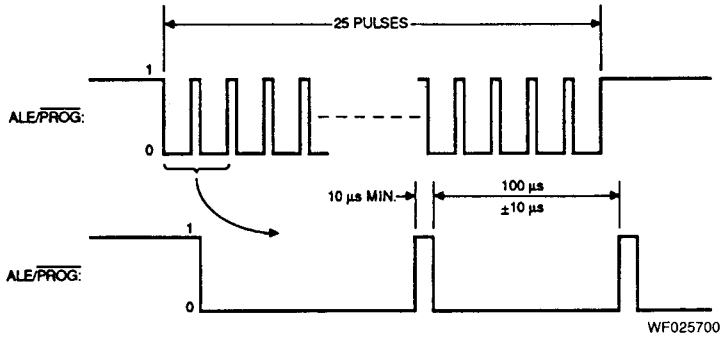


Figure 2. PROG Waveforms

Program Verification

The 87C51/87C52T2 provides a method of reading the programmed code bytes in the EPROM array for program verification. This function is possible as long as Lock Bit 2 has not been programmed.

For program verification, the address of the Program Memory location to be read is applied to Ports 1 and 2 as shown in Figure 3. Verification of the 87C52T2 is identical except that P2.4 is also used as an address input. Once RST, PSEN, Port 2, and Port 3 are held to the levels indicated, the contents of the addressed location will be emitted on Port 0. External pullups are required on Port 0 for this operation. The EPROM programming and verification waveforms provide further details.

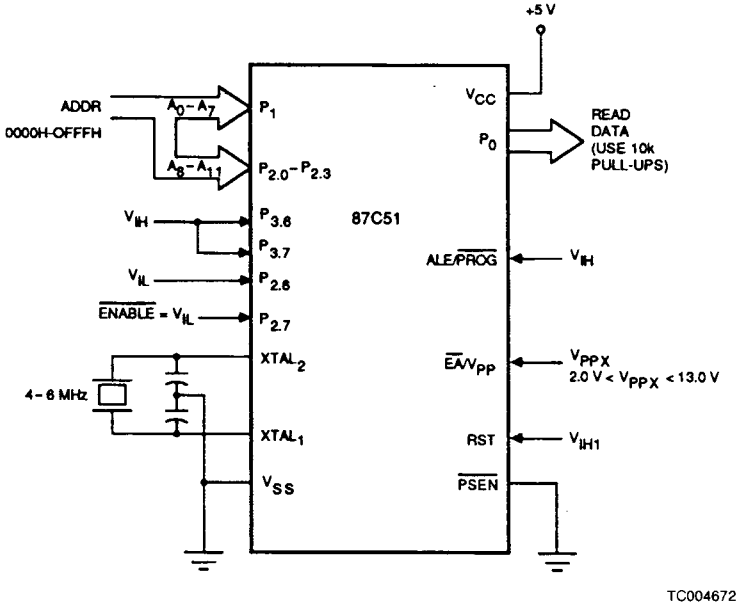


Figure 3. 87C51 Program Verification

Program Encryption Table

The 87C51/87C52T2 features a 32-byte Encryption Array. It can be programmed by the customer, thus encrypting the program code bytes read during EPROM verification. The EPROM verification procedure is performed as usual except that each code byte comes out logically X-NORed with one of the 32 key bytes.

The key byte used is the one whose address corresponds to the lower 5 bits of the EPROM verification address. Thus, when the EPROM is verified starting with address 0000H, all 32 keys in their correct sequence must be known. Unprogrammed bytes have the value FFH. Thus, if the Encryption Table is left unprogrammed, no encryption will be performed, since any byte X-NORed with FFH leaves that byte unchanged.

To program the Encryption Table, programming is set up as usual, except that P3.6 is held Low, as shown in Table 1. The 25-pulse programming sequence is applied to each address, 00 through 1FH. The programming of these bytes does not affect the standard 4K-byte EPROM array. When the Encryption Table is programmed, the Program Verify operation will produce only encrypted data.

The Encryption Table cannot be directly read. The programming of Lock Bit 1 will disable further Encryption Table programming.

Security Lock Bits

The 87C51 contains two Lock Bits which can be programmed to obtain additional security features. P = Programmed and U = Unprogrammed.

Lock Bit 1	Lock Bit 2	Result
U	U	Normal Operation
P	U	• Externally fetched code cannot access internal Program Memory • All further Programming disabled (except Lock Bit 2)
U	P	Reserved
P	P	• Externally fetched code cannot access internal Program Memory • All further Programming disabled • Program Verification disabled

To program the Lock Bits, a 100 pulse programming sequence is required using the levels shown in Table 1. After Lock Bit 1 is programmed, further programming of the Code Memory and Encryption Table is disabled. However, Lock Bit 2 may still be programmed, providing the highest level of security available on the 87C51/87C52T2.

When Lock Bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Silicon Signature Verification

AMD supports silicon signature verification for the 87C51/87C52T2. The manufacturer code and part code can be read from the device before any programming is done to enable the EPROM Programmer to recognize the device.

To read the silicon signature, the external pins are set up as shown in Figure 4. This procedure is the same as a normal verification except that P3.6 and P3.7 are pulled to a logic Low. The values returned are:

Manufacturer Code	Address: 0030H	Code: 01H
87C51 Part Code	Address: 0031H	Code: B0H
87C52T2 Part Code	Address: 0031H	Code: 31H

Code 01H indicates AMD as the manufacturer. Code B0H indicates the device type is the 87C51, and Code 31H indicates a 87C52T2.

In-Circuit Test Mode

The In-Circuit Test Mode facilitates testing and debugging of systems using the 87C51 without the 87C51 having to be removed from the circuit. The In-Circuit Test Mode is invoked by:

1. Pulling ALE Low while RST is held High, and $\overline{PSEN}$ is High.

2. Holding ALE Low as RST is de-activated.

While the device is in In-Circuit Test Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled High. The oscillator circuit remains active. While the 87C51 is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a Hardware Reset is applied.

Erasure Characteristics

Light and other forms of electromagnetic radiation can lead to erasure of the EPROM when exposed for extended periods of time.

Wavelengths of light shorter than 4000 angstroms, such as sunlight or indoor fluorescent lighting, can ultimately cause inadvertent erasure and should, therefore, not be allowed to expose the EPROM for lengthy durations (approximately one week in sunlight or three years in room-level fluorescent lighting). It is suggested that the window be covered with an opaque label if an application is likely to subject the device to this type of radiation.

It is recommended that ultraviolet light (of 2537 angstroms) be used to a dose of at least 15 W-sec/cm^2 when erasing the EPROM. An ultraviolet lamp rated at 12,000 μW/cm^2 held one inch away for 20–30 minutes should be sufficient.

EPROM erasure leaves the Program Memory in an "all ones" state.

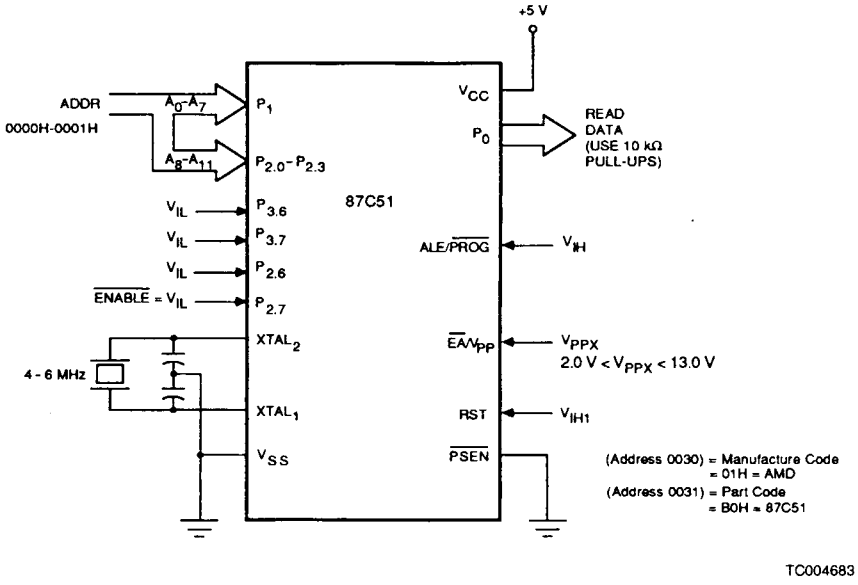


Figure 4. 87C51 Silicon Signature Verification Configuration

Oscillator Characteristics

$XTAL_1$ and $XTAL_2$ are the input and output, respectively, of an inverting amplifier which is configured for use as an on-chip oscillator (see Figure 5). Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, $XTAL_1$ should be driven while $XTAL_2$ is left unconnected (see Figure 6). There are no requirements on the duty cycle of the external clock signal since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum High and Low times specified on the data sheet must be observed.

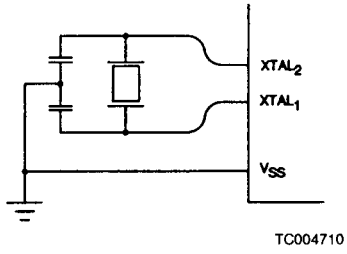


Figure 5. Crystal Oscillator

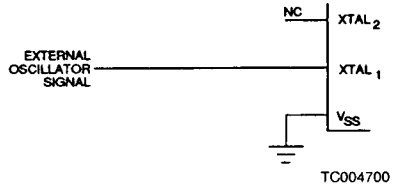


Figure 6. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on $\overline{EA}$/V_{PP} Pin to V_{SS} ..... −0.5 to +13.0 V
Voltage on V_{CC} to V_{SS} ..... −0.5 to +6.5 V
Voltage on Any Other Pin to V_{SS} ..... −0.5 to +6.5 V
Power Dissipation ..... 200 mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Industrial (I) Devices
Ambient Temperature (T_A) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage (Except $\overline{EA}$)		−0.5	0.2 V_{CC} − 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		0	0.2 V_{CC} − 0.3	V
V_{IH}	Input High Voltage (Except $XTAL_1$, RST)		0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage to $XTAL_1$, RST		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)	I_{OL} = 1.6 mA (Note 1)		0.45	V
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA (Note 1)		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3), ALE, $\overline{PSEN}$	I_{OH} = −60 µA, V_{CC} = 5 V ±10%	2.4		V
		I_{OH} = −10 µA	0.9 V_{CC}		
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = −800 µA, V_{CC} = 5 V ±10%	2.4		V
		I_{OH} = −80 µA (Note 2)			
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45 V		−50	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)	(Note 3)		−650	µA
I_{LI}	Input Leakage Current (Port 0)	V_{IN} = V_{IL} or V_{IH}		±10	µA
I_{CC}	Power Supply Current: Active Mode @ 12 MHz (Note 4)	(Note 5)		Note 4	mA
	Idle Mode @ 12 MHz (Note 4)			Note 4	
	Power-Down Mode			50	µA
RRST	Reset Pulldown Resistor		50	300	kΩ
C_{IO}	Pin Capacitance	Test Freq = 1 MHz, T_A = 25°C		10	pF

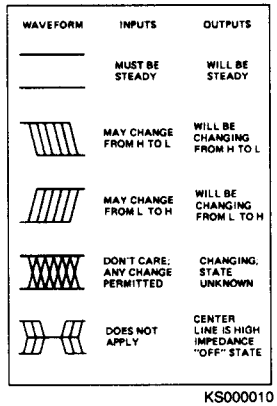
Notes:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.
3. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V.
4. I_{CCMAX} at other frequencies is given by:
   Active Mode: I_{CC} TYPICAL = 0.94 x Freq + 13.71 I_{CC} MAX = 1.38 x Freq + 20.4
   Idle Mode: I_{CC} TYPICAL = 0.38 x Freq + 5.4 I_{CC} MAX = 0.38 x Freq + 11.9
   where Freq is the external oscillator frequency in MHz. I_{CCMAX} is given in mA (see Figure 5).
5. Active Mode I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; $XTAL_2$ N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}.
   Idle Mode I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; $XTAL_2$ = N.C.; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS}.
   Power-Down Mode I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = Port 0 = V_{CC}; $XTAL_2$ NC; RST = V_{SS}.

SWITCHING CHARACTERISTICS over operating ranges
(Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

Parameter Symbol	Parameter Description	16 MHz Osc.		12 MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
1/TCLCL	Oscillator Frequency					3.5	16	MHz
TLHLL	ALE Pulse Width	85		127		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	7		28		TCLCL-55		ns
TLLAX	Address Hold After ALE Low	27		48		TCLCL-35		ns
TLLIV	ALE Low to Valid Instr. In		150		234		4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	22		43		TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	142		205		3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr. In		83		145		3TCLCL-105	ns
TPXIX	Input Instr. Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instr. Float After $\overline{PSEN}$		38		59		TCLCL-25	ns
TAVIV	Address to Valid Instr. In		208		312		5TCLCL-105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	275		400		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	275		400		6TCLCL-100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		148		252		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		55		97		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		350		517		8TCLCL-150	ns
TAVDV	Address to Valid Data In		398		585		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	137	238	200	300	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	120		203		4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	2		23		TCLCL-60		ns
TQVWH	Data Valid to $\overline{WR}$ High	287		433		7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	12		33		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	22	103	43	123	TCLCL-40	TCLCL+40	ns

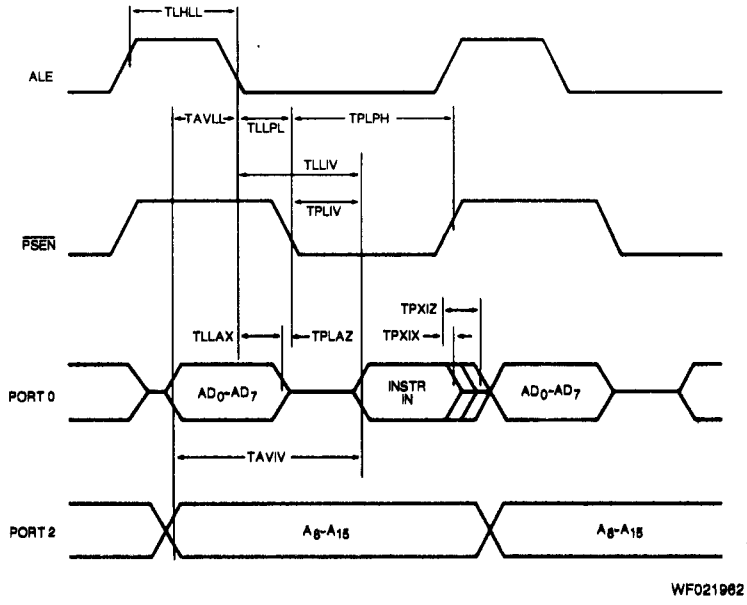
SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

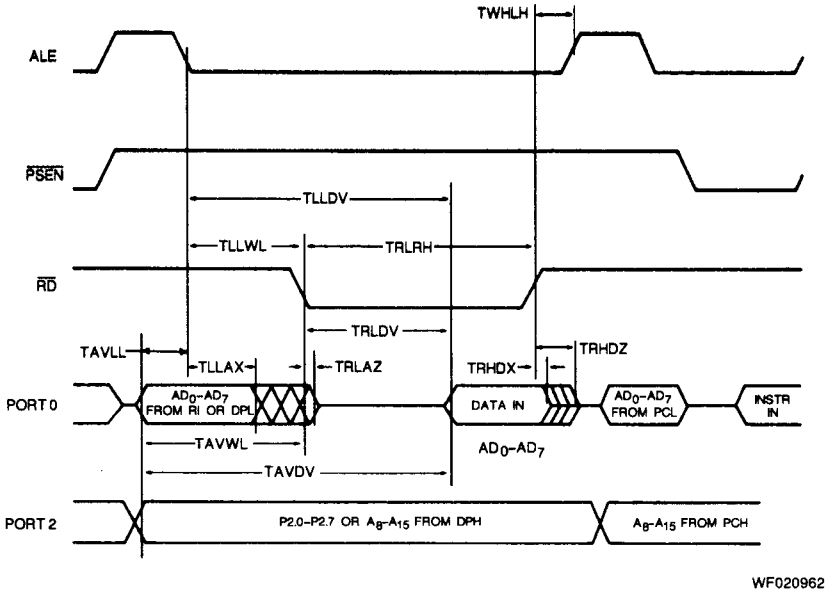


KS000010

SWITCHING WAVEFORMS

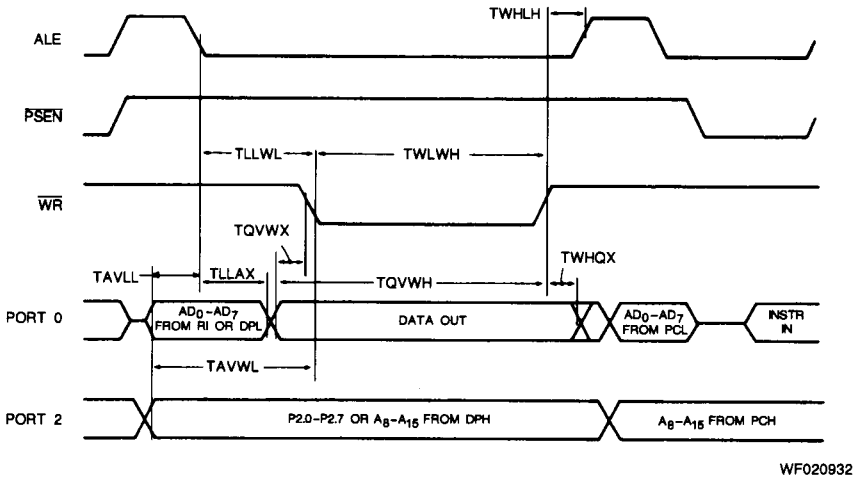


External Program Memory Read Cycle



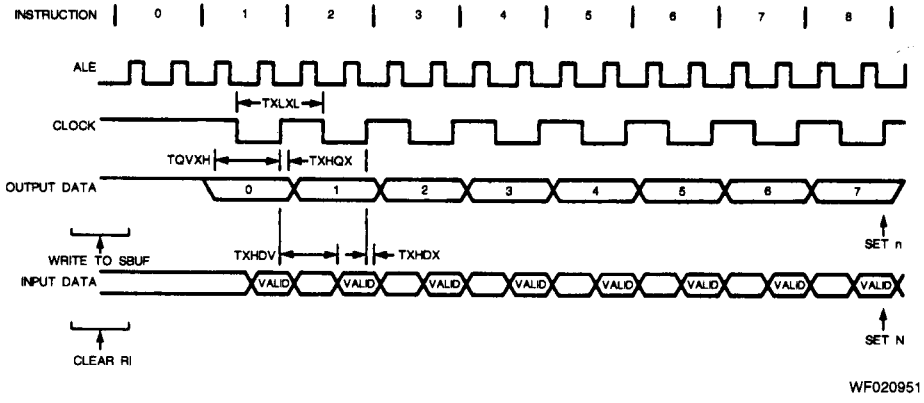
External Data Memory Read Cycle

SWITCHING WAVEFORMS (continued)



WF020932

External Data Memory Write Cycle

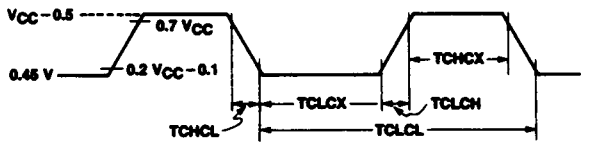


WF020951

Shift Register Timing Waveforms

EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Unit
1/TCLCL	Oscillator Frequency		16	MHz
TCHCX	High Time			ns
TCLCX	Low Time			ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



WF020910

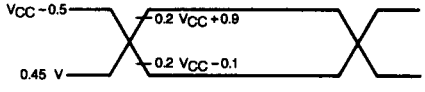
External Clock Drive Waveform

SERIAL PORT TIMING — SHIFT REGISTER MODE

(Test Conditions: T_A = 0 to +70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V; Load Capacitance = 80 pF)

Parameter Symbol	Parameter Description	16 MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	
TXLXL	Serial Port Clock Cycle Time	750		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	492		10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	8		2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		492		10TCLCL-133	ns

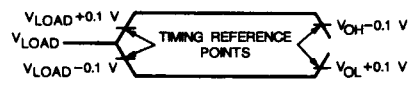
AC Testing



WF020901

AC inputs during testing are driven at V_{CC} - 0.5 for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Input/Output Waveform



WF020941

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

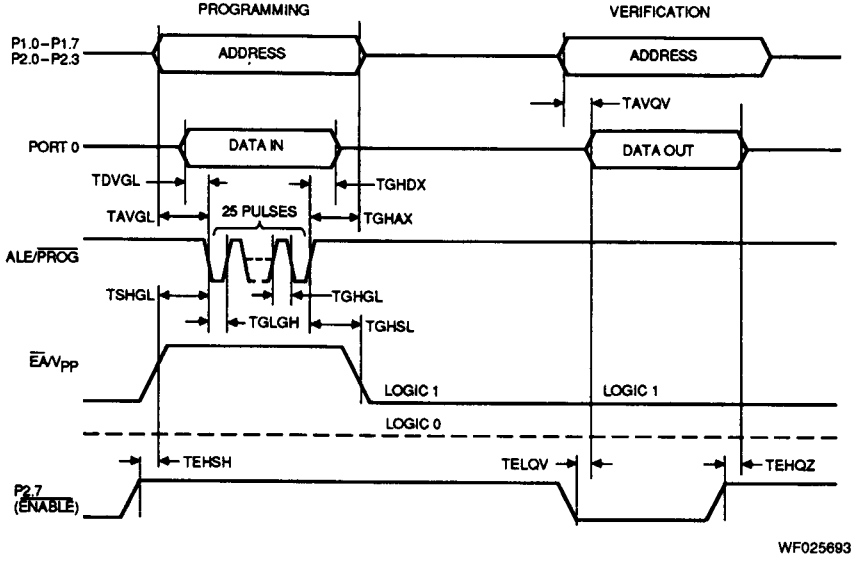
Float Waveform

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = +21 to +27°C)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		50	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



WF025693

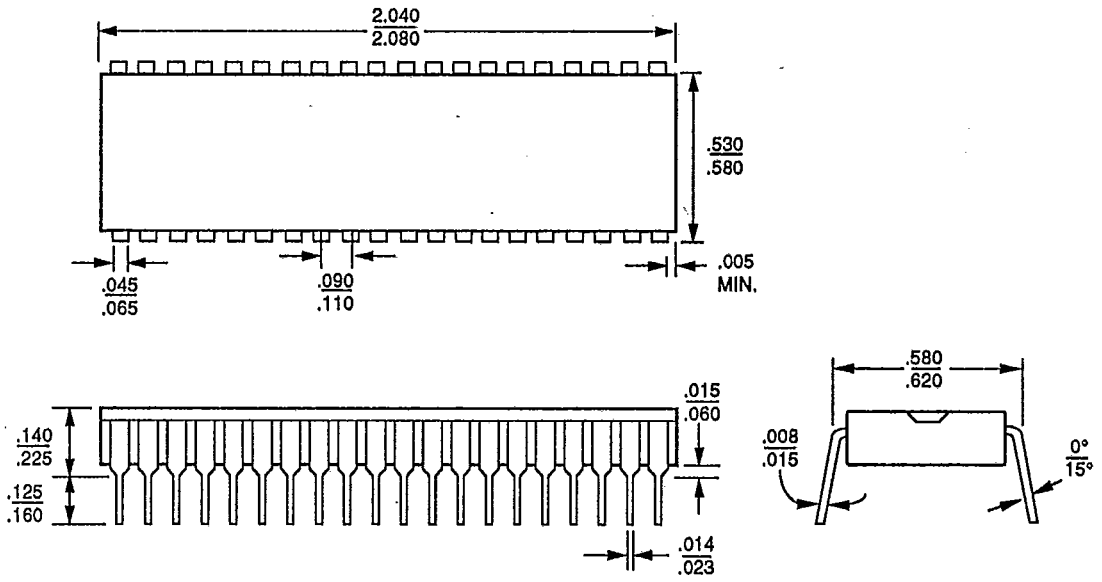
For Programming conditions, see Figures 1 and 2.
For Verification conditions, see Figure 3.

CHAPTER 11 T-90-20

Package Outlines

PHYSICAL DIMENSIONS*

Plastic Dual-In-Line Package (PD)
PD 040



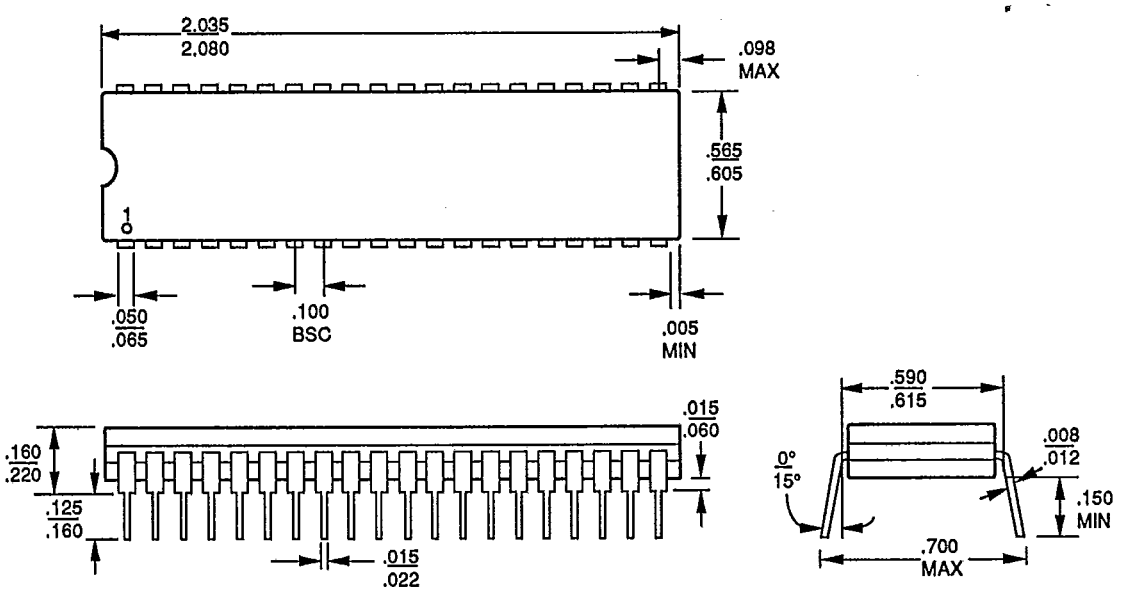
PID# 06823B

* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

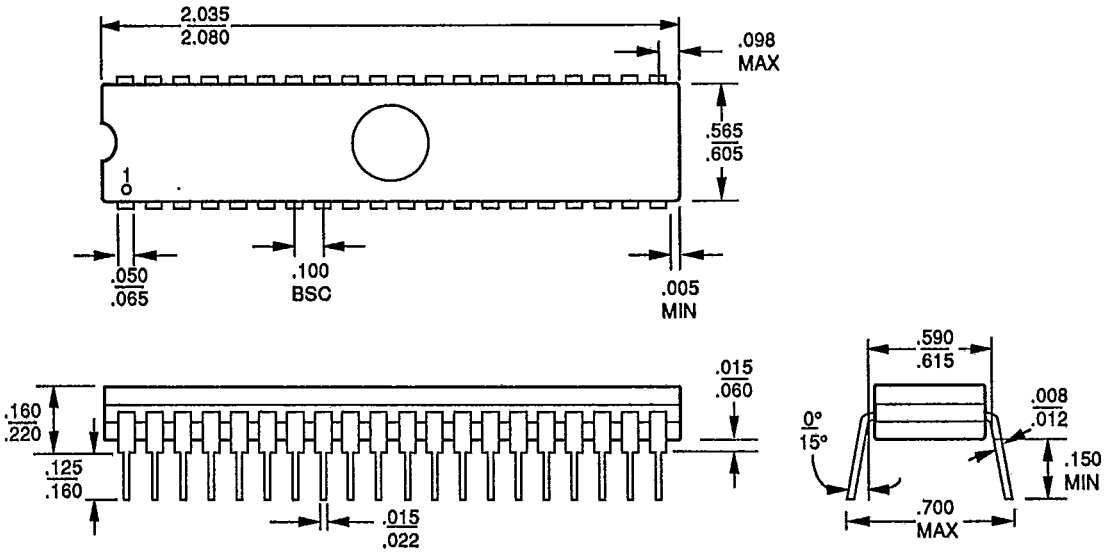
Ceramic Hermetic Dual-In-Line Packages (CD/CDV)

CD 040



06824C

CDV 040

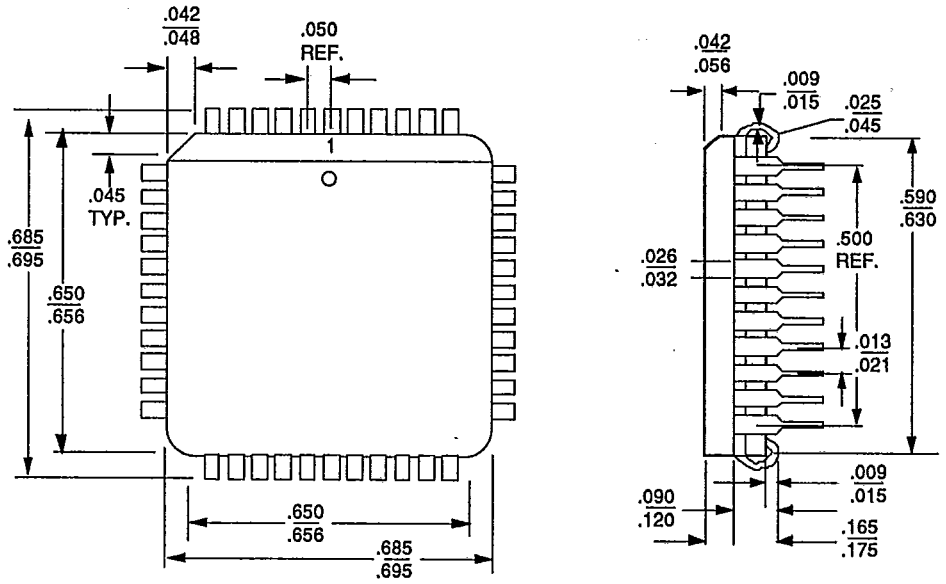


07880C

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

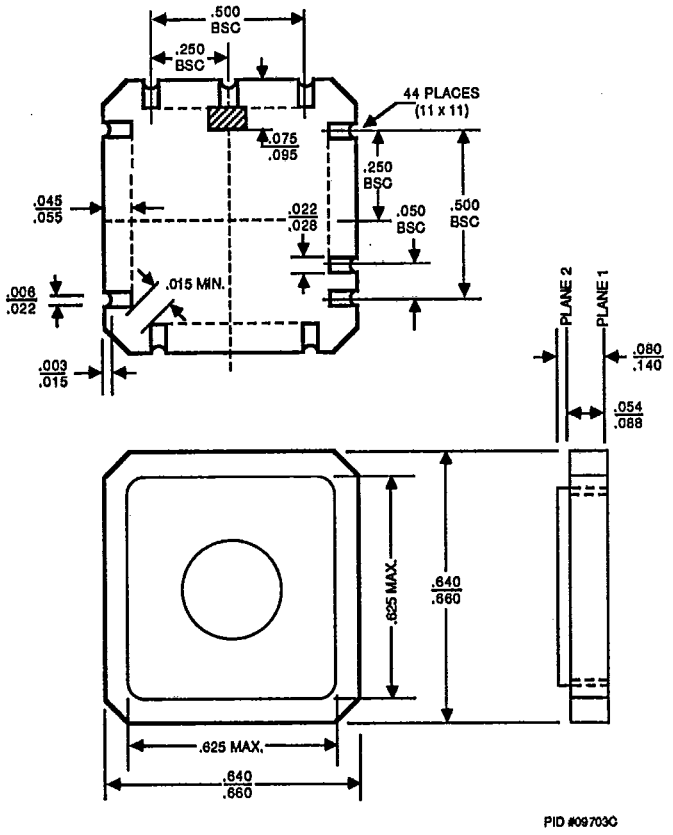
Plastic Leaded Chip Carriers (PL)
PL 044

T-90-20



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

Ceramic Leadless Chip Carrier (CLV)
CLV 044



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.