DDR4 SDRAM UDIMM Addendum

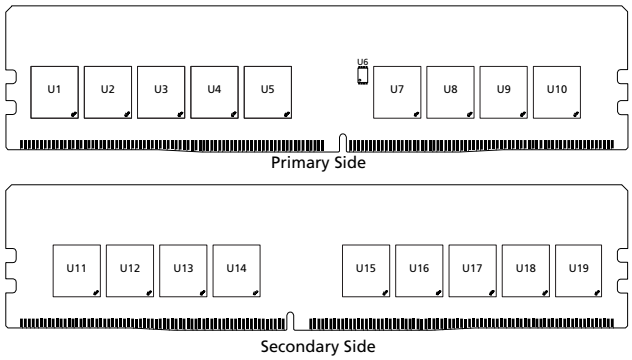
MTA18ASF4G72AZ – 32GB

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR4 UDIMM Core data sheet.

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC4-2666, PC4-3200
- 32GB (4 Gig x 72)
- Supports ECC error detection and correction
- Data bus inversion (DBI) for data bus
- Dual-rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 4 internal device bank groups with 4 banks per group produce 16 device banks

Figure 1: 288-Pin UDIMM (R/C-E1)



Options	Marking
• Operating temperature	
– Commercial ($0°C \le T_{OPER} \le 95°C$)	None
• Package	
– 288-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.625ns @ CL = 22 (DDR4-3200)	-3G2
– 0.75ns @ CL= 19 (DDR4-2666)	-2G6

Table 1: Addressing

Parameter	32GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	2 CS_n[1:0]

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT40A2G8,[1] 16Gb DDR4 SDRAM.

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)
MTA18ASF4G72AZ-3G2__	32GB	4 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA18ASF4G72AZ-2G6__	32GB	4 Gig x 72	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

Notes: 1. The data sheet for the base device can be found at micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA18ASF4G72AZ-3G2F1.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3	157	U2	0	10	23
	1	0	5		1	9	161
	2	2	12		2	11	168
	3	1	150		3	8	16
	4	7	155		4	14	21
	5	4	3		5	13	159
	6	6	10		6	15	166
	7	5	148		7	12	14
U3	0	18	34	U4	0	26	45
	1	17	172		1	24	38
	2	19	179		2	27	190
	3	16	27		3	25	183
	4	22	32		4	31	188
	5	21	170		5	28	36
	6	23	177		6	30	43
	7	20	25		7	29	181
U5	0	CB2	56	U7	0	34	104
	1	CB1	194		1	32	97
	2	CB3	201		2	35	249
	3	CB0	49		3	33	242
	4	CB6	54		4	38	102
	5	CB5	192		5	37	240
	6	CB7	199		6	39	247
	7	CB4	47		7	36	95
U8	0	42	115	U9	0	50	126
	1	40	108		1	48	119
	2	43	260		2	51	271
	3	41	253		3	49	264
	4	47	258		4	54	124
	5	44	106		5	53	262
	6	46	113		6	55	269
	7	45	251		7	52	117

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	58	137	U11	0	57	257
	1	57	275		1	58	137
	2	59	282		2	56	130
	3	56	130		3	59	282
	4	63	280		4	61	273
	5	61	273		5	63	280
	6	62	135		6	60	128
	7	60	128		7	62	135
U12	0	48	119	U13	0	40	108
	1	50	126		1	42	115
	2	49	264		2	41	253
	3	51	271		3	43	260
	4	53	262		4	44	106
	5	54	124		5	47	258
	6	52	117		6	45	251
	7	55	269		7	46	113
U14	0	32	97	U15	0	CB1	194
	1	34	104		1	CB2	56
	2	33	242		2	CB0	49
	3	35	249		3	CB3	201
	4	37	240		4	CB5	192
	5	38	102		5	CB6	54
	6	36	95		6	CB4	47
	7	39	247		7	CB7	199
U16	0	24	38	U17	0	17	172
	1	26	45		1	18	34
	2	25	183		2	16	27
	3	27	190		3	19	179
	4	28	36		4	21	170
	5	31	188		5	22	32
	6	29	181		6	20	25
	7	30	43		7	23	177
U18	0	9	161	U19	0	0	5
	1	10	23		1	3	157
	2	8	16		2	1	150
	3	11	168		3	2	12
	4	13	159		4	4	3
	5	14	21		5	7	155
	6	12	14		6	5	148
	7	15	166		7	6	10

I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions – 32GB (Die Revision B)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet.

Parameter	Symbol	3200	2666	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	954	936	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{PP0}[1]	63	63	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}[1]	1053	1035	mA
Precharge standby current	I_{DD2N}[2]	936	900	mA
Precharge standby ODT current	I_{DD2NT}[1]	891	873	mA
Precharge power-down current	I_{DD2P}[2]	774	774	mA
Precharge quite standby current	I_{DD2Q}[2]	846	846	mA
Active standby current	I_{DD3N}[2]	1440	1404	mA
Active standby I_{PP} current	I_{PP3N}[2]	54	54	mA
Active power-down current	I_{DD3P}[2]	1242	1224	mA
Burst read current	I_{DD4R}[1]	2205	2025	mA
Burst write current	I_{DD4W}[1]	2034	1881	mA
Different logic rank burst refresh current (1x REF)	I_{DD5R}[1]	1098	1080	mA
Different logic rank burst refresh I_{PP} current (1x REF)	I_{PP5R}[1]	72	72	mA
Self refresh current: Normal temperature range (0°C to 85°C)	$I_{DD6N\ (0–85°C)}$[2]	1206	1206	mA
Self refresh current: Extended temperature range (0°C to 95°C)	$I_{DD6E\ (0–95°C)}$[2]	2178	2178	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	$I_{DD6R\ (0–45°C)}$[2]	522	522	mA
Auto self refresh current (25°C)	$I_{DD6A\ (25°C)}$[2]	180	180	mA
Auto self refresh current (45°C)	$I_{DD6A\ (45°C)}$[2]	522	522	mA
Auto self refresh current (75°C)	$I_{DD6A\ (75°C)}$[2]	1098	1098	mA
Auto self refresh current (95°C)	$I_{DD6A\ (95°C)}$[2]	2178	2178	mA
Auto self refresh I_{PP} current (0°C to 95°C)	I_{PP6X}[2]	198	198	mA
Bank interleave read current	I_{DD7}[1]	2151	2097	mA
Bank interleave read I_{PP} current	I_{PP7}[1]	117	117	mA
Maximum power-down current	I_{DD8}[2]	720	720	mA

Notes: 1. One module rank in the active $I_{DD/PP}$, the other rank in $I_{DD2P/PP3N}$.
2. All ranks in this $I_{DD/PP}$ condition.

Table 5: DDR4 I_{DD} Specifications and Conditions – 32GB (Die Revision F)

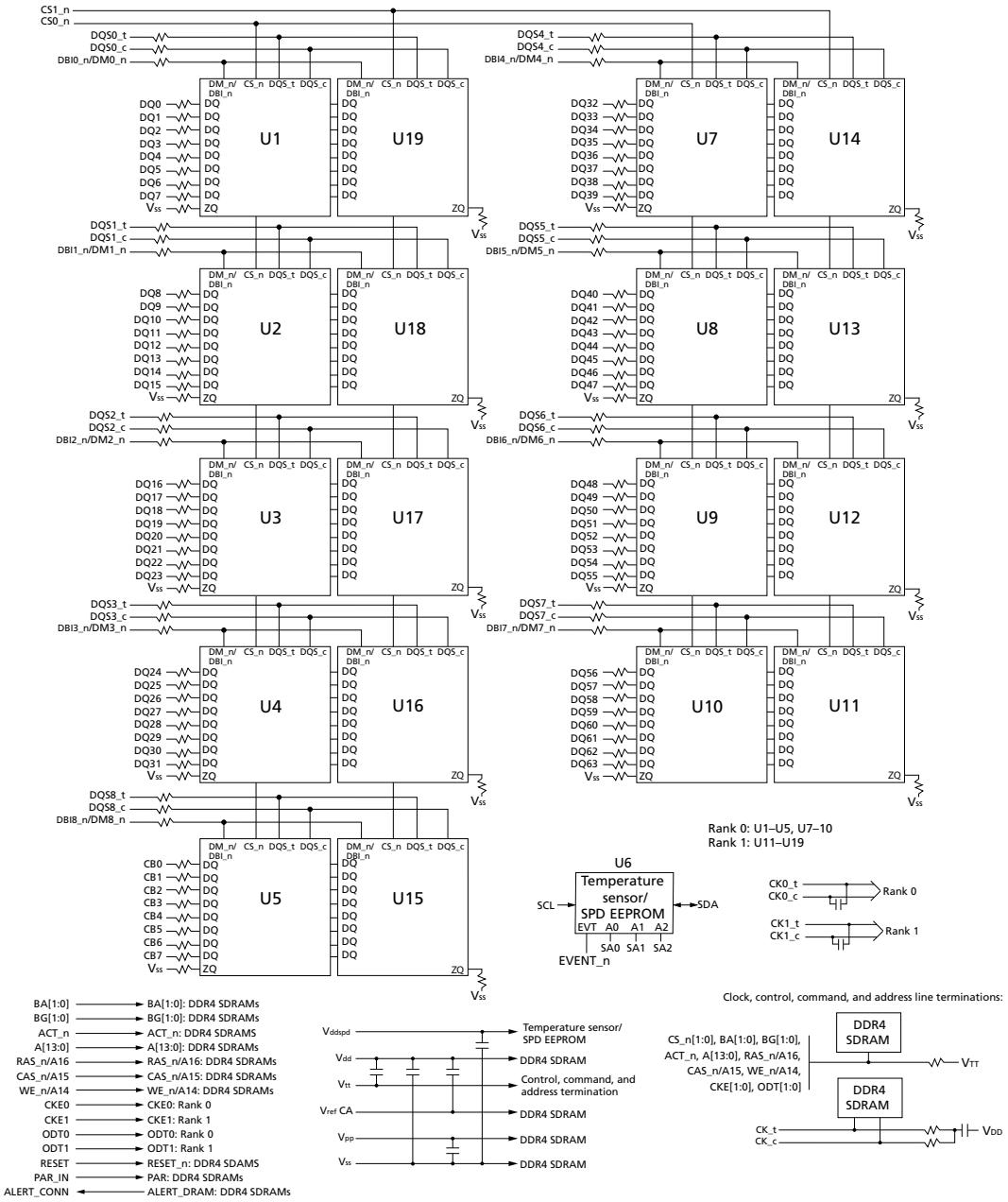
Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet.

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	882	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{PP0}[1]	45	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}[1]	981	mA
Precharge standby current	I_{DD2N}[2]	810	mA
Precharge standby ODT current	I_{DD2NT}[1]	801	mA
Precharge power-down current	I_{DD2P}[2]	684	mA
Precharge quite standby current	I_{DD2Q}[2]	756	mA
Active standby current	I_{DD3N}[2]	1098	mA
Active standby I_{PP} current	I_{PP3N}[2]	36	mA
Active power-down current	I_{DD3P}[2]	900	mA
Burst read current	I_{DD4R}[1]	1602	mA
Burst write current	I_{DD4W}[1]	1350	mA
Different logic rank burst refresh current (1x REF)	I_{DD5R}[1]	954	mA
Different logic rank burst refresh I_{PP} current (1x REF)	I_{PP5R}[1]	54	mA
Self refresh current: Normal temperature range (0°C to 85°C)	$I_{DD6N\ (0–85°C)}$[2]	954	mA
Self refresh current: Extended temperature range (0°C to 95°C)	$I_{DD6E\ (0–95°C)}$[2]	1620	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	$I_{DD6R\ (0–45°C)}$[2]	360	mA
Auto self refresh current (25°C)	$I_{DD6A\ (25°C)}$[2]	198	mA
Auto self refresh current (45°C)	$I_{DD6A\ (45°C)}$[2]	360	mA
Auto self refresh current (75°C)	$I_{DD6A\ (75°C)}$[2]	198	mA
Auto self refresh current (95°C)	$I_{DD6A\ (95°C)}$[2]	360	mA
Auto self refresh I_{PP} current (0°C to 95°C)	I_{PP6X}[2]	918	mA
Bank interleave read current	I_{DD7}[1]	1620	mA
Bank interleave read I_{PP} current	I_{PP7}[1]	108	mA
Maximum power-down current	I_{DD8}[2]	1845	mA

Notes: 1. One module rank in the active $I_{DD/PP}$, the other rank in $I_{DD2P/PP3N}$.
2. All ranks in this $I_{DD/PP}$ condition.

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.