19-3900; Rev 1; 8/11

EVALUATION KIT AVAILABLE

+5V Multiprotocol, Software-Selectable Clock Transceiver

General Description

The MAX13172E is a four-driver/four-receiver multiprotocol transceiver that operates from a single +5V supply in conjunction with the MAX13170E and MAX13174E. The MAX13172E, along with the MAX13170E and the MAX13174E, form a complete software-selectable data terminal equipment (DTE) or data communication equipment (DCE) interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21, RS-423), and V.35 protocols. The MAX13172E transceiver carries serial-interface control signaling, while the MAX13170E carries the high-speed clock and data signals. Typically, the MAX13170E is terminated using the MAX13174E.

The MAX13172E is available in a 5.3mm x 10.2mm, 28-pin SSOP package and operates over the 0°C to +70°C commercial temperature range.

Applications

Data Networking

CSU/DSU Devices

Data Routers

Switches

PCI Cards

Telecommunication Equipment

Pin Configuration appears at end of data sheet.

Features

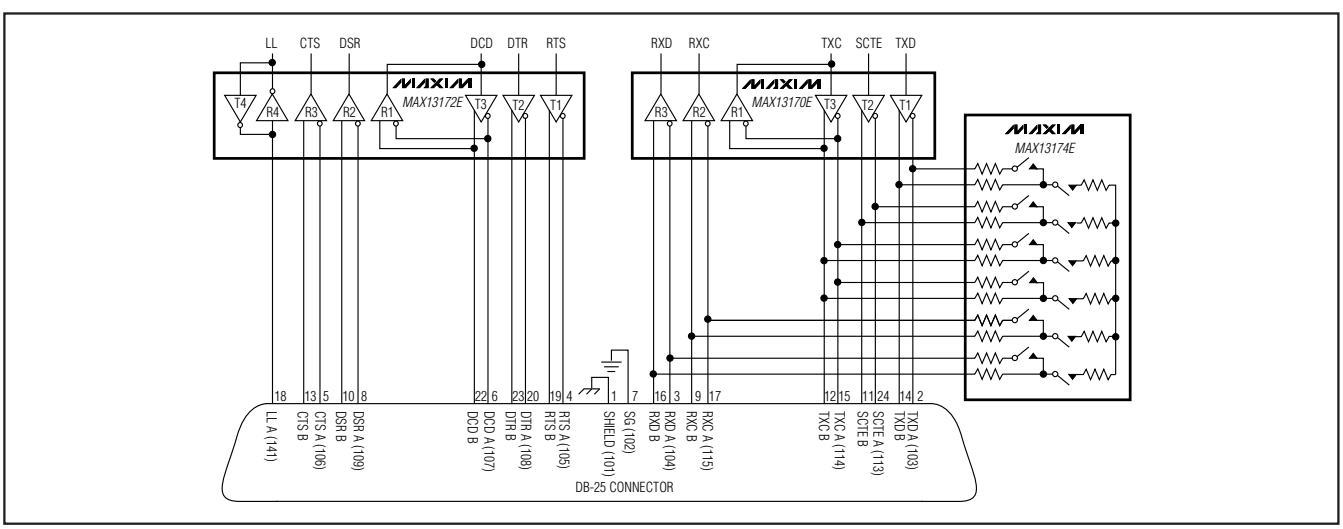
- **The MAX13170E/MAX13172E/MAX13174E Chipset is a Pin-for-Pin Upgrade to the MXL1544/MAX3175/MXL1543/MXL1543B Chipset**
- **Chipset Operates from a Single +5V Supply**
- **Software-Selectable DCE/DTE Configurations**
- **Supports V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21, RS-423) Protocols**
- **Flowthrough Pin Configuration**
- **Fail-Safe Receivers While Maintaining V.11 and V.35 Compatibility**
- **Extremely Low Maximum Shutdown Current (No-Cable Mode)**
- **TUV-Certified NET1/NET2 and TBR1/TBR2 Compliant (Pending)**
- **Extended ESD Protection for All Transmitter Outputs and Receivers Inputs to GND**
  - **±10kV Using the Human Body Model**
  - **±3kV Using the Contact Method Specified in IEC 61000-4-2**
  - **±3kV Using the Air Gap Discharge Method Specified in IEC 61000-4-2**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX13172ECAI+	0°C to +70°C	28 SSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



+5V Multiprotocol, Software-Selectable Clock Transceiver

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
Supply Voltages
- V_{CC} ..... -0.3V to +6V
- V_{DD} ..... -0.3V to +7.1V
- V_{EE} ..... +0.3V to -7.1V
- V_{DD} to V_{CC} ..... +0.3 to +6V

Logic Input Voltages
- M0, M1, M2, DCE/$\overline{DTE}$, T_IN, INVERT ..... -0.3V to +6V

Logic Output Voltages
- R_OUT ..... -0.3V to (V_{CC} + 0.3V)

Transmitter Outputs
- T_OUT_, T_OUT_/R_IN_ (No-Cable Mode, V.28 only) ..... -15V to +15V
- Short-Circuit Duration to GND ..... Continuous

Receiver Inputs
- R_IN_, T_OUT_/R_IN_ ..... -15V to +15V
- R_INA to R_INB, T3OUTA/R1INA to T3OUT/R1INB ..... -15V to +15V

Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP
- Single-Layer Board (derate 9.5mW/°C above +70°C) 762mW
- Multi-Layer Board (derate 14.9mW/°C above +70°C) 1194mW

Operating Temperature Range ..... 0°C to 70°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SSOP
- Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... +67°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) ..... +25°C/W

Note 1: Package thermal resistances were obtained using the method described in JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C, V.28 mode only: V_{DD} = +5.6V to +7.1V and V_{EE} = -7.1V to -5.4V. Typical values are at V_{DD} = +6.9V and V_{EE} = -6.7V, no-cable mode: V_{DD} = V_{CC} and V_{EE} = 0V, other modes: V_{DD} = +5.15V to +5.7V and V_{EE} = -4.84V to -4.16V. Typical value are at V_{DD} = +5.3V and V_{EE} = -4.5V.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Operating Range	V_{CC}		4.5		5.5	V
V_{DD} Operating Range	V_{DD}	V.28 mode	5.6		7.1	V
		V.10 or V.11 mode	5.15		5.7	
V_{EE} Operating Range	V_{EE}	V.28 mode	-7.1		-5.4	V
		V.10 or V.11 mode	-4.84		-4.16	
V_{CC} Supply Current (DCE Mode) (Digital Inputs = GND or V_{CC}) (Transmitter Outputs Static)	I_{CC}	CH1, CH3 = V.11, CH2 = V.10, CH4 = V.10, no load		5.5		mA
		CH1, CH3 = V.11, CH2 = V.10, CH4 = V.10, full load		95	135	
		CH1, CH2, CH3 = V.11, CH4 = V.10, full load		138	180	
		V.28 mode		3.5	9	
		No cable mode; M0, M1, M2, DCE/$\overline{DTE}$, INVERT, open or at V_{CC} (V_{DD} = V_{CC} and V_{EE} = GND)		0	10	µA
Internal Power Dissipation (DCE Mode)	P_D	CH1, CH3 = V.11, CH2, CH4 = V.10, no load		300		mW
		V.28 mode, full load		54		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C, V.28 mode only: V_{DD} = +5.6V to +7.1V and V_{EE} = -7.1V to -5.4V. Typical values are at V_{DD} = +6.9V and V_{EE} = -6.7V, no-cable mode: V_{DD} = V_{CC} and V_{EE} = 0V, other modes: V_{DD} = +5.15V to +5.7V and V_{EE} = -4.84V to -4.16V. Typical value are at V_{DD} = +5.3V and V_{EE} = -4.5V.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{EE} Supply Current	I_{EE}	CH1, CH3 = V.11, CH2 = V.10 or V.11, CH4 = V.10, no load		2.1		mA
		CH1, CH2, CH3 = V.11, CH4 = V.10, full load (output low)		13	30	
		CH1, CH3 = V.11, CH2, CH4 = V.10, full load (output low)		22	30	
		V.28 mode, no load		1		
		V.28 mode, full load (output low)		12	18	
		No cable mode (V_{DD} = V_{CC} and V_{EE} = GND)		0	10	µA
V_{DD} Supply Current	I_{DD}	CH1, CH3 = V.11, CH2 = V.10 or V.11, CH4 = V.10, no load		0.6		mA
		CH1, CH2, CH3 = V.11, CH4 = V.10, full load (output high)		11	30	
		CH1, CH3 = V.11, CH2, CH4 = V.10, full load (output high)		22	30	
		V.28 mode, no load		2.5		
		V.28 mode, full load (output high)		12	10	
		No cable mode (V_{DD} = V_{CC} and V_{EE} = GND)		0	10	µA
Thermal-Shutdown Protection	THSD			+145		°C
LOGIC INPUTS (M0, M1, M2, DCE/$\overline{DTE}$, INVERT, T1IN, T2IN, T3IN, T4IN)						
Input High Voltage	V_{IH}		0.66 x V_{CC}			V
Input Low Voltage	V_{IL}				0.33 x V_{CC}	V
Logic-Input Current	I_{IN}	T1IN, T2IN, T3IN, T4IN	-1		+1	µA
Pullup Resistor	R_{PUIN}	M0, M1, M2, DCE/$\overline{DTE}$, INVERT to V_{CC}	50	100	166	kΩ
LOGIC OUTPUTS (R1OUT, R2OUT, R3OUT, R4OUT)						
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	0.66 x V_{CC}			V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA			0.33 x V_{CC}	V
Output Pullup Resistor	R_{PUY}	No cable mode (to V_{CC})		71.4		kΩ
Transmitter Output Leakage Current	I_Z	-0.25V < V_{OUT} < +0.25V, V_{CC} = 0V or no cable mode		±1	±5	µA
V.11 TRANSMITTER						
Open-Circuit Differential Output Voltage	V_{ODO}	Open circuit, R = 1.95kΩ, Figure 1	- V_{CC}		+V_{CC}	V
Loaded Differential Output Voltage (Note 4)	$\lvert V_{ODL} \rvert$	R = 50Ω, Figure 1	0.5 x V_{ODO}			V
		R = 50Ω, Figure 1	2			
Change in Magnitude of Output Differential Voltage	ΔV_{OD}	R = 50Ω, Figure 1			0.2	V

+5V Multiprotocol, Software-Selectable Clock Transceiver

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C, V.28 mode only: V_{DD} = +5.6V to +7.1V and V_{EE} = -7.1V to -5.4V. Typical values are at V_{DD} = +6.9V and V_{EE} = -6.7V, no-cable mode: V_{DD} = V_{CC} and V_{EE} = 0V, other modes: V_{DD} = +5.15V to +5.7V and V_{EE} = -4.84V to -4.16V. Typical value are at V_{DD} = +5.3V and V_{EE} = -4.5V.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Output Voltage	V_{OC}	R = 50Ω, Figure 1			3.0	V
Change in Magnitude of Common-Mode Output Voltage	ΔV_{OC}	R = 50Ω, Figure 1			0.2	V
Short-Circuit Current	I_{SC}	V_{OUT} = V_{GND}			150	mA
Rise Time	t_R	Figures 2, 5		4	10	ns
Fall Time	t_F	Figures 2, 5		6	10	ns
Transmitter Input-to-Output Prop Delay	t_{PHL}, t_{PLH}	Figures 2, 5			22	ns
Data Skew	$\lvert t_{PHL}-t_{PLH}\rvert$	Figures 2, 5 (Note 5)			3	ns
Output-to-Output Skew	t_{SKEWT}	Figures 2, 5 (Notes 5, 6)			3	ns
V.11 RECEIVER						
Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ +7V	-200		-50	mV
Input Hysteresis	ΔV_{TH}	-7V ≤ V_{CM} ≤ +7V		15		mV
Receiver Input Current	I_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	-0.66		+0.66	mA
Receiver Input Resistance	R_{IN}	-10V ≤ $V_{A,B}$ ≤ +10V	15	30		kΩ
Rise or Fall Time	t_R, t_F	Figures 2, 6		3		ns
Receiver Input-to-Output Delay	t_{PHL}, t_{PLH}	Figures 2, 6		16	26	ns
Data Skew	$\lvert t_{PHL}-t_{PLH}\rvert$	Figures 2, 6 (Note 5)			3.5	ns
Output-to-Output Skew	t_{SKEWR}	(Notes 5, 6)			3.5	ns
V.10 TRANSMITTER						
Open-Circuit Output Voltage Swing (Figure 3)	V_O	R_L = 3.9kΩ (out high)	4		6	V
		R_L = 3.9kΩ (out low)	-6		-4	
Output Voltage Swing (Figure 3)	V_T	R_L = 450Ω (out high)	3.6			V
		R_L = 450Ω (out low)			-3.6	
		R_L = 450Ω	0.9 x $\lvert V_O\rvert$			
Short-Circuit Current	I_{SC}	V_O = V_{GND}	-55		+55	mA
Rise or Fall Time	t_R, t_F	R_L = 450Ω, C_L =100pF (Figure 7)		2		µs
Transmitter Input-to-Output Delay	t_{PLH}, t_{PHL}	R_L = 450Ω, C_L =100pF (Figure 7)		1		µs
V.10 RECEIVER						
Input Threshold Voltage	V_{TH}	Measured on inverting input (A)	50		250	mV
Input Hysteresis	ΔV_{TH}			25		mV
Receiver Input Current	I_{IN}	-10V ≤ V_A ≤ +10V	-0.66		+0.66	mA
Receiver Input Impedance	R_{IN}	-10V ≤ V_A ≤ +10V	15	30		kΩ
Rise or Fall Time	t_R, t_F	Figures 4, 8		3		ns
Receiver Input-to-Output Delay from Low to High	t_{PLH}	Figures 4, 8		55		ns
Receiver Input-to-Output Delay from High to Low	t_{PHL}	Figures 4, 8		109		ns
Data Skew	$\lvert t_{PHL}-t_{PLH}\rvert$	Figures 4, 8		60		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V, and T_A = +25°C, V.28 mode only: V_{DD} = +5.6V to +7.1V and V_{EE} = -7.1V to -5.4V. Typical values are at V_{DD} = +6.9V and V_{EE} = -6.7V, no-cable mode: V_{DD} = V_{CC} and V_{EE} = 0V, other modes: V_{DD} = +5.15V to +5.7V and V_{EE} = -4.84V to -4.16V. Typical value are at V_{DD} = +5.3V and V_{EE} = -4.5V.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V.28 TRANSMITTER							
Output-Voltage Swing	V_{OD}	Open circuit (output high)				V_{DD}	V
		Open circuit (output low)		V_{EE}			
		R_L = 3kΩ	Output high	+5	+6.8		
			Output low		-6.8	-5	
Short-Circuit Current	$\|I_{SC}\|$					85	mA
Output Slew Rate	$SR_{R/F}$	R_L = 3kΩ, C_L = 2500pF, Figures 3, 9		4		30	V/µs
Transmitter Input-to-Output Propagation Delay	t_{PHL}, t_{PLH}	R_L = 3kΩ, C_L = 2500pF, Figures 3, 9			1	2	µs
V.28 RECEIVER							
Input Threshold Low	V_{IL}			0.8			V
Input Threshold High	V_{IH}					2	V
Input Hysteresis	V_{Hyst}				0.25		V
Input Resistance	R_{IN}	-15V ≤ V_{IN} ≤ +15V		3	5	7	kΩ
Rise or Fall Time	t_R, t_F	Figures 4, 10			3		ns
Receiver Input-to-Output Delay	t_{PHL}, t_{PLH}	Figures 4, 10				150	ns
ESD PROTECTION (T_OUT_, T_OUT_/R_OUT_, R_IN_ to GND)							
ESD Protection		Contact Discharge IEC61000-4-2			±3		kV
		Air Gap Discharge IEC61000-4-2			±3		
		Human Body Model			±10		

Note 2: The MAX13172E is designed to operate with V_{DD} and V_{EE} supplied by the MAX13170E charge pump.

Note 3: All devices are 100% production tested at T_A = +25°C, and are guaranteed by design for T_A = 0°C to +70°C as specified.

Note 4: $|V_{ODL}|$ is guaranteed at both 0.5 x V_{ODO} and 2V.

Note 5: Guaranteed by design, not production tested.

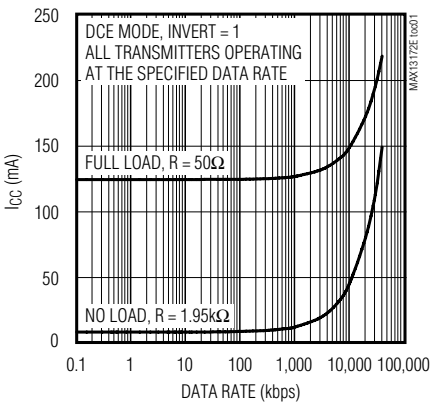
Note 6: Ouput-to-output skews are evaluated as a difference of propagation delays between different channels in the same condtion and for the same polarity (LH or HL).

+5V Multiprotocol, Software-Selectable Clock Transceiver

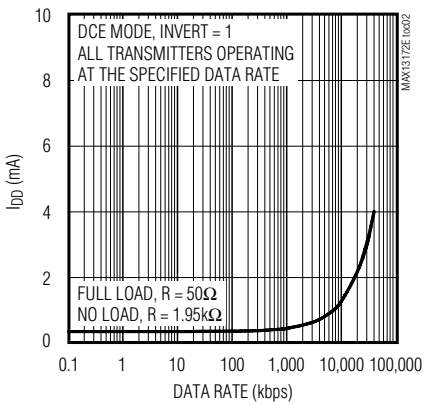
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

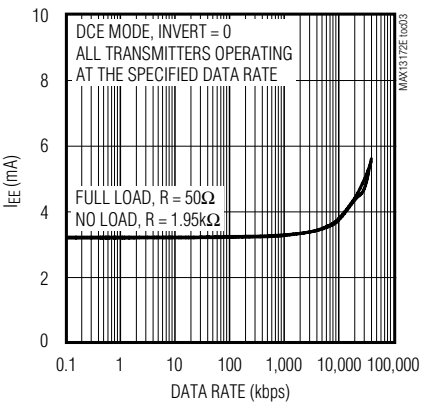
V.11 MODE SUPPLY CURRENT (I_{CC}) vs. DATA RATE



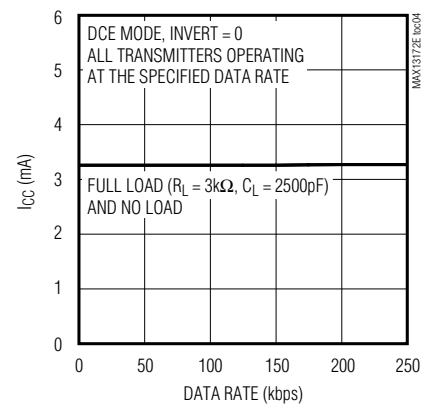
V.11 MODE SUPPLY CURRENT (I_{DD}) vs. DATA RATE



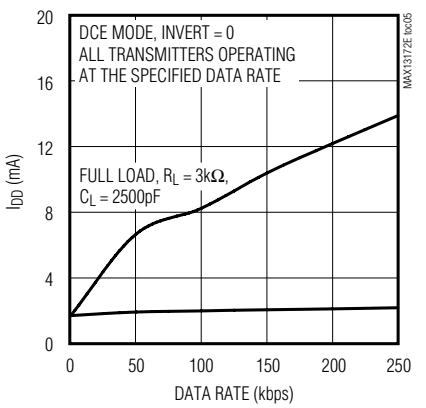
V.11 MODE SUPPLY CURRENT (I_{EE}) vs. DATA RATE



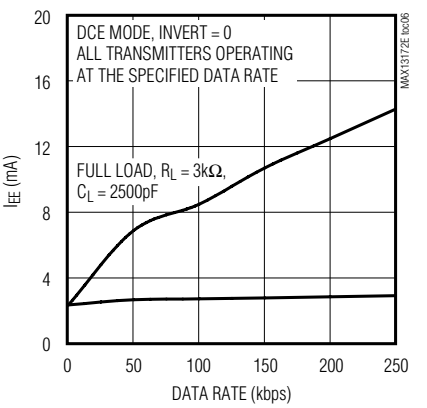
V.28 MODE SUPPLY CURRENT (I_{CC}) vs. DATA RATE



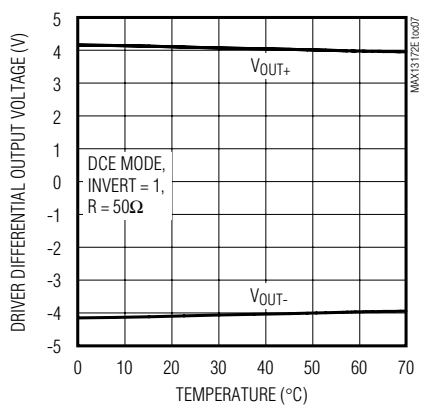
V.28 MODE SUPPLY CURRENT (I_{DD}) vs. DATA RATE



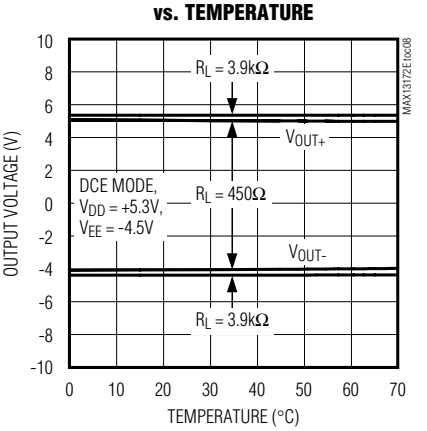
V.28 MODE SUPPLY CURRENT (I_{EE}) vs. DATA RATE



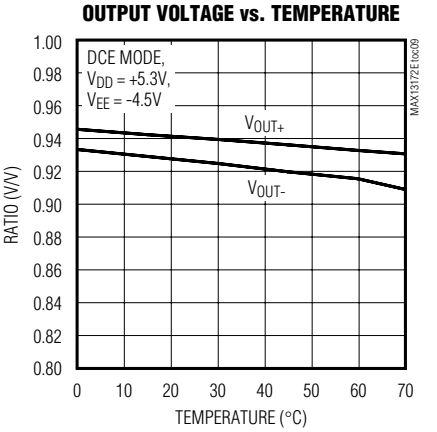
V.11 LOADED DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



V.10 OUTPUT VOLTAGE vs. TEMPERATURE



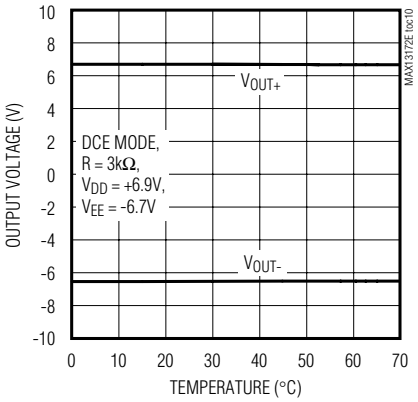
V.10 RATIO OF LOADED/UNLOADED OUTPUT VOLTAGE vs. TEMPERATURE



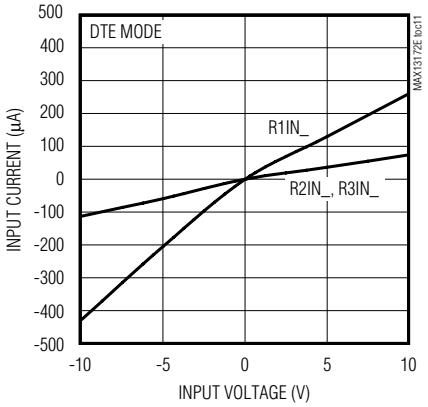
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

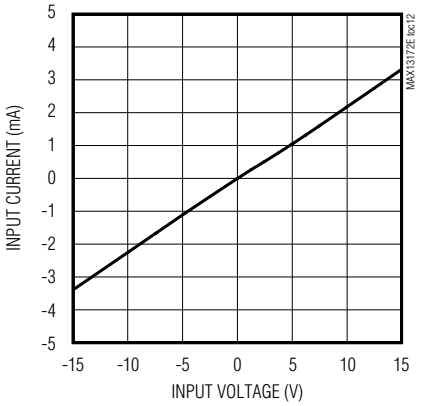
V.28 LOADED OUTPUT VOLTAGE vs. TEMPERATURE



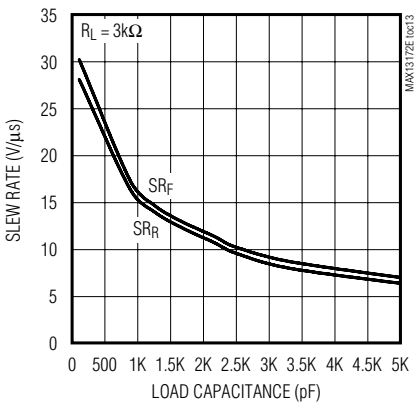
V.11 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



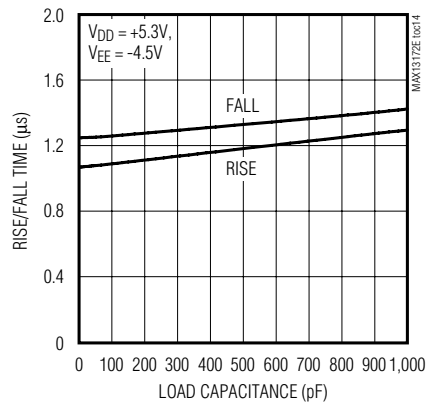
V.28 RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



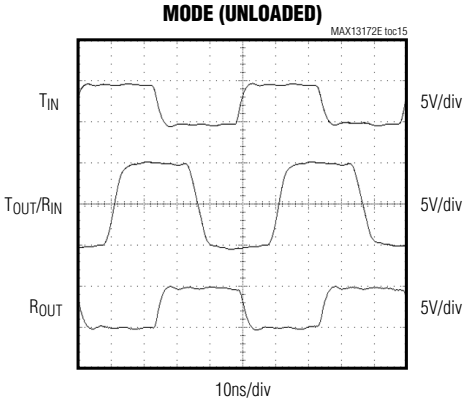
V.28 SLEW RATE vs. LOAD CAPACITANCE



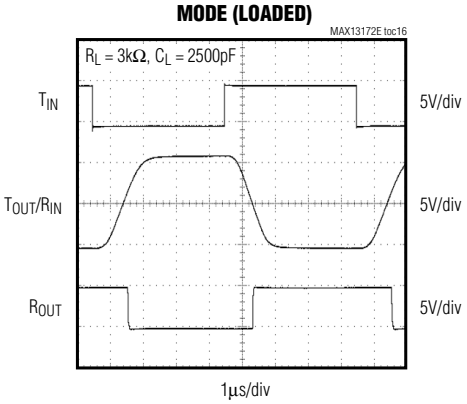
V.10 TEANSMITTER RISE/FALL TIME vs. LOAD CAPACITANCE



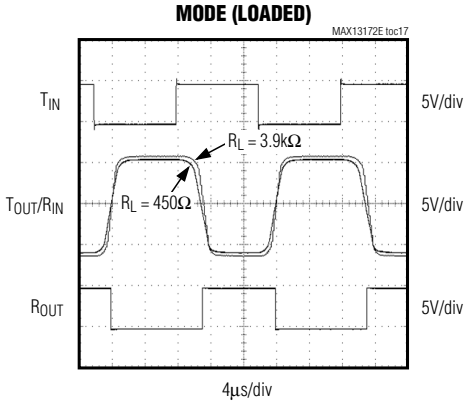
LOOPBACK SCOPE SHOT PHOTO V.11 MODE (UNLOADED)



LOOPBACK SCOPE SHOT PHOTO V.28 MODE (LOADED)



LOOPBACK SCOPE SHOT PHOTO V.10 MODE (LOADED)



+5V Multiprotocol, Software-Selectable Clock Transceiver

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Device Supply Voltage. Bypass V_{CC} with a 1µF capacitor-to-ground as close as possible to the device.
2	V_{DD}	Positive Supply Voltage Input. V_{DD} is generated by the MAX13170E. Bypass V_{DD} with a 1µF capacitor to ground.
3	T1IN	Transmitter 1 Logic Input
4	T2IN	Transmitter 2 Logic Input
5	T3IN	Transmitter 3 Logic Input
6	R1OUT	Receiver 1 Logic Output
7	R2OUT	Receiver 2 Logic Output
8	R3OUT	Receiver 3 Logic Output
9	T4IN	Transmitter 4 Logic input
10	R4OUT	Receiver 4 Logic Output
11	M0	Mode Select 0 Input. Internally pullup to V_{CC}.
12	M1	Mode Select 1 Input. Internally pullup to V_{CC}.
13	M2	Mode Select 2 Input. Internally pullup to V_{CC}.
14	DCE/$\overline{DTE}$	DCE/$\overline{DTE}$ Input. Internally pullup to V_{CC}. Logic level high selects DCE interface.
15	INVERT	T4/R4 Select Input. Internally pullup to V_{CC}. INVERT reverses the action of DCE/$\overline{DTE}$ for Channel 4.
16	T4OUTA/ R4INA	Transmitter 4 Inverting Output/Receiver 4 Inverting Input
17	R3INB	Receiver 3 Noninverting Input
18	R3INA	Receiver 3 Inverting Input
19	R2INB	Receiver 2 Noninverting Input
20	R2INA	Receiver 2 Inverting Input
21	T3OUTB/ R1INB	Transmitter 3 Noninverting Output/Receiver 1 Noninverting Input
22	T3OUTA/ R1INA	Transmitter 3 Inverting Output/Receiver 1 Inverting Input
23	T2OUTB	Transmitter 2 Noninverting Output
24	T2OUTA	Transmitter 2 Inverting Output
25	T1OUTB	Transmitter 1 Noninverting Output
26	T1OUTA	Transmitter 1 Inverting Output
27	GND	Ground
28	V_{EE}	Negative Supply Input. V_{EE} is generated by the MAX13170E. Bypass V_{EE} with a 1µF capacitor to ground.

Test Circuits

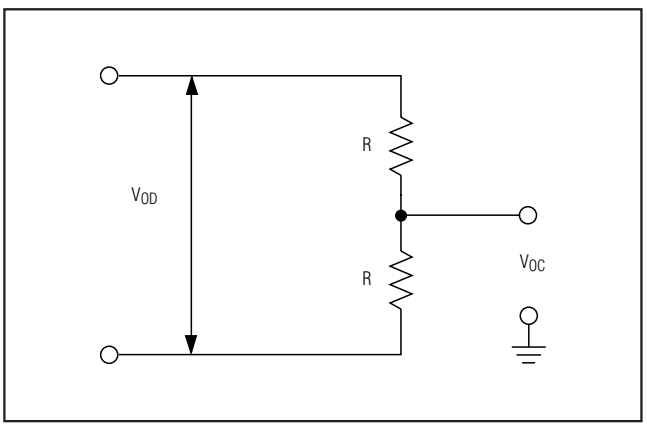


Figure 1. V.11 DC Test Circuit

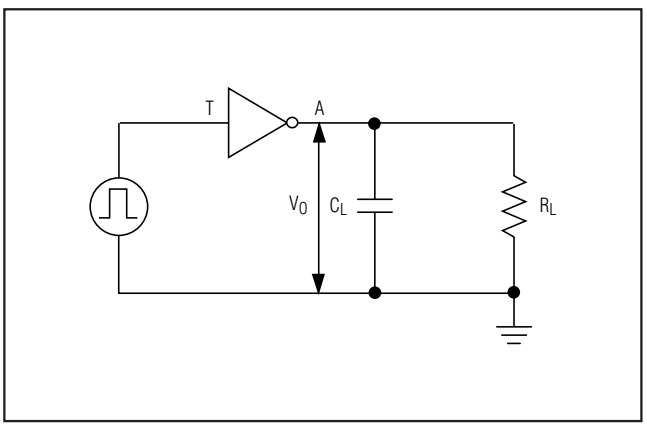


Figure 3. V.10/V.28 Transmitter Test Circuit

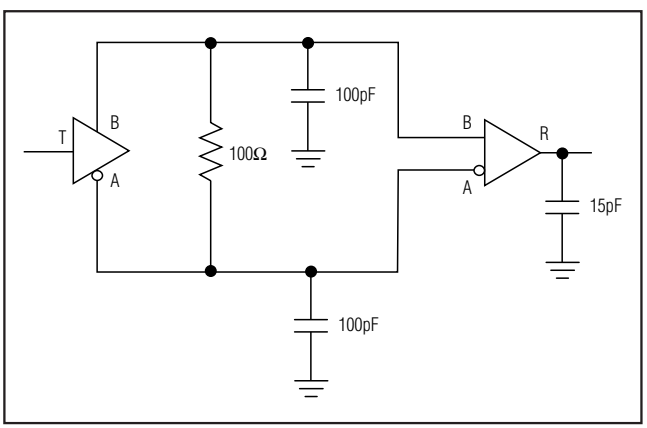


Figure 2. V.11 AC Test Circuit

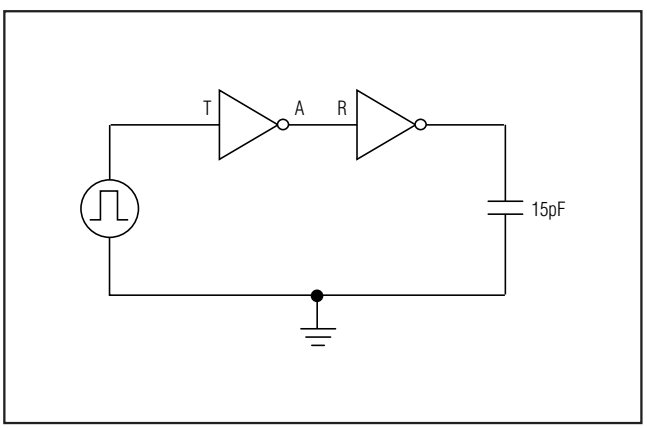


Figure 4. V.10/V.28 Receiver Test Circuit

Detailed Description

The MAX13172E is a four-driver/four-receiver, multiprotocol transceiver that operates from a single +5V supply. The charge pump operates from the MAX13170E. The MAX13172E along with the MAX13170E and MAX13174E, form a complete software-selectable DTE or DCE interface port that supports the V.28 (RS-232), V.10/V.11 (RS-449/V.36, EIA-530, EIA-530A, X.21, RS-423), and V.35 protocols. The MAX13172E usually carries the control signals. The MAX13170E carries the high-speed clock and data signals, and the MAX13174E provides termination for the clock and data signals.

The MAX13172E features an ultra-low supply current no-cable mode, fail-safe operation, and thermal-shutdown circuitry. Thermal shutdown protects the transmitter and receiver outputs against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

The state of the mode-select inputs M0, M1, and M2 determines which serial-interface protocol is selected (Table 1). The state of the DCE/$\overline{\text{DTE}}$ input determines whether the transceivers are configured as a DTE serial port or a DCE serial port. When the DCE/$\overline{\text{DTE}}$ input is logic-high, driver T3 is activated and receiver R1 is disabled. When the DCE/$\overline{\text{DTE}}$ input is logic-low, driver T3 disabled and receiver R1 is activated. The INVERT input state changes the DCE/$\overline{\text{DTE}}$ functionality regarding T4 and R4 only. M0, M1, M2, INVERT, and DCE/$\overline{\text{DTE}}$ are internally pulled up to V_{CC} to ensure logic-high if left unconnected.

+5V Multiprotocol, Software-Selectable Clock Transceiver

Switching Time Waveforms

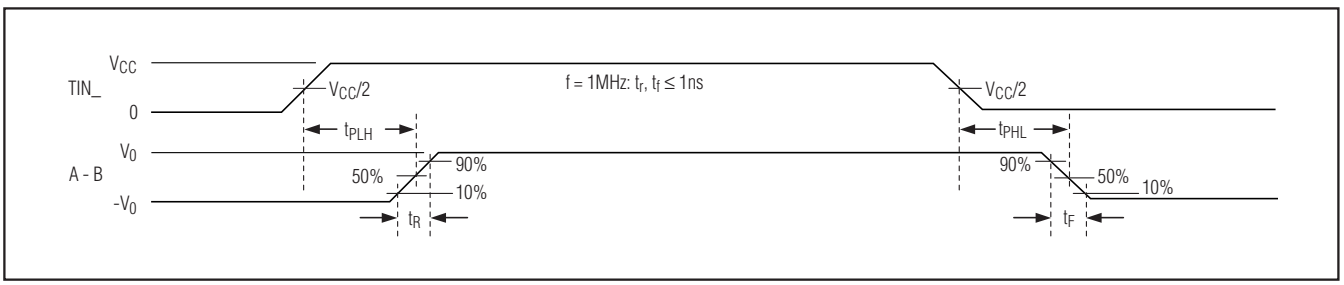


Figure 5. V.11 Transmitter Propogation Delays

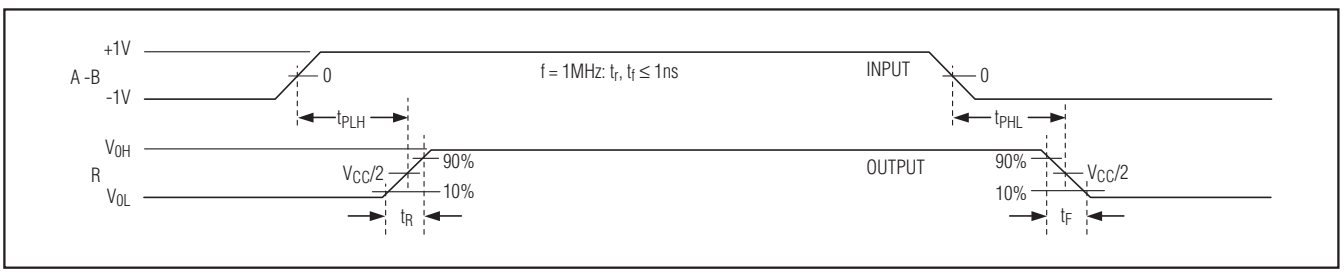


Figure 6. V.11 Receiver Propagation Delays

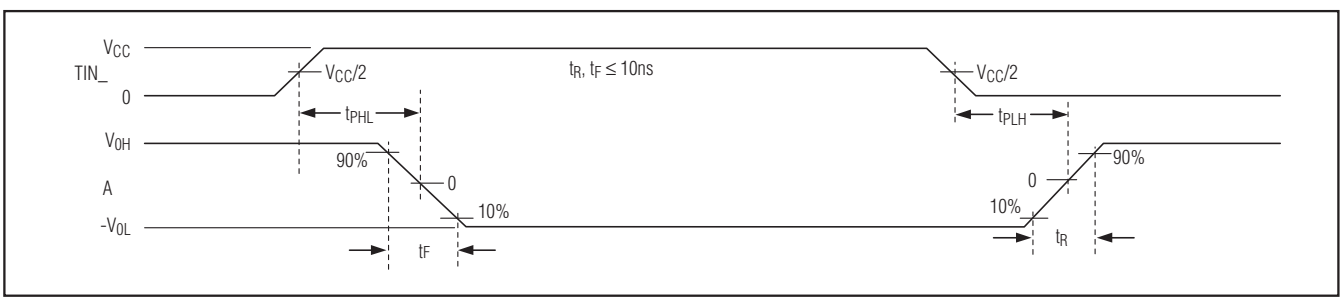


Figure 7. V.10 Transmitter Propagation Delays

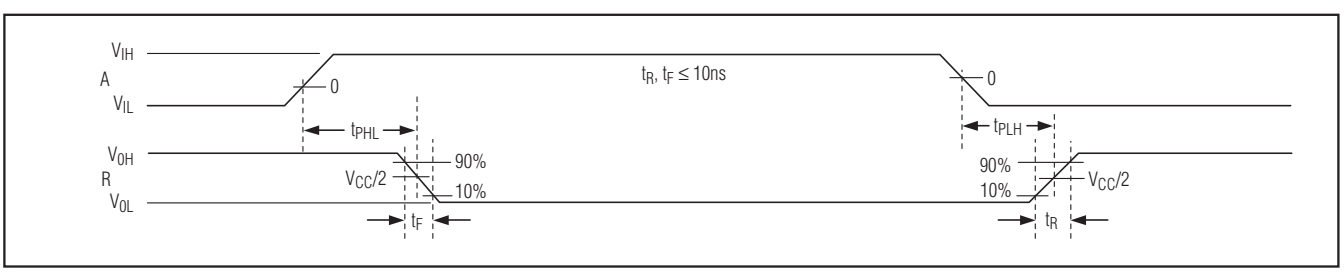


Figure 8. V.10 Receiver Propogation Delays

Switching Time Waveforms (continued)

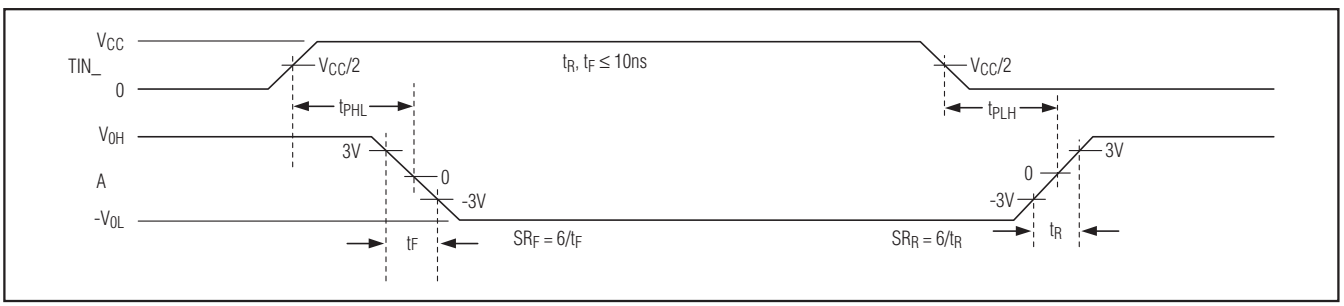


Figure 9. V.28 Transmitter Propagation Delays

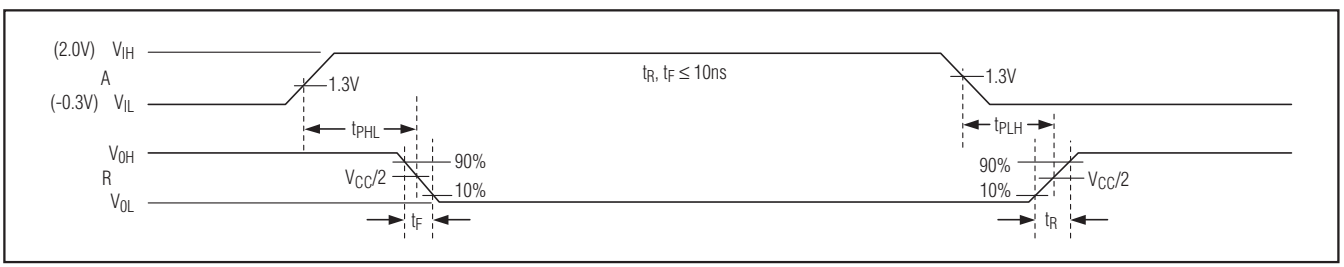


Figure 10. V.28 Receiver Propogation Delays

Table 1. Mode Select Table

PROTOCOL	M2	M1	M0	DCE/$\overline{\text{DTE}}$	INVERT	T1	T2	T3	R1	R2	R3	T4	R4
Not Used (Default V.11)	0	0	0	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10
RS-530A	0	0	1	0	0	V.11	V.10	Z	V.11	V.10	V.11	Z	V.10
RS-530	0	1	0	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10
X.21	0	1	1	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10
V.35	1	0	0	0	0	V.28	V.28	Z	V.28	V.28	V.28	Z	V.28
RS-449/V.36	1	0	1	0	0	V.11	V.11	Z	V.11	V.11	V.11	Z	V.10
V.28/RS-232	1	1	0	0	0	V.28	V.28	Z	V.28	V.28	V.28	Z	V.28
No Cable	1	1	1	0	0	Z	Z	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z
RS-530A	0	0	1	0	1	V.11	V.10	Z	V.11	V.10	V.11	V.10	Z
RS-530	0	1	0	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z
X.21	0	1	1	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z
V.35	1	0	0	0	1	V.28	V.28	Z	V.28	V.28	V.28	V.28	Z
RS-449/V.36	1	0	1	0	1	V.11	V.11	Z	V.11	V.11	V.11	V.10	Z
V.28/RS-232	1	1	0	0	1	V.28	V.28	Z	V.28	V.28	V.28	V.28	Z
No Cable	1	1	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z

+5V Multiprotocol, Software-Selectable Clock Transceiver

Table 1. Mode Select Table (continued)

PROTOCOL	M2	M1	M0	DCE/$\overline{\text{DTE}}$	INVERT	T1	T2	T3	R1	R2	R3	T4	R4
Not Used (Default V.11)	0	0	0	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z
RS-530A	0	0	1	1	0	V.11	V.10	V.11	Z	V.10	V.11	V.10	Z
RS-530	0	1	0	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z
X.21	0	1	1	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z
V.35	1	0	0	1	0	V.28	V.28	V.28	Z	V.28	V.28	V.28	Z
RS-449/V.36	1	0	1	1	0	V.11	V.11	V.11	Z	V.11	V.11	V.10	Z
V.28/RS-232	1	1	0	1	0	V.28	V.28	V.28	Z	V.28	V.28	V.28	Z
No Cable	1	1	1	1	0	Z	Z	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10
RS-530A	0	0	1	1	1	V.11	V.10	V.11	Z	V.10	V.11	Z	V.10
RS-530	0	1	0	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10
X.21	0	1	1	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10
V.35	1	0	0	1	1	V.28	V.28	V.28	Z	V.28	V.28	Z	V.28
RS-449/V.36	1	0	1	1	1	V.11	V.11	V.11	Z	V.11	V.11	Z	V.10
V.28/RS-232	1	1	0	1	1	V.28	V.28	V.28	Z	V.28	V.28	Z	V.28
No Cable	1	1	1	1	1	Z	Z	Z	Z	Z	Z	Z	Z

The MAX13172E's mode can be selected through software control of the M0, M1, M2, INVERT, and DCE/$\overline{\text{DTE}}$ inputs. Alternatively, the mode can be selected by shorting the appropriate combination of mode control inputs to GND (the inputs left unconnected will be internally pulled up to V_{CC} - logic-high). If the M0, M1, and M2 mode inputs are all unconnected, the MAX13172E will enter no-cable mode.

Fail-Safe

The MAX13172E guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all the drivers disabled. The V.11 receivers threshold is set between -200mV and -50mV to guarantee fail-safe operation. If the differential receiver input voltage (B - A) is ≥ -50mV, ROUT is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0 by the termination. With the receiver thresholds of the MAX13172E, this results in ROUT logic-high.

The V.10 receiver threshold is set between +50mV and +250mV. If the V.10 receiver input voltage is less than or equal to +50mV, ROUT is logic-high. The V.28 receiver threshold is set between 0.8V and 2.0V. If the receiver input voltage is less than or equal to 0.8V, ROUT is logic-high. In the case of a terminated bus with transmitters disabled, the receiver's input voltage is pulled to 0 by the termination.

ESD Protection

As with all Maxim devices, a minimum of ±2kV-to-GND ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13172E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±10kV without damage (HBM). The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13172E keeps working without latchup or damage. ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13172E are characterized for protection to the following limits:

- ±10kV using the Human Body Model
- ±3kV using the Contact Method specified in IEC 61000-4-2
- ±3kV using the Air Gap Discharge Method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

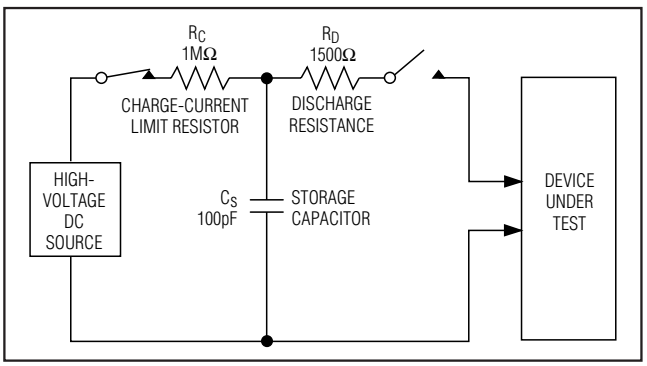


Figure 11a. Human Body ESD Test Model

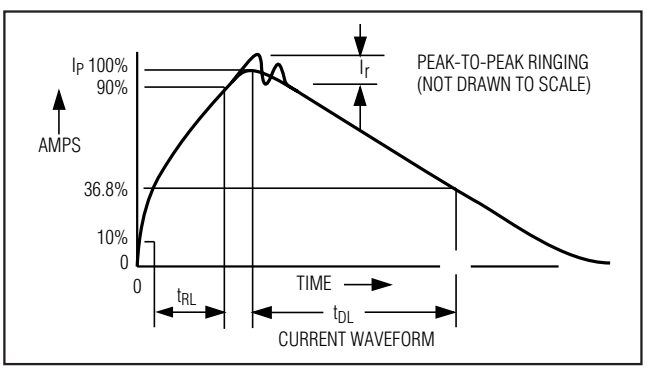


Figure 11b. Human Body Current Waveform

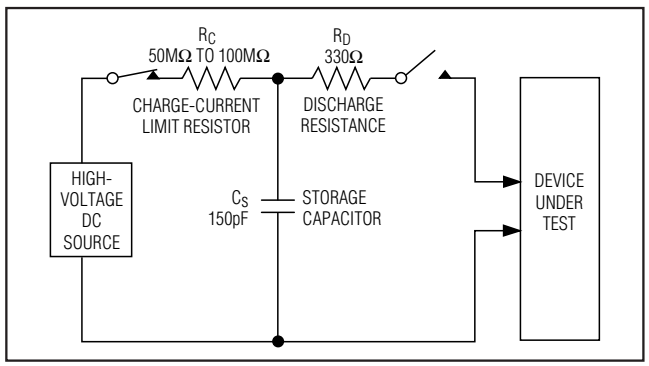


Figure 11c. IEC 61000-4-2 ESD Test Model

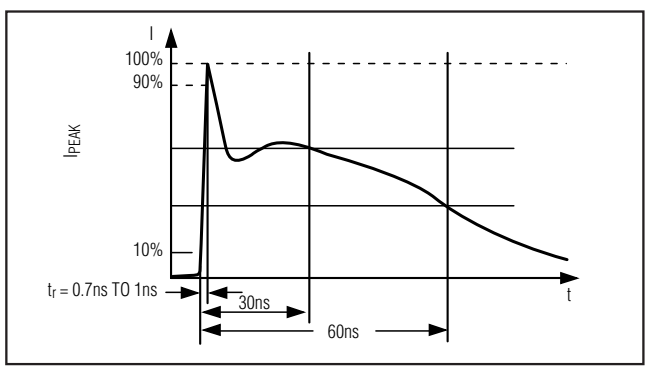


Figure 11d. IEC 61000-4-2 ESD Generator Current Waveform

Human Body Model

Figure 11a shows the Human Body Model, and Figure 11b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13172E helps equipment designs meet IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 11c shows the IEC 61000-4-2 model, and Figure 11d shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

+5V Multiprotocol, Software-Selectable Clock Transceiver

Applications Information

Cable-Selectable Configuration Application

A cable-selectable, multiprotocol DTE/DCE interface is shown in Figure 12. The mode control lines M0, M1, and DCE/$\overline{DTE}$ are wired to the DB-25 connector. To select the serial-interface mode, the appropriate combination of M0, M1, M2, and DCE/$\overline{DTE}$ are grounded within the cable wiring. The control lines that are not grounded are pulled high by the internal pullups on the MAX13170E. The serial-interface protocol of the MAX13172E is now selected based on the cable that is connected to the DB-25 interface.

V.10 (RS-423) Interface

The V.10 interface (Figure 13) is an unbalanced single-ended interface capable of driving a 450Ω load. The V.10 driver generates a minimum V_O voltage of ±4V across A' and C' when unloaded and a minimum voltage of 0.9 × V_O when loaded with 450Ω. The V.10 receiver has a single-ended input and does not reject common-mode differences between C and C'. The V.10 receiver input trip threshold is defined between +250mV and -250mV with input impedance characteristic shown in Figure 14.

The MAX13172E V.10 mode receiver has a threshold between +50mV and +250mV. To ensure that the receiver has proper fail-safe operation see the *Fail-Safe* section. To aid in rejecting system noise, the MAX13172E V.10 receiver has a typical hysteresis of 25mV. Switch S3 in Figures 16a and 16b is open in V.10 mode to disable the V.28 5kΩ termination at the receiver input. Switch S2 is closed and switch S1 is open to internally ground the receiver B input.

V.11 (RS-422) Interface

As shown in Figure 15, the V.11 protocol is a fully balanced differential interface. The V.11 driver generates a minimum of ±2V between nodes A and B when 100Ω minimum resistance is presented at the load. The V.11 receiver is sensitive to differential signals of ±200mV at receiver inputs A' and B'. The V.11 receiver input must comply with the impedance curve of Figure 14 and reject common-mode signals developed across the cable (referenced from C to C' in Figure 15) of up to ±7V.

The MAX13172E V.11 mode receiver has a differential threshold between -50mV and -200mV. To ensure that the receiver has proper fail-safe operation; see the *Fail-Safe* section. To aid in rejecting system noise, the MAX13172E V.11 receiver has a typical hysteresis of 15mV. Switch S3 in Figure 17 is open in V.11 mode to disable the V.28 5kΩ termination at the inverting receiver input. Because the control signals are slow (60kbps), 100Ω termination resistance is generally not required for the MAX13172E. The receiver inputs must also be compliant with the impedance curve shown in Figure 14.

V.28 (RS-232) Interface

The V.28 interface is an unbalanced single-ended interface (Figure 13). The V.28 generator provides a minimum of ±5V across the 3kΩ load impedance between A' and C'. The V.28 receiver has a single-ended input.

The MAX13172E V.28 mode receiver has a threshold between +0.8V and +2.0V. To aid in rejecting system noise, the MAX13172E V.28 receiver has a typical hysteresis of 0.25V. Switch S3 in Figures 18a and 18b is closed in V.28 mode to enable the 5kΩ V.28 termination at the receiver inputs.

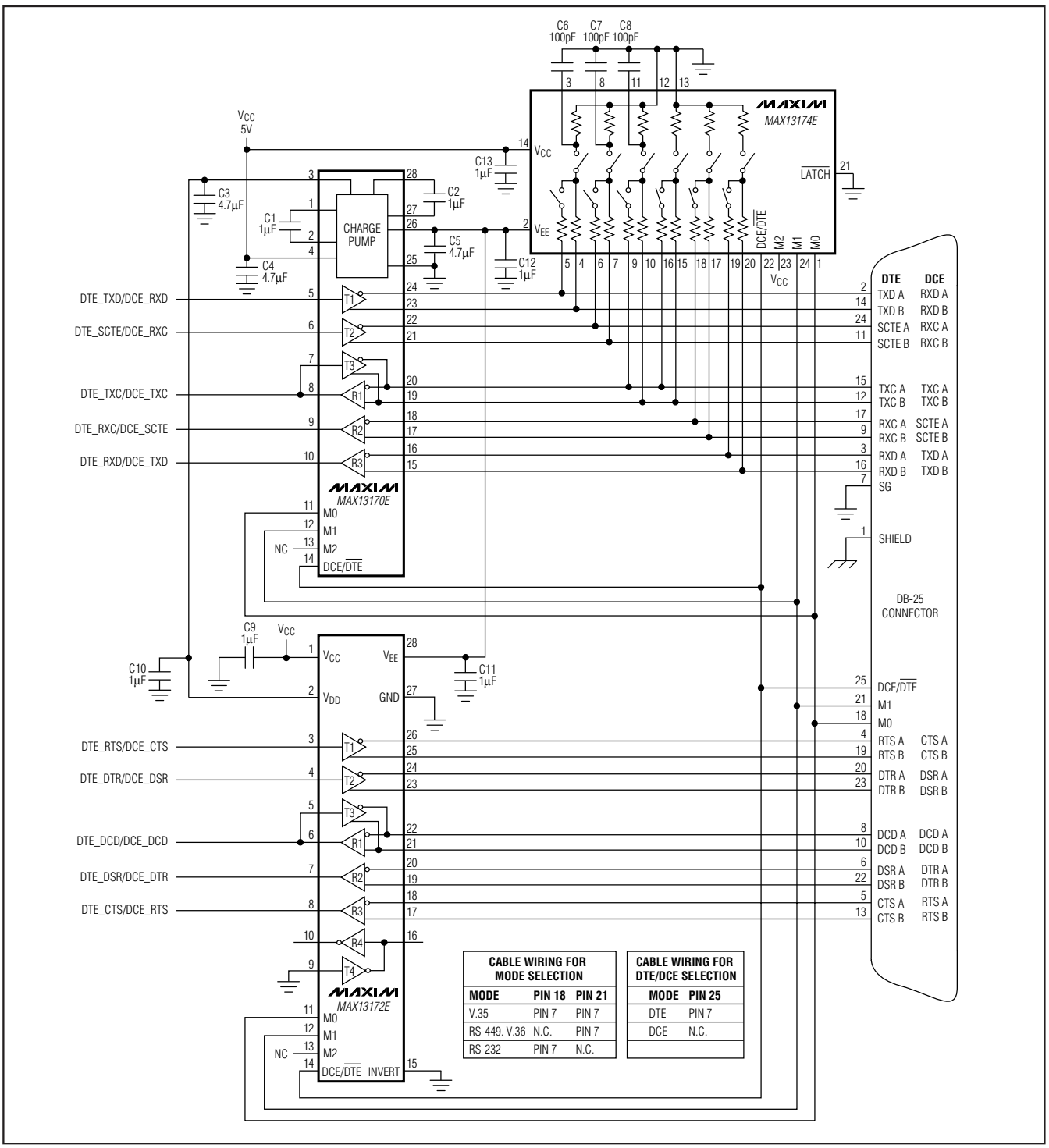
No-Cable Mode

The MAX13172E will enter no-cable mode when the mode-select pins are left unconnected or connected high (M0 = M1 = M2 = 1). In this mode, the multiprotocol drivers and receivers are disabled and the supply current is less than 10µA. The receiver outputs enter a high-impedance state in no-cable mode, which allows these output lines to be shared with other receiver outputs (the receiver outputs have an internal pullup resistor to pull the outputs high if not driven). Also, in no-cable mode, the transmitter outputs enter a high-impedance state, so these output lines can be shared with other devices.

DTE vs. DCE Operation

Figure 19 shows a port with one DB-25 connector that can be configured for either DTE or DCE operation. The configuration requires separate cables for proper signal routing in DTE or DCE operation. Figures 20 and 21 illustrates a DCE or DTE controller-selectable interface. The DCE/$\overline{DTE}$ and INVERT inputs switch the port's mode of operation (Table 1).

The MAX13170E and MAX13172E can be connected for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with an appropriate gender connector or a port with a connector that can be configured for DTE or DCE operation by rerouting the signals to the MAX13170E and MAX13172E using a dedicated DTE cable or dedicated DCE cable. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 20. Figure 21 illustrates a dedicated DTE port using a DB-25 male connector.



CABLE WIRING FOR MODE SELECTION		
MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
RS-449. V.36	N.C.	PIN 7
RS-232	PIN 7	N.C.

CABLE WIRING FOR DTE/DCE SELECTION	
MODE	PIN 25
DTE	PIN 7
DCE	N.C.

Figure 12. Cable-Selectable Multiprotocol DTE/DCE Port

+5V Multiprotocol, Software-Selectable Clock Transceiver

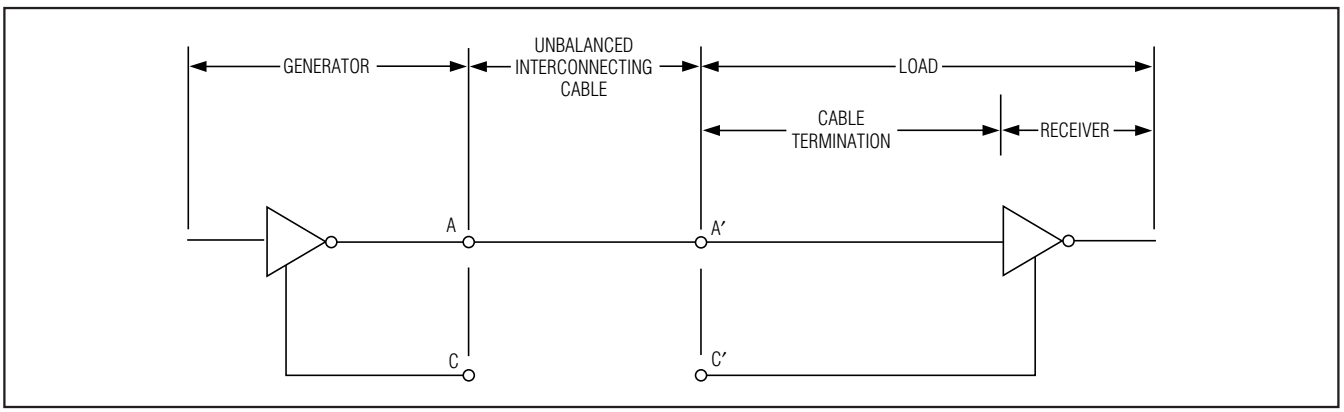


Figure 13. Typical V.10/V.28 Interface

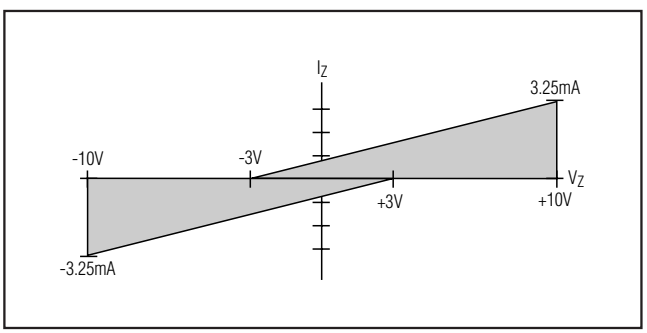


Figure 14. Receiver Input Impedance Curve

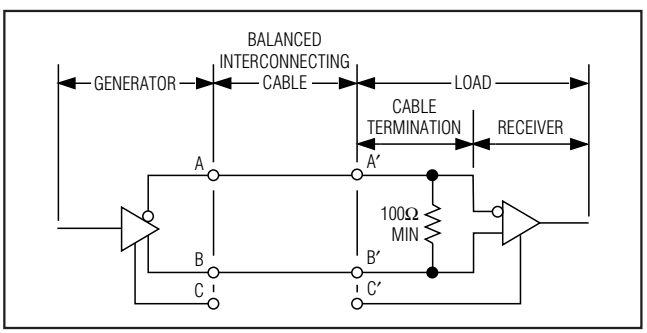


Figure 15. Typical V.11 Interface

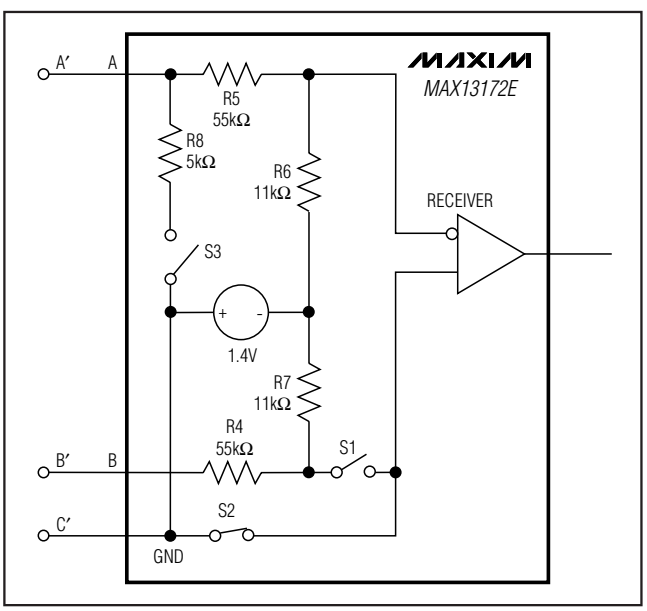


Figure 16a. V.10 Internal Resistance Network for Receivers 1, 2, and 3

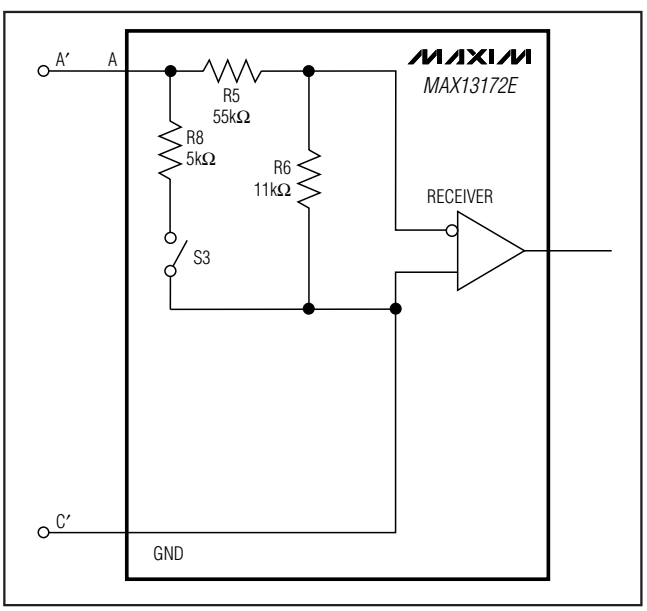


Figure 16b. V.10 Internal Resistance Network for Receiver 4

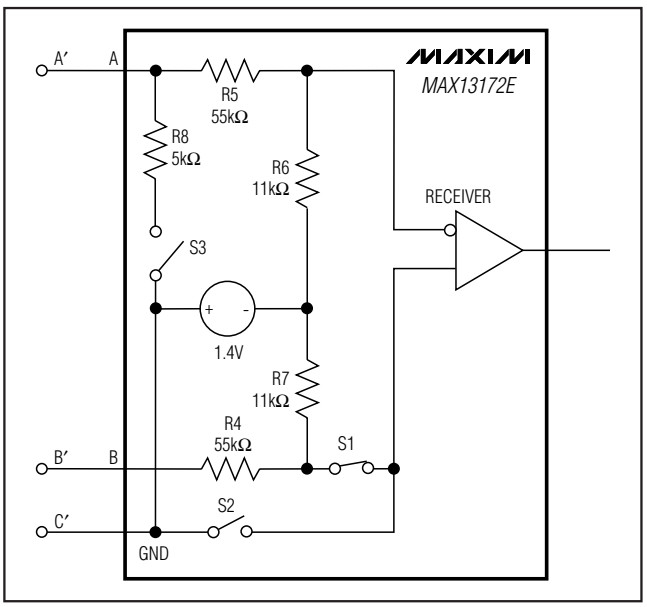


Figure 17. V.11 Internal Resistance Networks

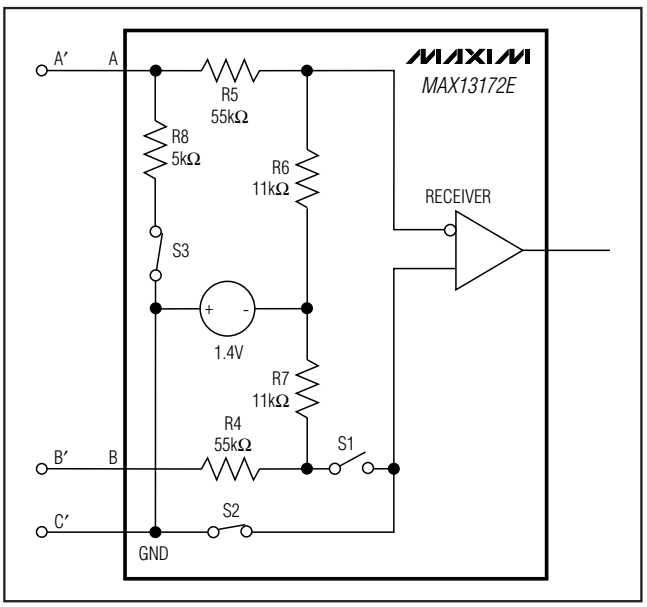


Figure 18a. V.28 Internal Resistance Network for Receiver 1, 2, and 3

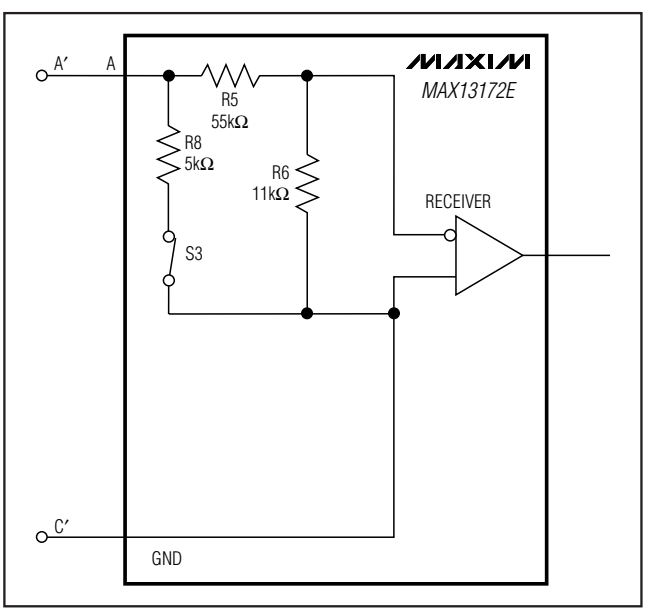


Figure 18b. V.28 Internal Resistance Network for Receiver 4

+5V Multiprotocol, Software-Selectable Clock Transceiver

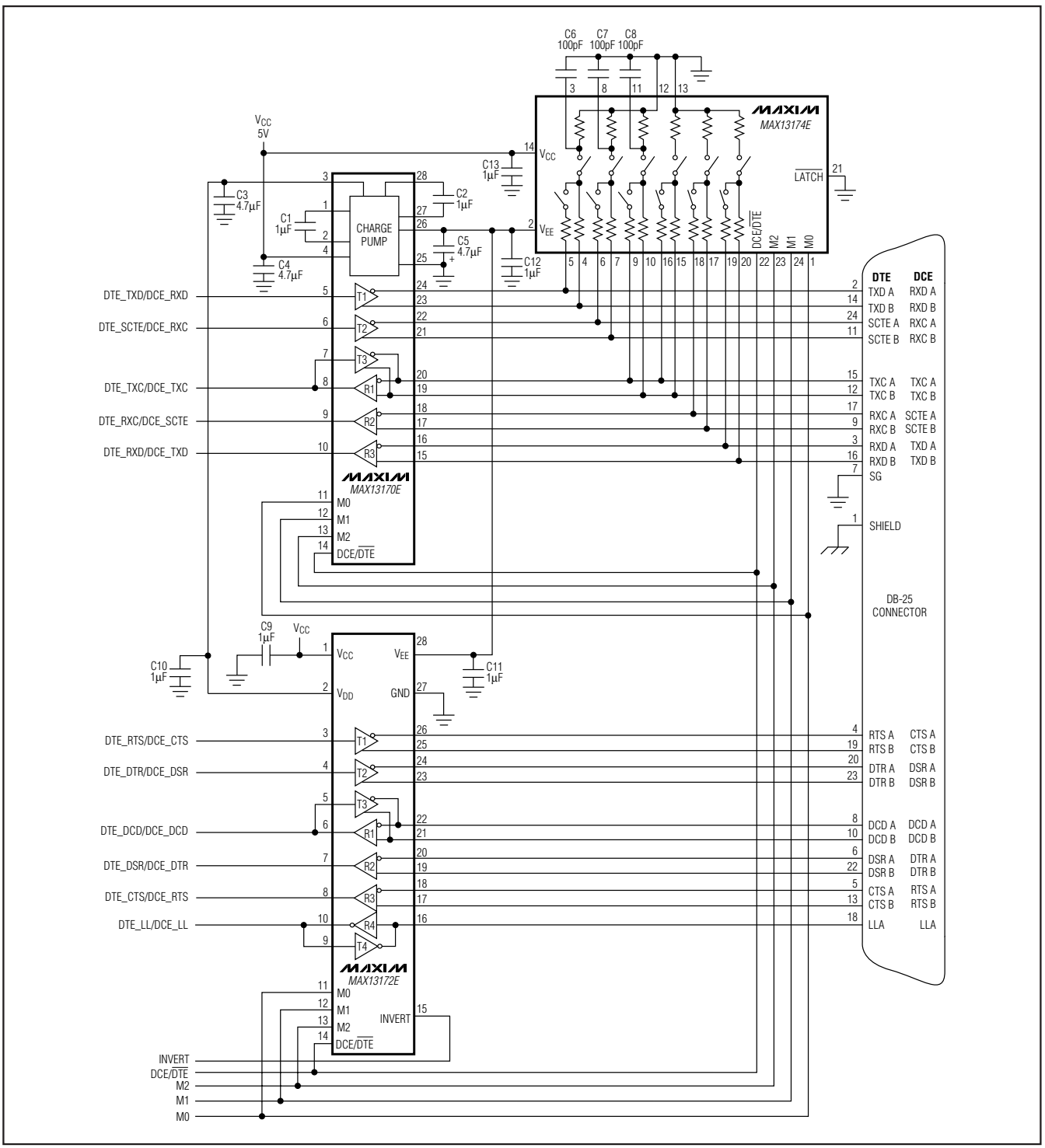


Figure 19. Controller-Selectable Multiprotocol DCE/DTE Port with DB-25 Connector

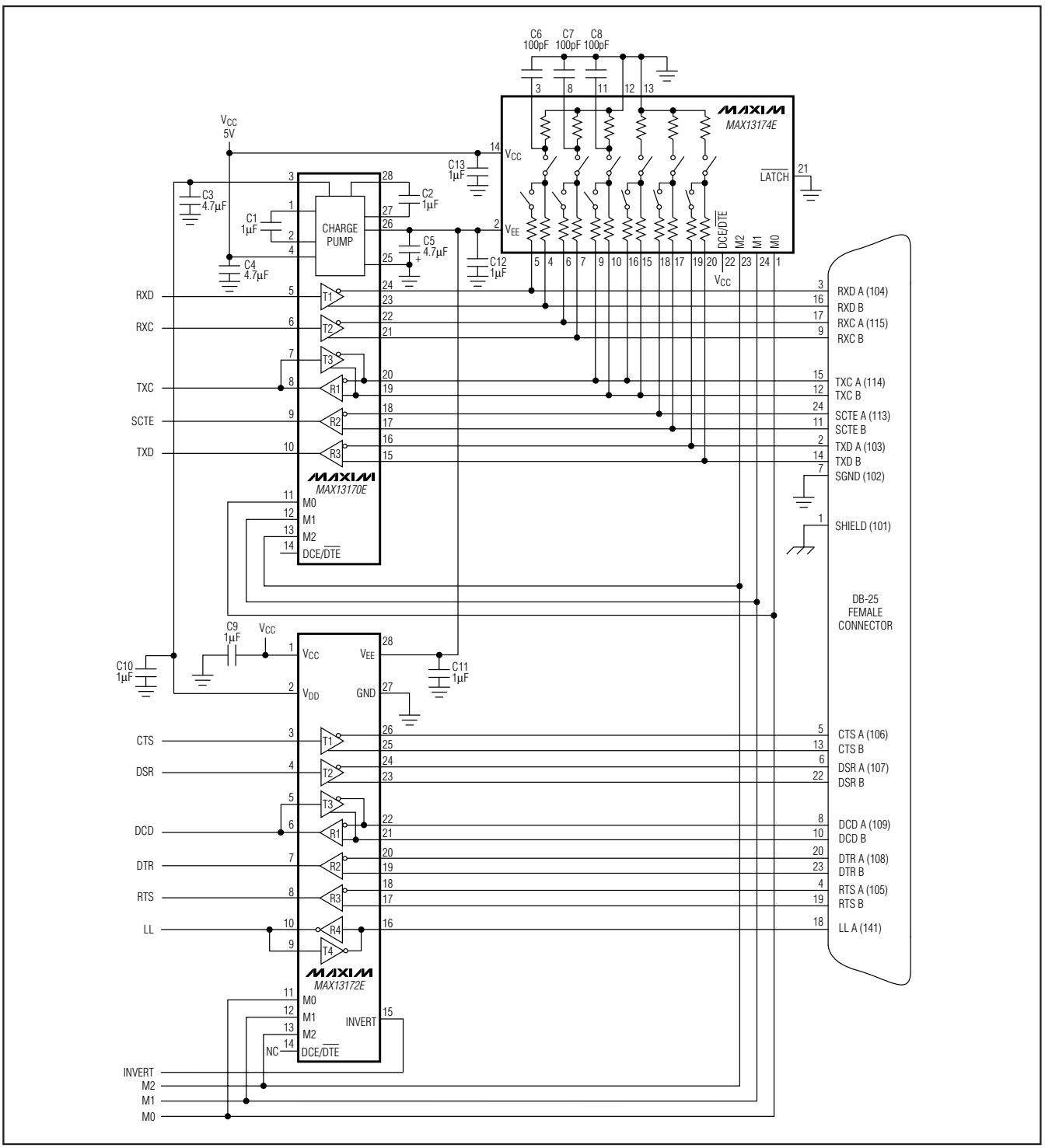


Figure 20. Controller-Selectable DCE Port with DB-25 Connector

+5V Multiprotocol, Software-Selectable Clock Transceiver

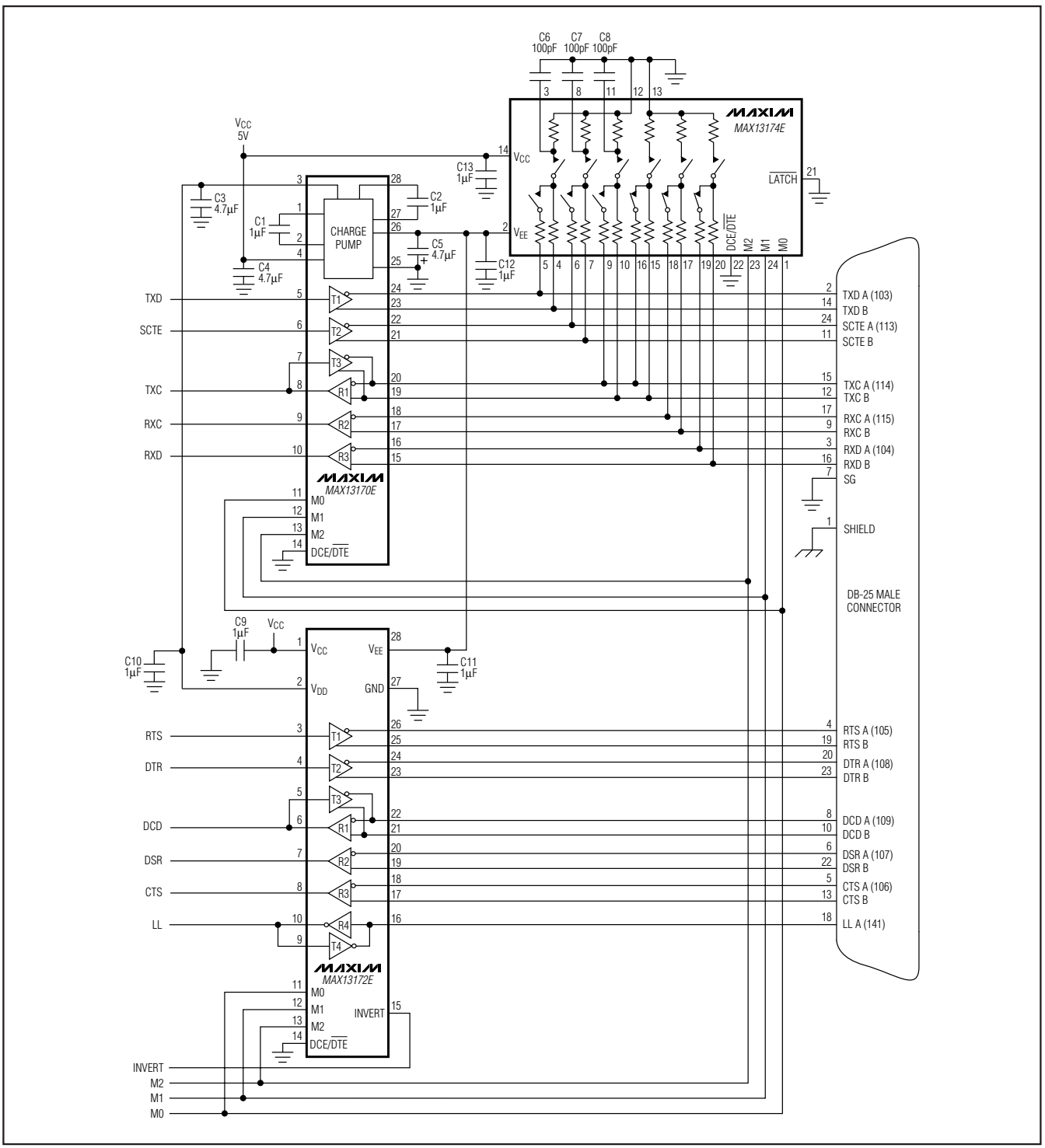
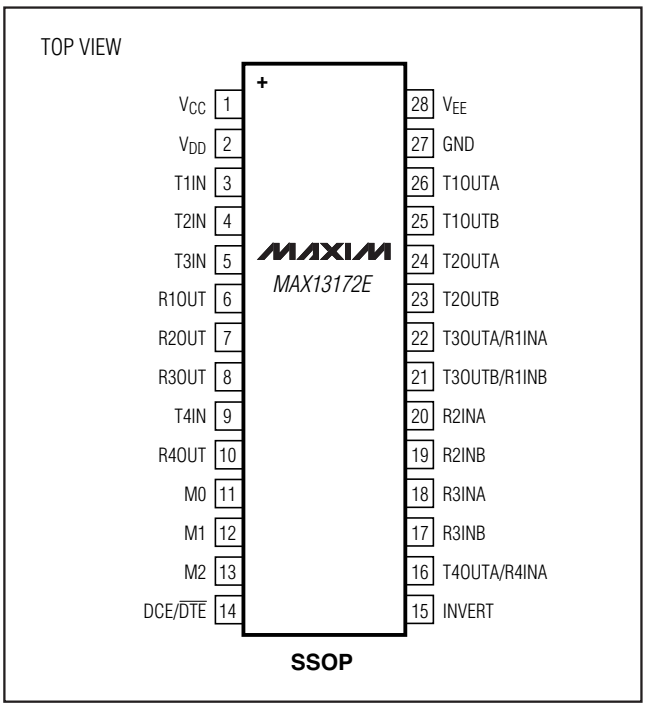


Figure 21. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

+5V Multiprotocol, Software-Selectable Clock Transceiver

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 SSOP	A28+2	**21-0056**	**90-0095**

+5V Multiprotocol, Software-Selectable Clock Transceiver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	8/11	Updated soldering temperature in *Absolute Maximum Ratings*, updated *Fail-Safe* section, updated *Package Information* section, and added lead-free indicator to *Pin Configuration*	2, 23, 38