74HC257; 74HCT257

Quad 2-input multiplexer; 3-state

Rev. 7 — 2 February 2016 Product data sheet

1. General description

The 74HC257; 74HCT257 is a quad 2-input multiplexer with 3-state outputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC257: CMOS level
  - For 74HCT257: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC257D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT257D				
74HC257DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT257DB				
74HC257PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT257PW				

4. Functional diagram

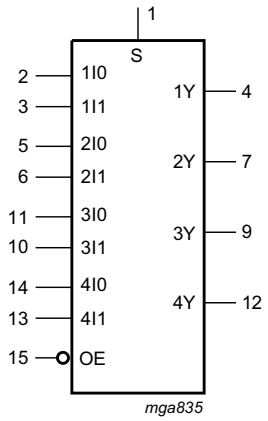

Fig 1. Logic symbol

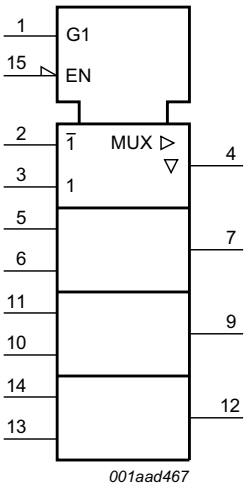

Fig 2. IEC logic symbol

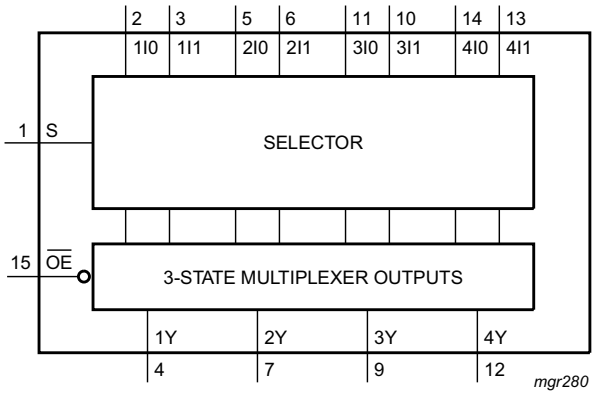

Fig 3. Functional diagram

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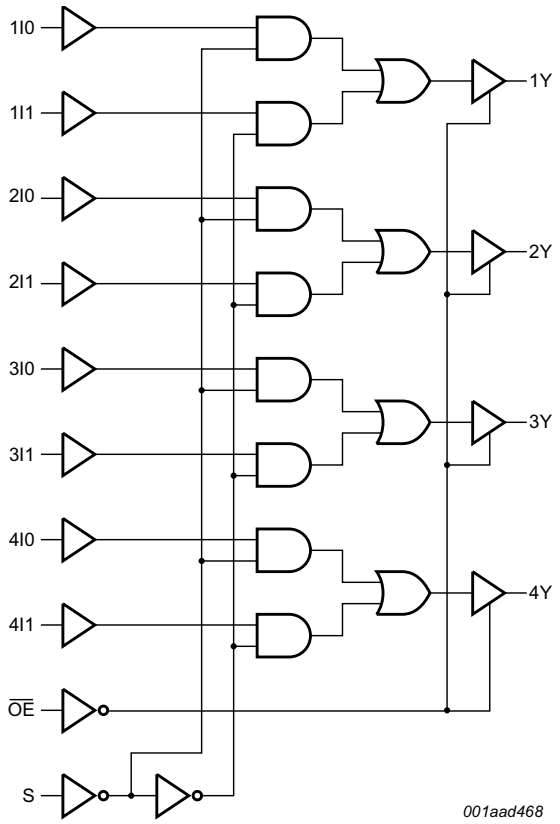

Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

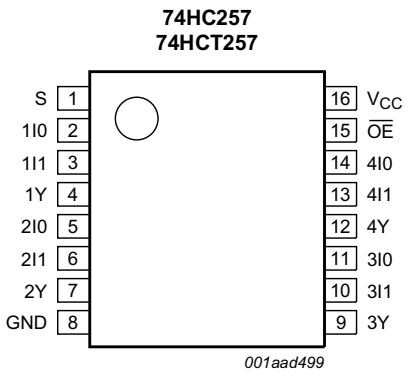

Fig 5. Pin configuration SO16, SSOP16 and TSSOP16

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0 to 4I0	2, 5, 11, 14	data input from source 0
1I1 to 4I1	3, 6, 10, 13	data input from source 1
1Y to 4Y	4, 7, 9, 12	3-state multiplexer output
GND	8	ground (0 V)
$\overline{OE}$	15	3-state output enable input (active LOW)
V_{CC}	16	supply voltage

6. Functional description

6.1 Function table

Table 3. Function table[1]

Control		Input		Output
$\overline{OE}$	S	nI0	nI1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±35	mA
I_{CC}	supply current			-	+70	mA
I_{GND}	ground current			–70	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	SO16 package	[2]	-	500	mW
		SSOP16 package	[3]	-	500	mW
		TSSOP16 package	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C, P_{tot} derates linearly with 8 mW/K.

[3] For SSOP16 and TSSOP16 packages: above 60 °C, P_{tot} derates linearly with 5.5 mW/K.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC257						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rates	V_{CC} = 2.0 V	-	-	625	ns
		V_{CC} = 4.5 V	-	1.67	139	ns
		V_{CC} = 6.0 V	-	-	83	ns
T_{amb}	ambient temperature		–40	-	+125	°C
74HCT257						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rates	V_{CC} = 4.5 V	-	1.67	139	ns
T_{amb}	ambient temperature		–40	-	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC257										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT257										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.33	-	0.4	V
		I_O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		per input pin; nI0, nI1 inputs	-	40	144	-	180	-	196	μA
		per input pin; $\overline{OE}$ input	-	135	486	-	608	-	662	μA
		per input pin; S input	-	70	252	-	315	-	343	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C		–40 °C to +85 °C	–40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
74HC257							
t_{pd}	propagation delay	nI0 to nY or nI1 to nY; see Figure 6 [1]					
		V_{CC} = 2.0 V	36	110	140	165	ns
		V_{CC} = 4.5 V	13	22	28	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	11	-	-	-	ns
		V_{CC} = 6.0 V	10	19	24	28	ns
		S to nY; see Figure 6					
		V_{CC} = 2.0 V	47	150	190	225	ns
		V_{CC} = 4.5 V	17	30	38	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	14	-	-	-	ns
		V_{CC} = 6.0 V	14	26	33	38	ns
t_{en}	enable time	$\overline{OE}$ to nY; see Figure 7 [2]					
		V_{CC} = 2.0 V	33	150	190	225	ns
		V_{CC} = 4.5 V	12	30	38	45	ns
		V_{CC} = 6.0 V	10	26	33	38	ns
t_{dis}	disable time	$\overline{OE}$ to nY; see Figure 7 [3]					
		V_{CC} = 2.0 V	41	150	190	225	ns
		V_{CC} = 4.5 V	15	30	38	45	ns
		V_{CC} = 6.0 V	12	26	33	38	ns
t_t	transition time	see Figure 6 [4]					
		V_{CC} = 2.0 V	14	60	75	90	ns
		V_{CC} = 4.5 V	5	12	15	18	ns
		V_{CC} = 6.0 V	4	10	13	15	ns
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC} [5]	45	-	-	-	pF
74HCT257							
t_{pd}	propagation delay	nI0 to nY or nI1 to nY; see Figure 6 [1]					
		V_{CC} = 4.5 V	16	30	38	45	ns
		V_{CC} = 5.0 V; C_L = 15 pF	13	-	-	-	ns
		S to nY; see Figure 6					
		V_{CC} = 4.5 V	20	35	44	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF	17	-	-	-	ns
t_{en}	enable time	$\overline{OE}$ to nY; V_{CC} = 4.5 V; see Figure 7 [2]	15	30	38	45	ns
t_{dis}	disable time	$\overline{OE}$ to nY; V_{CC} = 4.5 V; see Figure 7 [3]	16	30	38	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 6 [4]	5	12	15	18	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); For test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C		–40 °C to +85 °C	–40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
C_{PD}	power dissipation capacitance	per multiplexer; V_I = GND to V_{CC} – 1.5 V [5]	45	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

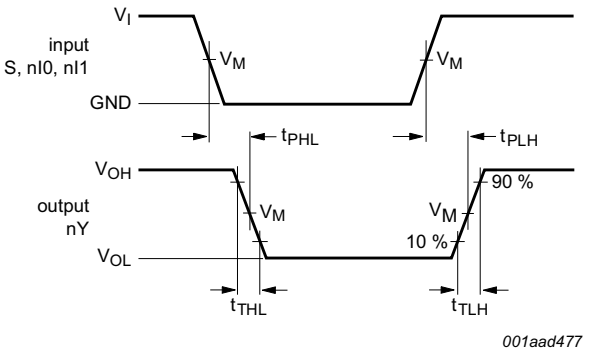
[2] t_{en} is the same as t_{PZH}, t_{PZL}.

[3] t_{dis} is the same as t_{PHZ}, t_{PLZ}.

[4] t_t is the same as t_{THL}, t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delays input (S, nI0, nI1) to output (nY) and output (nY) transition times

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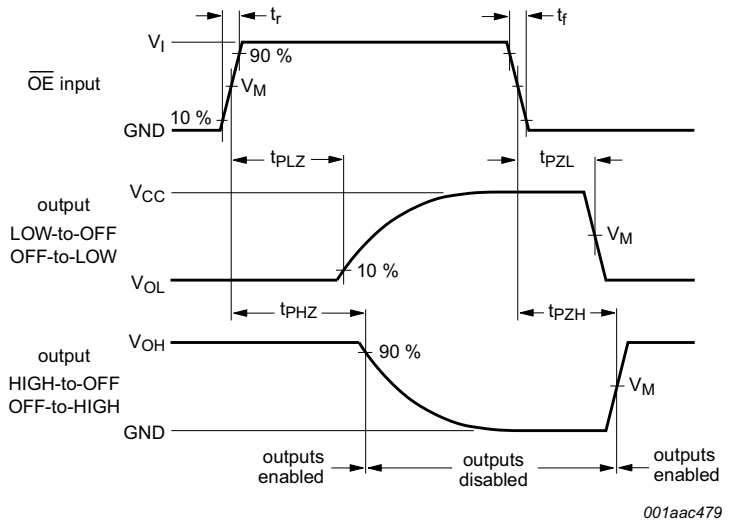

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. 3-state output enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC257	$0.5V_{CC}$	$0.5V_{CC}$
74HCT257	1.3 V	1.3 V

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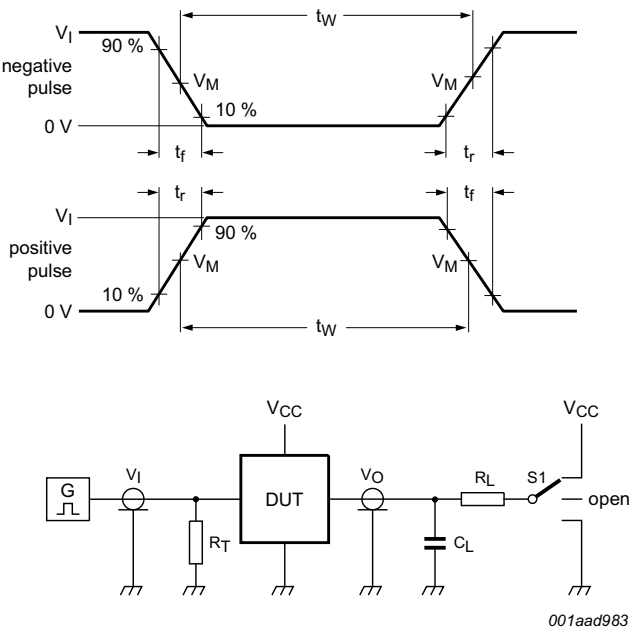

Measurement points are given in Table 8 and test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		Switch position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC257	V_{CC}	6 ns	50 pF	1 kΩ	open	GND	V_{CC}
74HCT257	3 V	6 ns	50 pF	1 kΩ	open	GND	V_{CC}

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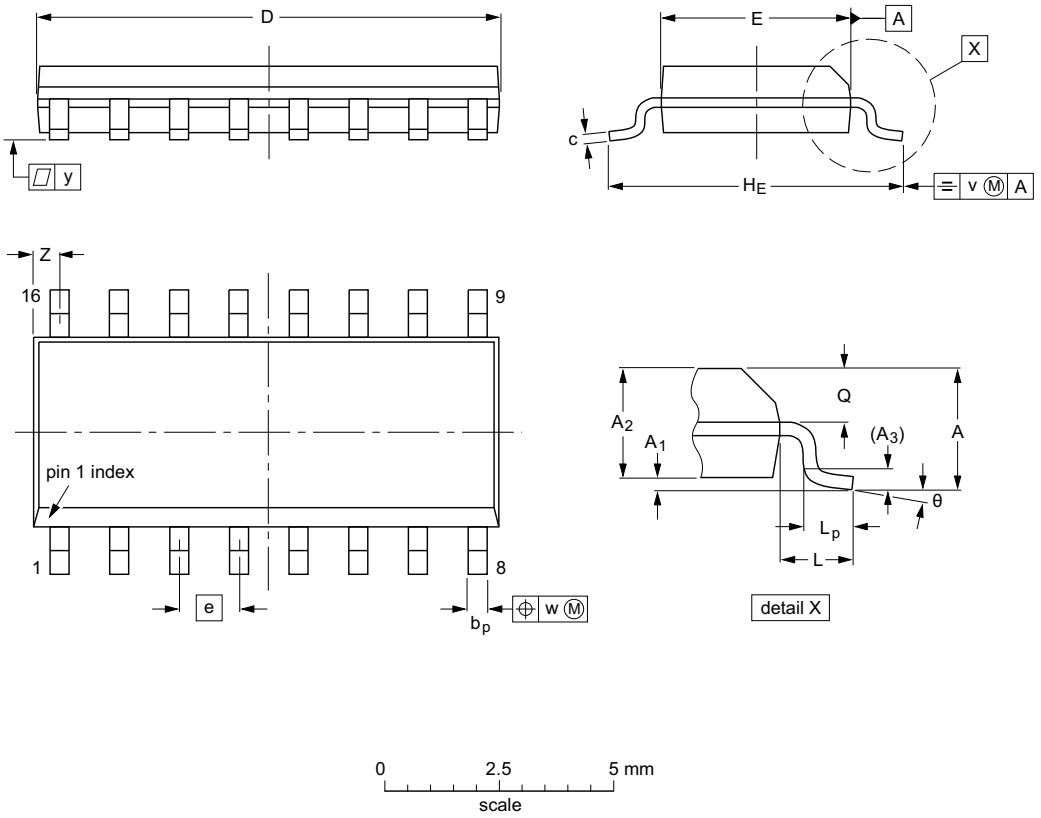
12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

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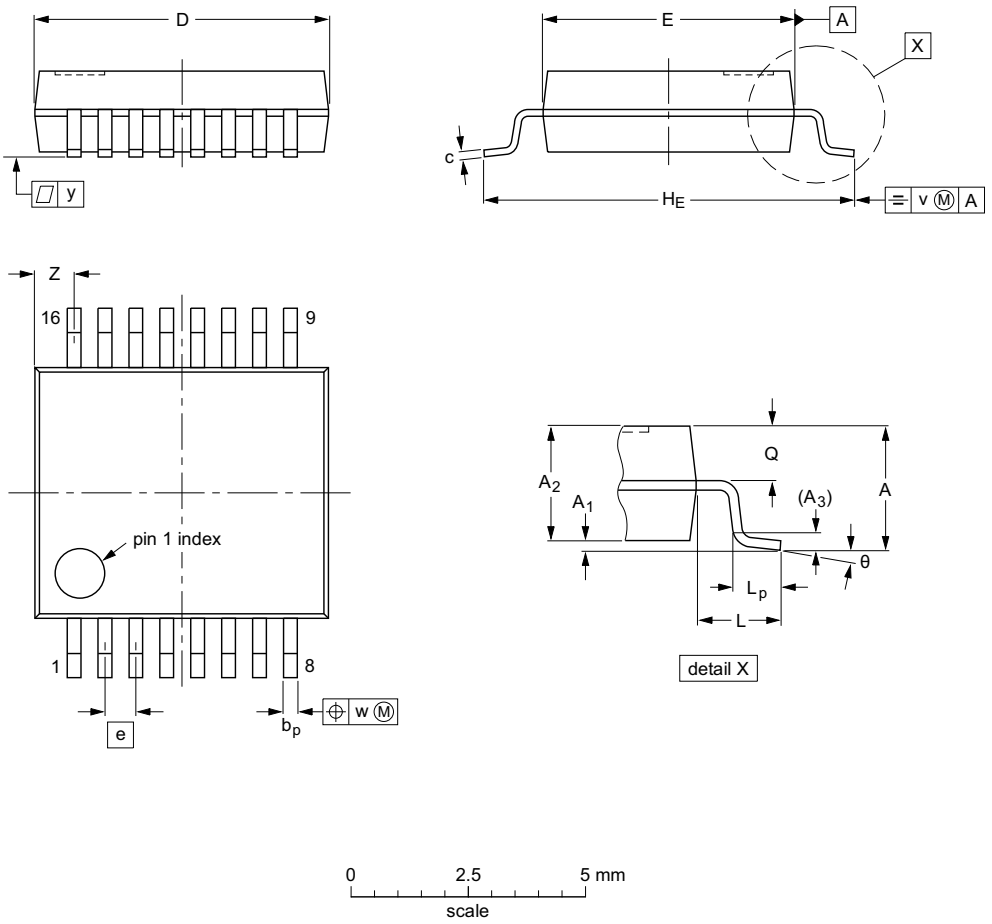
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT338-1 (SSOP16)

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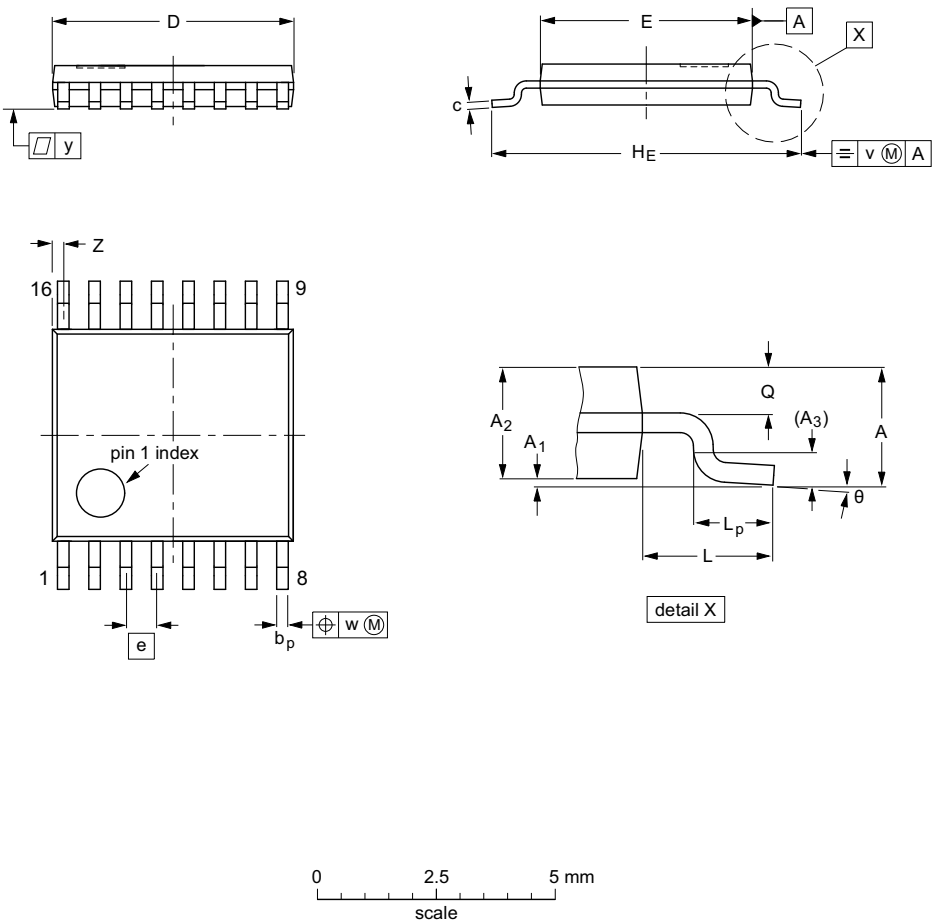
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT403-1 (TSSOP16)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT257 v.7	20160202	Product data sheet	-	74HC_HCT257 v.6
Modifications:	• Type numbers 74HC257N and 74HCT257N (SOT38-4) removed.			
74HC_HCT257 v.6	20150126	Product data sheet	-	74HC_HCT257 v.5
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT257 is corrected.			
74HC_HCT257 v.5	20100113	Product data sheet	-	74HC_HCT257 v.4
Modifications:	• Table 7: changed $\overline{3OE}$ to $\overline{OE}$			
74HC_HCT257 v.4	20090608	Product data sheet	-	74HC_HCT257 v.3
74HC_HCT257 v.3	20050920	Product data sheet	-	74HC_HCT257_CNV v.2
74HC_HCT257_CNV v.2	19980930	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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