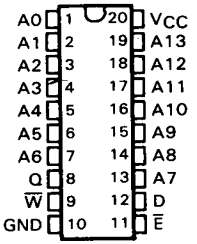
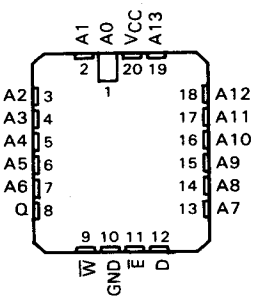
APRIL 1987—REVISED NOVEMBER 1987

- 16,384 × 1 Organization
- Separate I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2 Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '61CD16-25 . . . 25 ns
  '61CD16-35 . . . 35 ns
  '61CD16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Automatic Powerdown When Deselected
  — 125 μA MAX Standby Current at CMOS Levels
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 110 mW MAX (TTL Inputs)
  — Standby . . . 0.68 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Three State Output
- Packaging Options:
  — 20-Pin Ceramic 300-mil DIP
  — 20-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
D	Data Input
Q	Data Output
$\overline{E}$	Chip Enable/Power Down
GND	Ground
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '61CD16 is a separate I/O, 16,384-bit static random-access memory organized as 16,384 words by 1 bit. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. The six transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and extremely low standby power compared to the four transistor/two poly load cell making it ideal for military applications.

The '61CD16's static design and control signals ($\overline{E}$ and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin allows for easy memory expansion and automatic power-down. Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed upgrades for new and existing designs.

operation

addresses (A0-A13)

The 14 address inputs select one of the 16,384 -bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data in (D)

Data can be written into a selected device when the write-enable input is low. The input terminal can be driven directly from standard TTL circuits. Data on the input pin (D) is written into the memory location specified on the address pins (A0-A13).

data out (Q)

The three-state output buffer provides direct TTL compatability with a fanout of two Series 54 TTL gates, one Series 54S TTL gate, or eight Series 54LS TTL gates. The output terminal is in the high-impedance state when chip enable ($\overline{E}$) is high or whevever a write operation is being performed. Data out is the same polarity as data in.

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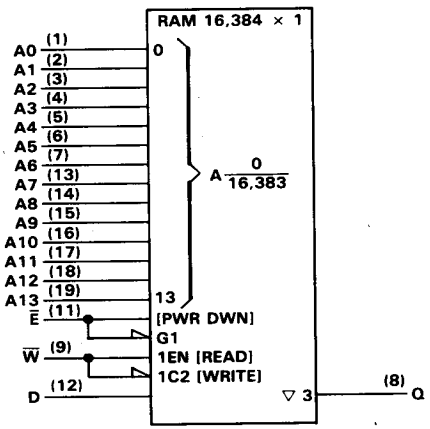
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

FUNCTION TABLE

INPUTS		OUTPUTS	MODE	POWER
$\overline{E}$	$\overline{W}$	Q		
H	X	HI-Z	Standby	Standby
L	H	Data Output	Read	Active
L	L	HI-Z	Write	Active

X = Don't Care.

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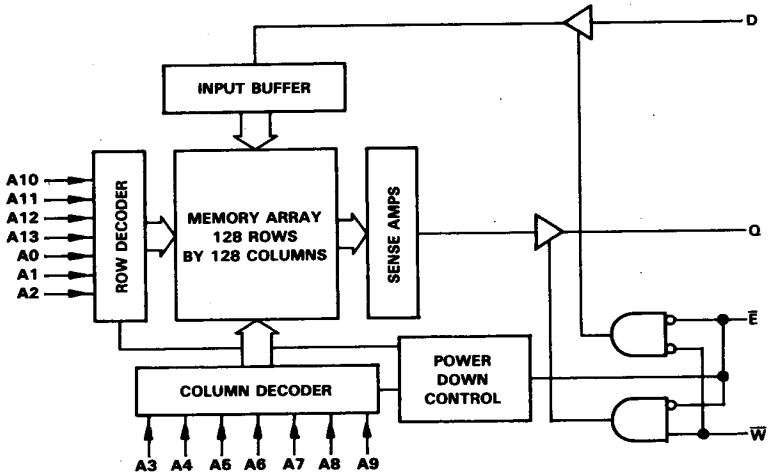
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (MIN) of −3 V for short pulse durations of 20 ns or less. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'61CD16-25 MIN	'61CD16-25 TYP	'61CD16-25 MAX	'61CD16-35 MIN	'61CD16-35 TYP	'61CD16-35 MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	µA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	−50		50	µA
I_{OS}	Short circuit output current (see Note 3)		V_{CC} = 5.5 V, V_O = GND			−350			−350	mA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20			20	mA
		CMOS-level inputs	Inputs = V_{CC} ± 0.3, V_{CC} = 5.5 V			125			125	µA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'61CD16-45 MIN	'61CD16-45 TYP	'61CD16-45 MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	µA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−50		50	µA
I_{OS}	Short circuit output current (see Note 3)		V_{CC} = 5.5 V, V_O = GND			−350	mA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20	mA
		CMOS-level inputs	Inputs = V_{CC} ± 0.3, V_{CC} = 5.5 V			125	µA

NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

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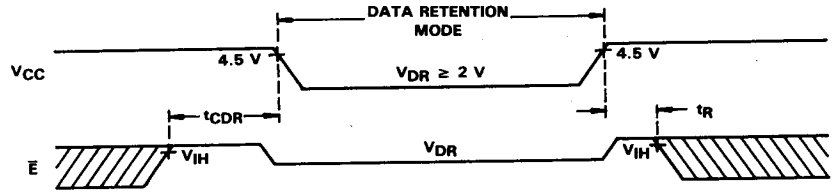
data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† VCC @ 2.0 V	TYP† VCC @ 3.0 V	MAX VCC @ 2.0 V	MAX VCC @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $\leq$ GND + 0.2 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	50	75	μA
t_{CDR}	Chip deselect to data retention time		0	—		—		ns
t_R	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		μA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, f = 1 MHz¶

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			4	pF
C_o	Output capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			7	pF

¶Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'61CD16-25 MIN	'61CD16-25 TYP	'61CD16-25 MAX	'61CD16-35 MIN	'61CD16-35 TYP	'61CD16-35 MAX	UNIT
$t_{c(rd)}$	Read cycle time	25			35			ns
$t_{c(wr)}$	Write cycle time	25			35			ns
$t_{w(W)}$	Write-enable pulse duration	15			20			ns
t_{ELWH}	Chip-enable low to end of write	25			30			ns
$t_{su(A)}$	Address setup time to write start	0			0			ns
$t_{su(D)}$	Data setup time to write end	12			15			ns
$t_{h(A)}$	Address hold from write end	0			0			ns
$t_{h(D)}$	Data hold from write end	0			0			ns
t_{ELIH}	Delay time, chip-enable low to power up§	5			5			ns
t_{EHIL}	Delay time, chip-enable high to power down§			35			35	ns
t_{AVWH}	Address setup to write end	25			30			ns

§This parameter is guaranteed but not tested.

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timing requirements over recommended supply voltage range and operating temperature range

		'61CD16-45			UNIT
		MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	45			ns
$t_{c(wr)}$	Write cycle time	45			ns
$t_{w(W)}$	Write-enable pulse duration	20			ns
t_{ELWH}	Chip-enable low to end of write	40			ns
$t_{su(A)}$	Address setup time to write start	0			ns
$t_{su(D)}$	Data setup time to write end	15			ns
$t_{h(A)}$	Address hold from write end	0			ns
$t_{h(D)}$	Data hold from write end	0			ns
t_{ELIH}	Delay time, chip-enable low to power up†	5			ns
t_{EHIL}	Delay time, chip-enable high to power down†			35	ns
t_{AVWH}	Address setup to write end	40			ns

†This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'61CD16-25			'61CD16-35			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{a(A)}$	Access time from address	I_{OH} = −4 mA, I_{OL} = 8 mA			25			35	ns
$t_{a(E)}$	Access time from chip enable low	C_L = 30 pF,			25			35	ns
$t_{v(A)}$	Output data valid after address change	See Figure 1a.	0	3		0	3		ns
$t_{en(W)}$	Output enable time from write enable high‡		0		15	0		20	ns
$t_{en(E)}$	Output enable time from chip enable low‡	R1 = 481 Ω, R2 = 255 Ω,	5			5			ns
$t_{dis(E)}$	Output disable time from chip enable high‡	C_L = 5 pF, See Figure 1b.			10			15	ns
$t_{dis(W)}$	Output disable time from write enable low‡				10			15	ns

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'61CD16-45			UNIT
			MIN	TYP	MAX	
$t_{a(A)}$	Access time from address	I_{OH} = −4 mA, I_{OL} = 8 mA			45	ns
$t_{a(E)}$	Access time from chip enable low	C_L = 30 pF,			45	ns
$t_{v(A)}$	Output data valid after address change	See Figure 1a.	0	3		ns
$t_{en(W)}$	Output enable time from write enable high‡		0		20	ns
$t_{en(E)}$	Output enable time from chip enable low‡	R1 = 481 Ω, R2 = 255 Ω,	5			ns
$t_{dis(E)}$	Output disable time from chip enable high‡	C_L = 5 pF, See Figure 1b.			20	ns
$t_{dis(W)}$	Output disable time from write enable low‡				20	ns

‡Transition is measured ±500 mV from steady state voltage; this parameter is guaranteed but not tested.

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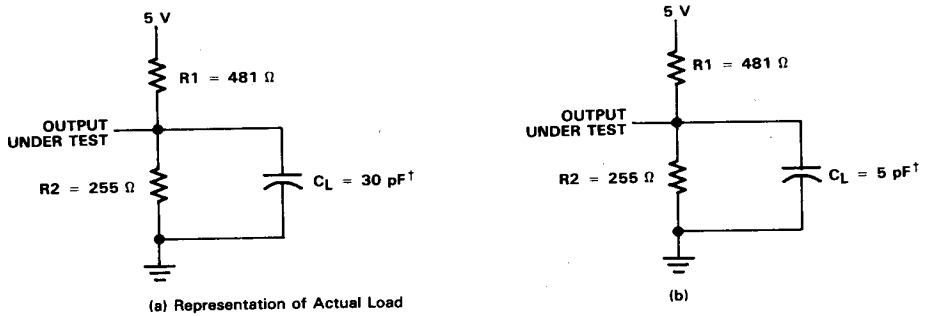
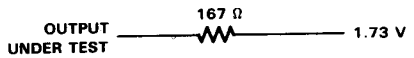
PARAMETER MEASUREMENT INFORMATION



(a) Representation of Actual Load

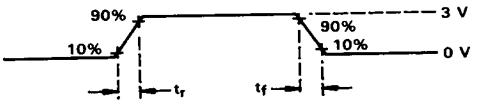
(b)

THEVENIN EQUIVALENT OF (a) OR (b)



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT



NOTE 4: t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

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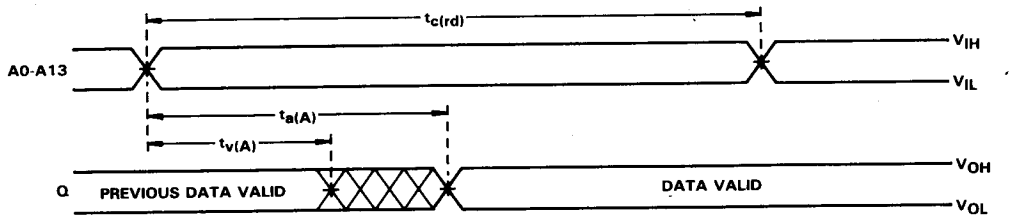
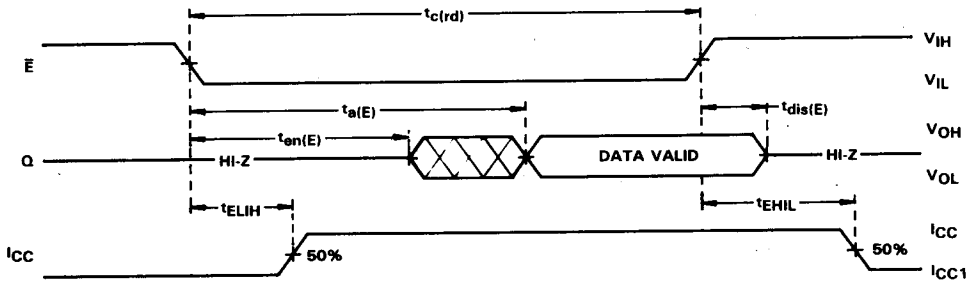
read cycle timing from address†



†$\overline{W}$ is high, and $\overline{E}$ is low.

read cycle timing from chip enable‡



‡$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

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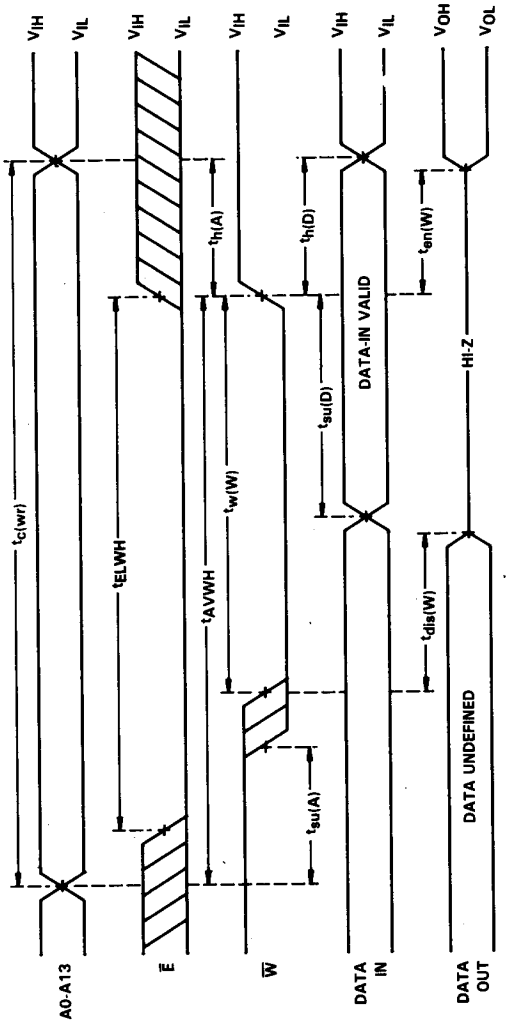
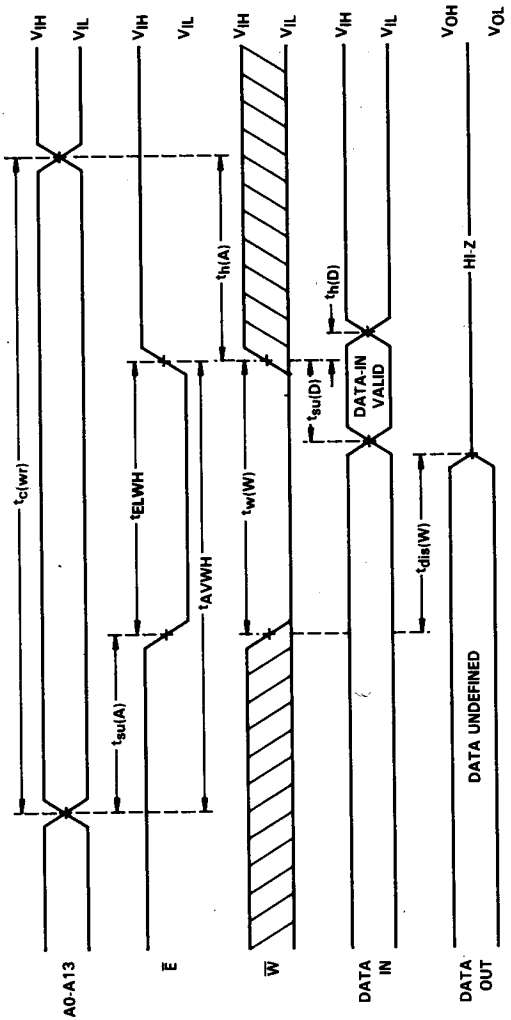
write cycle timing controlled by write enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.
NOTE: For both $\overline{W}$-controlled and $\overline{E}$-controlled Write operations, the internal write time of the memory is defined by the overlap of $\overline{E}$ low and $\overline{W}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge that terminates the write.

write cycle timing controlled by chip enable†



†$\overline{E}$ or $\overline{W}$ must be high during address transitions.

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