

Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPVZ5010G series piezoresistive transducers are state-of-the-art monolithic silicon pressure sensors designed for the appliance, consumer, healthcare, industrial and automotive market. The analog output can be read directly into the A/D input of Freescale microcontrollers. This transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure. The axial port has been modified to accommodate industrial grade tubing.

Features

- 5.0% Maximum Error over 0° to 85°C
- Temperature Compensated over -40° to +125°C
- Durable Thermoplastic (PPS) Package
- Available in Surface Mount (SMT) or Through-hole (DIP) Configurations

Application Examples

- Washing Machine Water Level Measurement (Reference AN1950)
- Ideally Suited for Microprocessor or Microcontroller-Based Systems
- Appliance Liquid Level and Pressure Measurement
- Respiratory Equipment

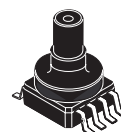
ORDERING INFORMATION

| Device Type | Case No. | MPVZ Series Order No. | Packing Options | Device Marking |
|---------------|----------|-----------------------|-----------------|----------------|
| Surface Mount | 1735-01 | MPVZ5010GW6U | Rails | MZ5010GW |
| Through-Hole | 1560-02 | MPVZ5010GW7U | Rails | MZ5010GW |
| Surface Mount | 482-01 | MPVZ5010G6U | Rails | MZ5010G |
| Surface Mount | 482-01 | MPVZ5010G6T1 | Tape & Reel | MZ5010G |
| Through-Hole | 482B-03 | MPVZ5010G7U | Rails | MZ5010G |

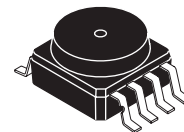
MPVZ5010G SERIES

**INTEGRATED
PRESSURE SENSOR**
0 to 10 kPa (0 to 1019.78 mm H₂O)
0.2 to 4.7 V OUTPUT

SMALL OUTLINE PACKAGE SURFACE MOUNT

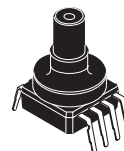


MPVZ5010GW6U
CASE 1735-01

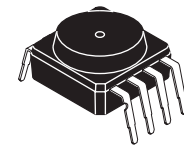


MPVZ5010G6U/T1
CASE 482-01

SMALL OUTLINE PACKAGE THROUGH-HOLE



MPVZ5010GW7U
CASE 1560-02



MPVZ5010G7U
CASE 482B-03

PIN NUMBERS⁽¹⁾

| | | | |
|---|------------------|---|-----|
| 1 | N/C | 5 | N/C |
| 2 | V _S | 6 | N/C |
| 3 | GND | 7 | N/C |
| 4 | V _{OUT} | 8 | N/C |

1. Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.

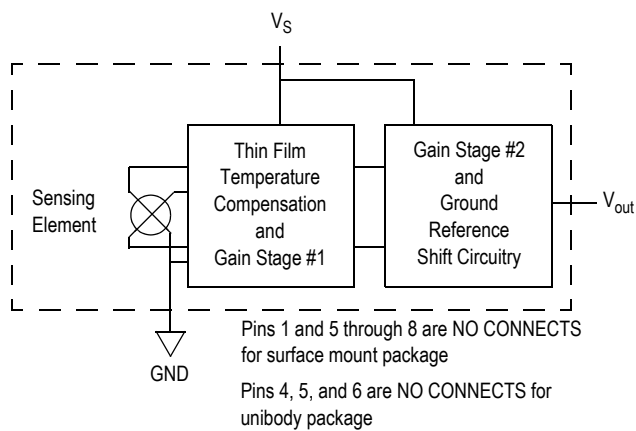


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings⁽¹⁾

| Rating | Symbol | Value | Unit |
|----------------------------------|-----------|-------------|------|
| Maximum Pressure ($P_1 > P_2$) | P_{max} | 40 | kPa |
| Storage Temperature | T_{stg} | -40 to +125 | °C |
| Operating Temperature | T_A | -40 to +125 | °C |

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Table 2. Operating Characteristics ($V_S = 5.0$ Vdc, $T_A = 25^\circ\text{C}$ unless otherwise noted, $P1 > P2$. Decoupling circuit shown in Figure 3 required to meet specification.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------|-------|--------------|---------------|----------------------------------|
| Pressure Range ⁽¹⁾ | P_{OP} | 0 | — | 10 1019.78 | kPa mm H ₂ O |
| Supply Voltage ⁽²⁾ | V_S | 4.75 | 5.0 | 5.25 | Vdc |
| Supply Current | I_o | — | 5.0 | 10 | mAdc |
| Minimum Pressure Offset ⁽³⁾ @ $V_S = 5.0$ Volts | V_{off} | 0 | 0.2 | 0.425 | Vdc |
| Full Scale Output ⁽⁴⁾ @ $V_S = 5.0$ Volts | V_{FSO} | 4.475 | 4.7 | 4.925 | Vdc |
| Full Scale Span ⁽⁵⁾ @ $V_S = 5.0$ Volts | V_{FSS} | 4.275 | 4.5 | 4.725 | Vdc |
| Accuracy ⁽⁶⁾ | — | — | — | ±5.0 | % V_{FSS} |
| Sensitivity | V/P | — | 450 4.413 | — | mV/kPa mV/mm H ₂ O |
| Response Time ⁽⁷⁾ | t_R | — | 1.0 | — | ms |
| Output Source Current at Full Scale Output | I_{O+} | — | 0.1 | — | mAdc |
| Warm-Up Time ⁽⁸⁾ | — | — | 20 | — | ms |
| Offset Stability ⁽⁹⁾ | — | — | ±0.5 | — | % V_{FSS} |

- 1.0 kPa (kiloPascal) equals 0.145 psi.
- Device is ratiometric within this specified excitation range.
- Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
- Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.
- Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
- Accuracy (error budget) consists of the following:
 - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
 - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
 - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25°C.
 - TcSpan: Output deviation over the temperature range of 0° to 85°C, relative to 25°C.
 - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 0° to 85°C, relative to 25°C.
 - Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V_{FSS} , at 25°C.
- Response Time is defined as the time for the incremental change in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
- Warm-up Time is defined as the time required for the product to meet the specified output voltage after the Pressure has been stabilized.
- Offset Stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the Differential or Gauge configuration in the basic chip carrier (Case 482). A gel die coat isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm.

The MPVZ5010G series pressure sensor operating characteristics, internal reliability and qualification tests are based on use of dry air as the pressure media. Media, other

than dry air, may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the integrated sensor to the A/D input of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 shows the sensor output signal relative to pressure input. Typical, minimum, and maximum output curves are shown for operation over a temperature range of 0° to 85°C using the decoupling circuit shown in Figure 3. The output will saturate outside of the specified pressure range.

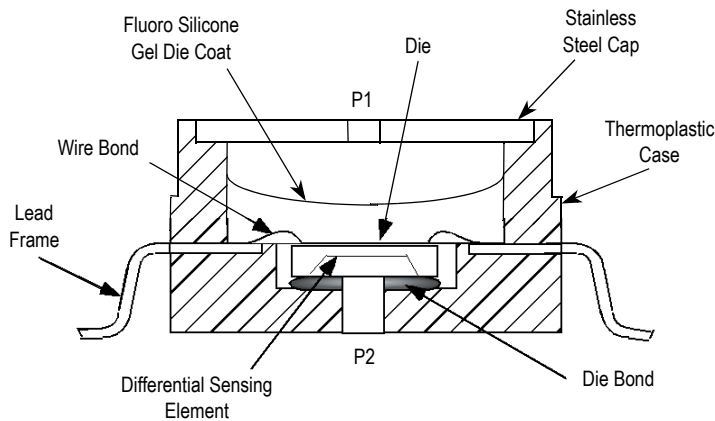


Figure 2. Cross-Sectional Diagram SOP (not to scale)

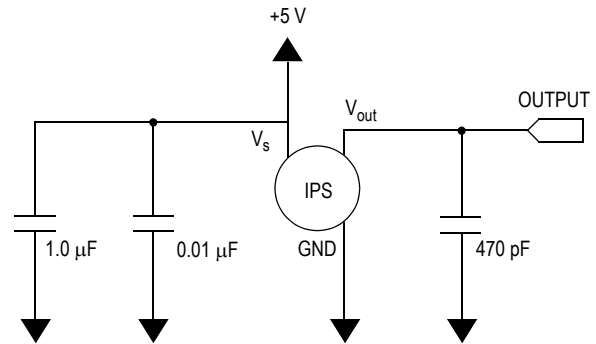


Figure 3. Recommended Power Supply Decoupling and Output Filtering
(For additional output filtering, please refer to Application Note AN1646.)

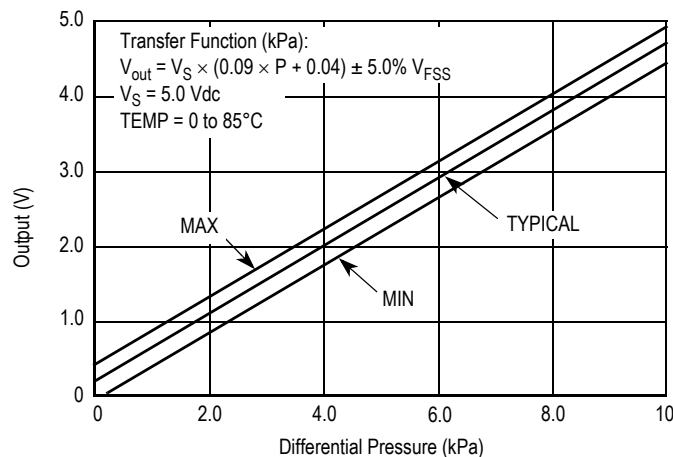


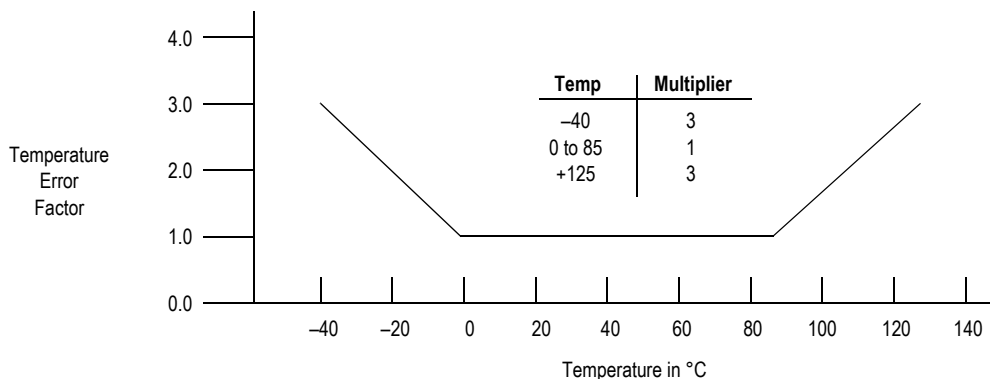
Figure 4. Output versus Pressure Differential

Transfer Function (MPVZ5010G)

Nominal Transfer Value: $V_{out} = V_S \times (0.09 \times P + 0.04)$
 $\pm (\text{Pressure Error} \times \text{Temp. Factor} \times 0.09 \times V_S)$
 $V_S = 5.0 \text{ V} \pm 0.25 \text{ Vdc}$
 $P = \text{kPa}$

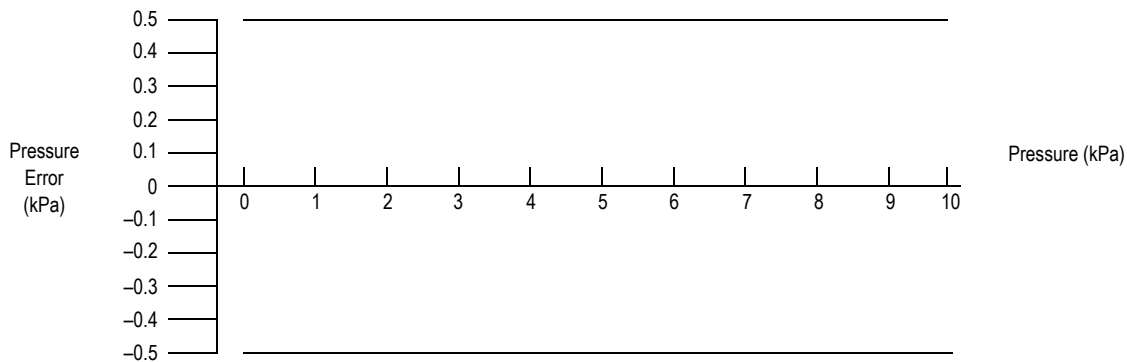
Temperature Error Band

MPVZ5010G SERIES



NOTE: The Temperature Multiplier is a linear response from 0° to -40°C and from 85° to 125°C.

Pressure Error Band



| Pressure | Error (Max) |
|---------------|-------------|
| 0 to 10 (kPa) | ±0.5 (kPa) |

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing a gel die coat which protects the die from harsh media. The MPX pressure sensor

is designed to operate with positive differential pressure applied, $P1 > P2$.

The Pressure (P1) side may be identified by using the table below:

| Part Number | Case Type | Pressure (P1) Side Identifier |
|----------------|-----------|-------------------------------|
| MPVZ5010GW6U | 1735-01 | Vertical Port Attached |
| MPVZ5010GW7U | 1560-02 | Vertical Port Attached |
| MPVZ5010G6U/T1 | 482-01 | Stainless Steel Cap |
| MPVZ5010G7U | 482B-03 | Stainless Steel Cap |

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct

footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

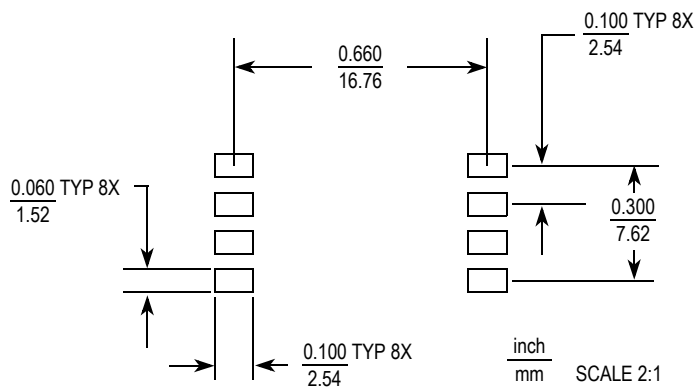
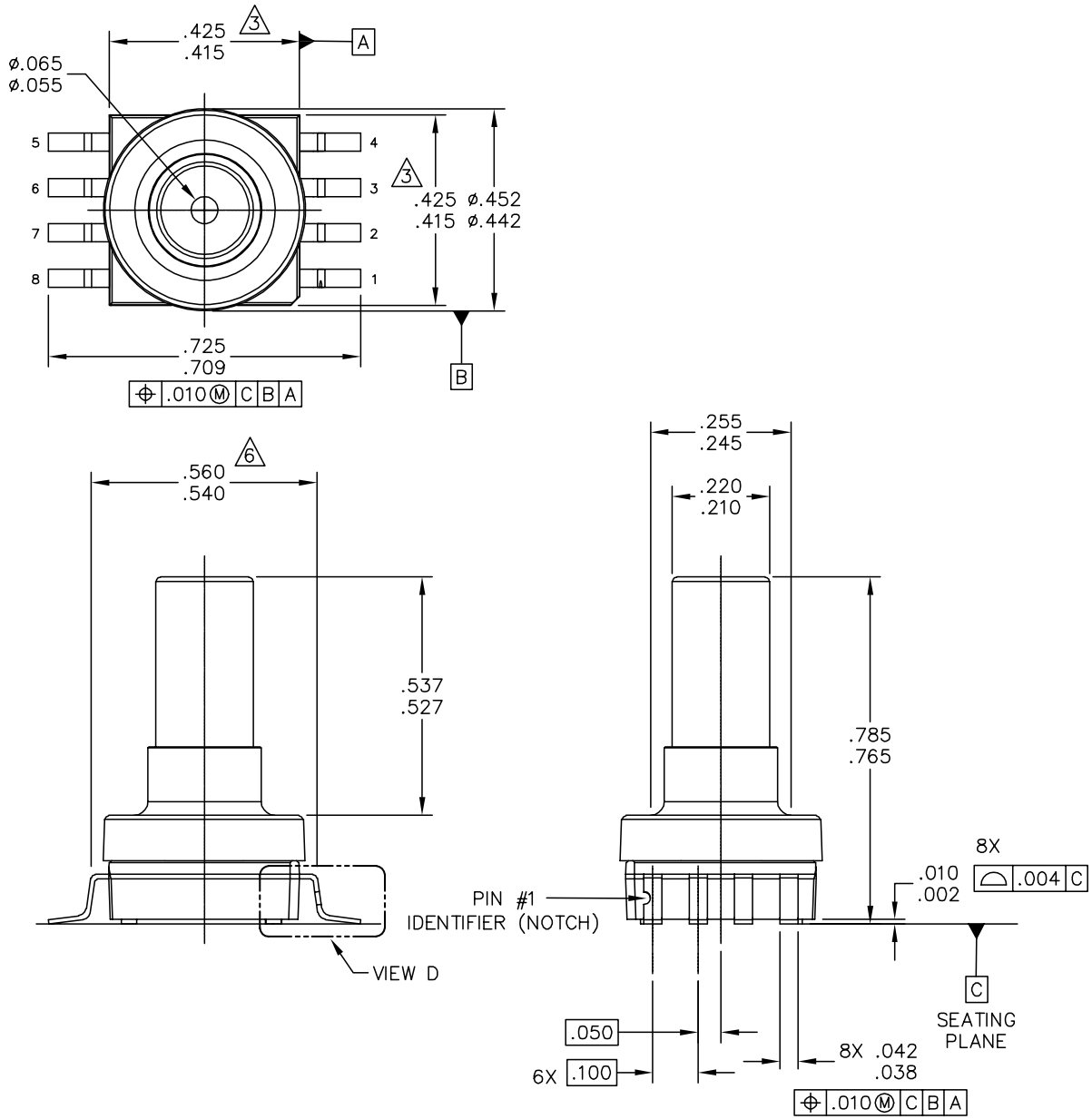


Figure 5. SOP Footprint (Case 482)

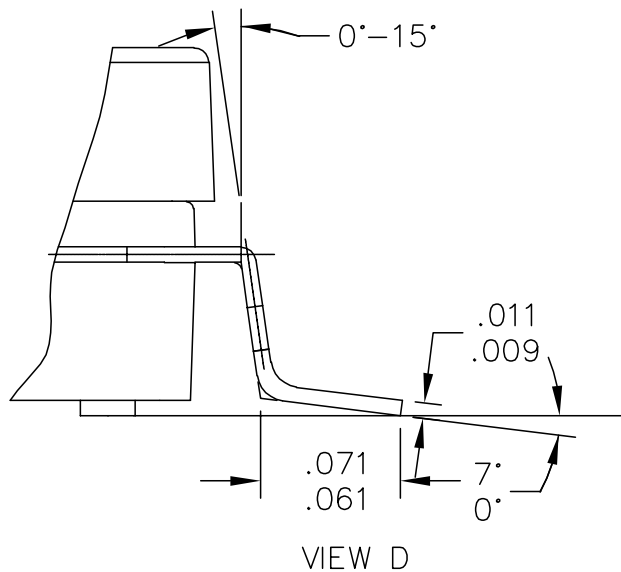
PACKAGE DIMENSIONS



| | | | |
|---|---------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH | DOCUMENT NO: 98ASA10686D | REV: A | |
| | CASE NUMBER: 1735-01 | 16 AUG 2005 | |
| | STANDARD: NON-JEDEC | | |

**CASE 1735-01
ISSUE A
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



| | | | |
|---|---------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH | DOCUMENT NO: 98ASA10686D | REV: A | |
| | CASE NUMBER: 1735-01 | 18 AUG 2005 | |
| | STANDARD: NON-JEDEC | | |

**CASE 1735-01
ISSUE A
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

NOTES:

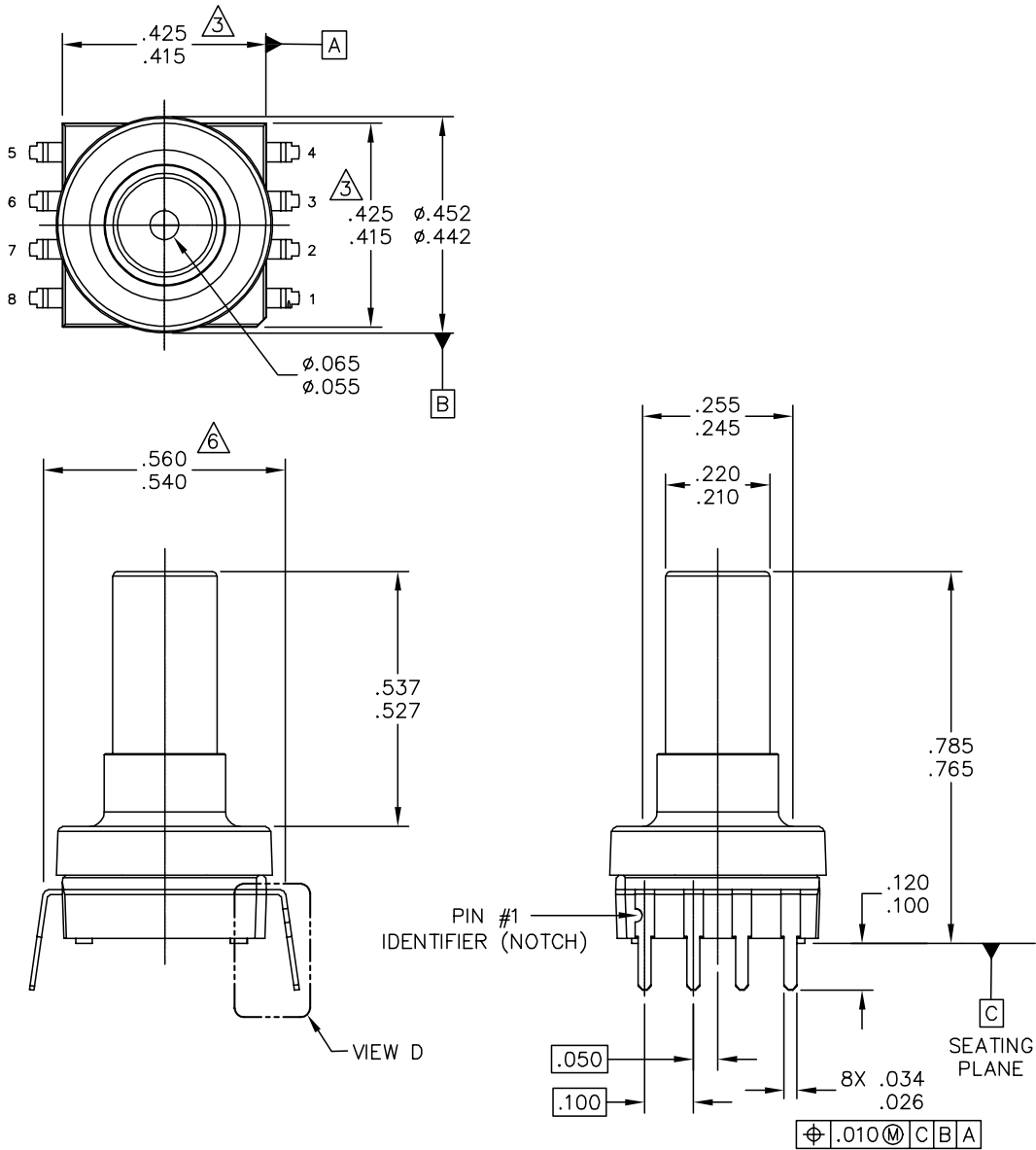
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION IS .006.
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

| | | | |
|---|---------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH | DOCUMENT NO: 98ASA10686D | REV: A | |
| | CASE NUMBER: 1735-01 | 18 AUG 2005 | |
| | STANDARD: NON-JEDEC | | |

PAGE 3 OF 3

**CASE 1735-01
ISSUE A
SMALL OUTLINE PACKAGE**

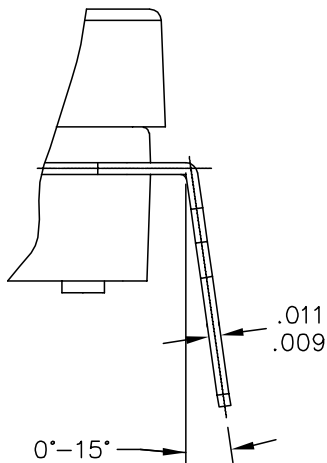
PACKAGE DIMENSIONS



| | | |
|---|---------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH | DOCUMENT NO: 98ASA10611D | REV: C |
| | CASE NUMBER: 1560-02 | 26 MAY 2005 |
| | STANDARD: NON-JEDEC | |

**CASE 1560-02
ISSUE C
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS



VIEW D

| | | | |
|---|---------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH | DOCUMENT NO: 98ASA10611D | REV: C | |
| | CASE NUMBER: 1560-02 | 26 MAY 2005 | |
| | STANDARD: NON-JEDEC | | |

PAGE 2 OF 3

**CASE 1560-02
ISSUE C
SMALL OUTLINE PACKAGE**

PACKAGE DIMENSIONS

NOTES:

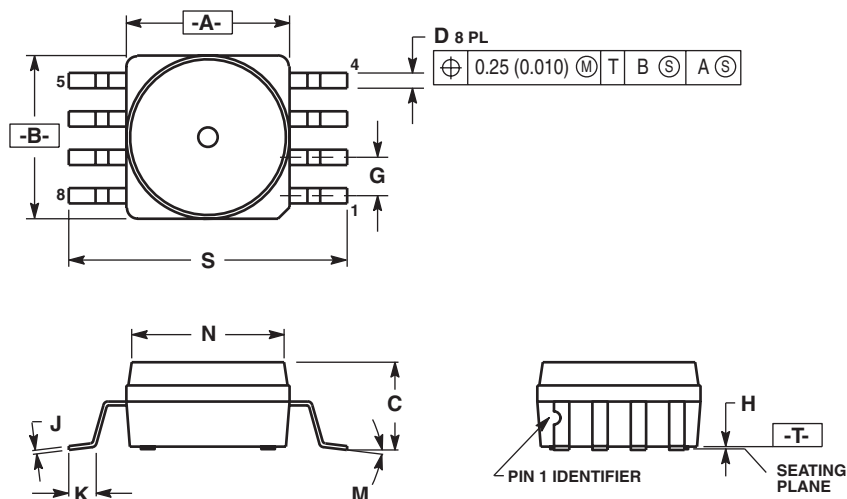
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION IS .006.
- 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
- 6. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

| | | | |
|---|---------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: SO, 8 I/O, .420 X .420 PKG, .100 IN PITCH | DOCUMENT NO: 98ASA10611D | REV: C | |
| | CASE NUMBER: 1560-02 | 26 MAY 2005 | |
| | STANDARD: NON-JEDEC | | |

PAGE 3 OF 3

**CASE 1560-02
ISSUE C
SMALL OUTLINE PACKAGE**

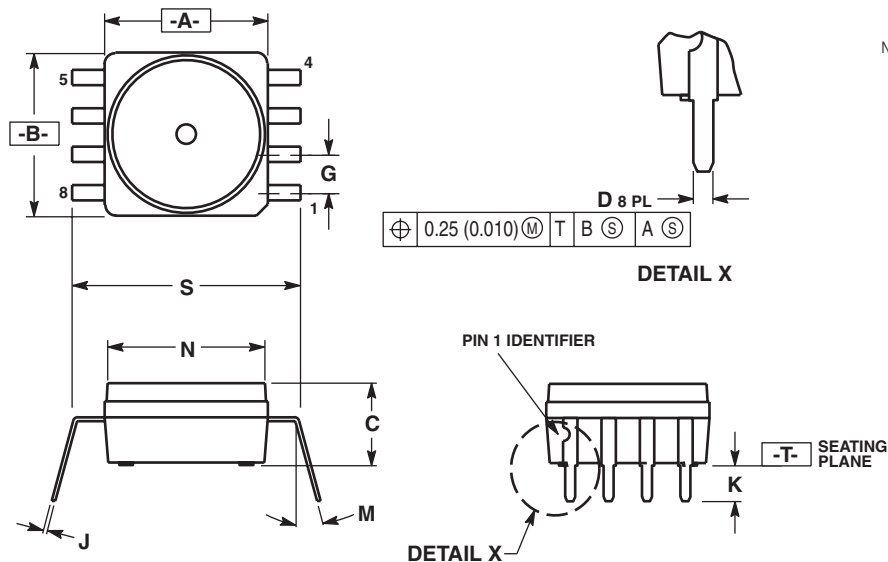
PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.415 | 0.425 | 10.54 | 10.79 |
| B | 0.415 | 0.425 | 10.54 | 10.79 |
| C | 0.212 | 0.230 | 5.38 | 5.84 |
| D | 0.038 | 0.042 | 0.96 | 1.07 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.002 | 0.010 | 0.05 | 0.25 |
| J | 0.009 | 0.011 | 0.23 | 0.28 |
| K | 0.061 | 0.071 | 1.55 | 1.80 |
| M | 0" | 7" | 0" | 7" |
| N | 0.405 | 0.415 | 10.29 | 10.54 |
| S | 0.709 | 0.725 | 18.01 | 18.41 |

**CASE 482-01
ISSUE O
SMALL OUTLINE PACKAGE**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
 6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.415 | 0.425 | 10.54 | 10.79 |
| B | 0.415 | 0.425 | 10.54 | 10.79 |
| C | 0.210 | 0.220 | 5.33 | 5.59 |
| D | 0.026 | 0.034 | 0.66 | 0.864 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.009 | 0.011 | 0.23 | 0.28 |
| K | 0.100 | 0.120 | 2.54 | 3.05 |
| M | 0" | 15" | 0" | 15" |
| N | 0.405 | 0.415 | 10.29 | 10.54 |
| S | 0.540 | 0.560 | 13.72 | 14.22 |

**CASE 482B-03
ISSUE B
SMALL OUTLINE PACKAGE**

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005. All rights reserved.