

MC10211

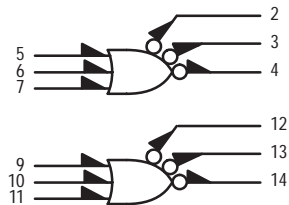
Dual 3-Input/3-Output NOR Gate

The MC10211 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the MC10211 particularly useful in clock distribution applications where minimum clock skew is desired.

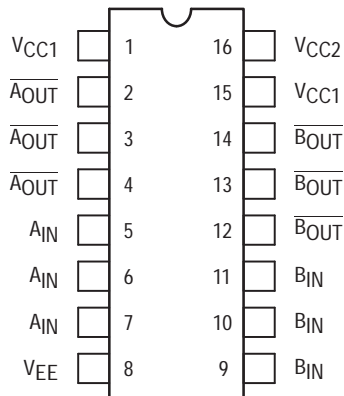
- $P_D = 160 \text{ mW typ/pkg (No Loads)}$
- $t_{pd} = 1.5 \text{ ns typ (All Output Loaded)}$
- $t_r, t_f = 1.5 \text{ ns typ (20\%–80\%)}$

LOGIC DIAGRAM



$V_{CC1} = \text{PIN } 1, 15$
 $V_{CC2} = \text{PIN } 16$
 $V_{EE} = \text{PIN } 8$

DIP PIN ASSIGNMENT



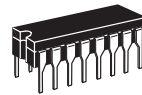
Pin assignment is for Dual-in-Line Package.
 For PLCC pin assignment, see the Pin Conversion Tables on page 18.



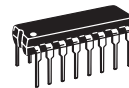
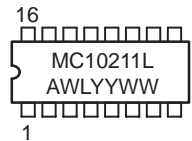
ON Semiconductor

<http://onsemi.com>

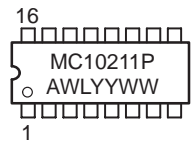
MARKING DIAGRAMS



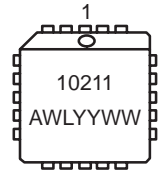
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648



PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10211L	CDIP-16	25 Units / Rail
MC10211P	PDIP-16	25 Units / Rail
MC10211FN	PLCC-20	46 Units / Rail

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit	
			-30°C		+25°C			+85°C			
			Min	Max	Min	Typ	Max	Min	Max		
Power Supply Drain Current	I_E	8		42		30	38		42	mAdc	
Input Current	I_{inH}	5, 6, 7		650			410		410	μ Adc	
	I_{inL}	5, 6, 7	0.5		0.5			0.3		μ Adc	
Output Voltage Logic 1	V_{OH}	2	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	
		3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		
		4	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700		
Output Voltage Logic 0	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	
		3	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		
		4	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615		
Threshold Voltage Logic 1	V_{OHA}	2	-1.080		-0.980			-0.910		Vdc	
		3	-1.080		-0.980			-0.910			
		4	-1.080		-0.980			-0.910			
Threshold Voltage Logic 0	V_{OLA}	2		-1.655			-1.630		-1.595	Vdc	
		3		-1.655			-1.630		-1.595		
		4		-1.655			-1.630		-1.595		
Switching Times (50 Ω Load)										ns	
Propagation Delay	t_{5+2-}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8		
		t_{5-2+}	2	1.0	2.6	1.0	1.5	2.5	1.0		2.8
		t_{5+3-}	3	1.0	2.6	1.0	1.5	2.5	1.0		2.8
		t_{5-3+}	3	1.0	2.6	1.0	1.5	2.5	1.0		2.8
		t_{5+4-}	4	1.0	2.6	1.0	1.5	2.5	1.0		2.8
		t_{5-4+}	4	1.0	2.6	1.0	1.5	2.5	1.0		2.8
Rise Time (20 to 80%)	t_{2+}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8		
		t_{3+}	3	1.0	2.6	1.0	1.5	2.5	1.0		2.8
		t_{4+}	4	1.0	2.6	1.0	1.5	2.5	1.0		2.8
Fall Time (20 to 80%)	t_{2-}	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8		
		t_{3-}	3	1.0	2.6	1.0	1.5	2.5	1.0		2.8
		t_{4-}	4	1.0	2.6	1.0	1.5	2.5	1.0		2.8

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ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature -30°C +25°C +85°C			TEST VOLTAGE VALUES (Volts)					(V _{CC}) Gnd
			V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
			-0.890	-1.890	-1.205	-1.500	-5.2	
			-0.810	-1.850	-1.105	-1.475	-5.2	
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V _{CC}) Gnd
Characteristic	Symbol	Pin Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
Power Supply Drain Current	I _E	8					8	1, 15, 16
Input Current	I _{inH}	5, 6, 7	*				8	1, 15, 16
	I _{inL}	5, 6, 7		*			8	1, 15, 16
Output Voltage Logic 1	V _{OH}	2					8	1, 15, 16
		3					8	1, 15, 16
		4					8	1, 15, 16
Output Voltage Logic 0	V _{OL}	2	5				8	1, 15, 16
		3	6				8	1, 15, 16
		4	7				8	1, 15, 16
Threshold Voltage Logic 1	V _{OHA}	2				5	8	1, 15, 16
		3				6	8	1, 15, 16
		4				7	8	1, 15, 16
Threshold Voltage Logic 0	V _{OLA}	2			5		8	1, 15, 16
		3			6		8	1, 15, 16
		4			7		8	1, 15, 16
Switching Times (50Ω Load)					Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t ₅₊₂₋ t ₅₋₂₊ t ₅₊₃₋ t ₅₋₃₊ t ₅₊₄₋ t ₅₋₄₊	2			5	2	8	1, 15, 16
		2			5	2	8	1, 15, 16
		3			5	3	8	1, 15, 16
		3			5	3	8	1, 15, 16
		4			5	4	8	1, 15, 16
		4			5	4	8	1, 15, 16
Rise Time (20 to 80%)	t ₂₊ t ₃₊ t ₄₊	2			5	2	8	1, 15, 16
		3			5	3	8	1, 15, 16
		4			5	4	8	1, 15, 16
Fall Time (20 to 80%)	t ₂₋ t ₃₋ t ₄₋	2			5	2	8	1, 15, 16
		3			5	3	8	1, 15, 16
		4			5	4	8	1, 15, 16

* Individually test each input using the pin connections shown.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.