

# 74ABT125

Quad buffer; 3-state

Rev. 8 — 30 June 2021

Product data sheet

## 1. General description

The 74ABT125 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ( $n\overline{OE}$ ). A HIGH on  $n\overline{OE}$  causes the outputs to assume a high impedance OFF-state. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Power-up 3-state
- Inputs are disabled during 3-state mode
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- Quad bus interface
- 3-state buffers
- Live insertion and extraction permitted
- Output capability: HIGH -32 mA; LOW +64 mA
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74ABT125BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

### 4. Functional diagram

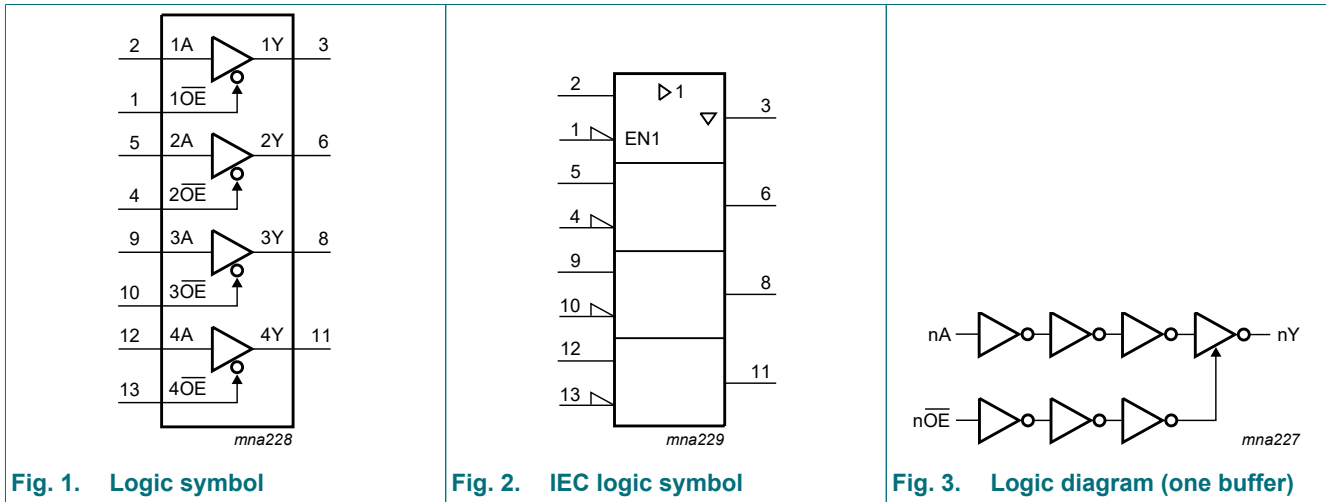


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one buffer)

### 5. Pinning information

#### 5.1. Pinning

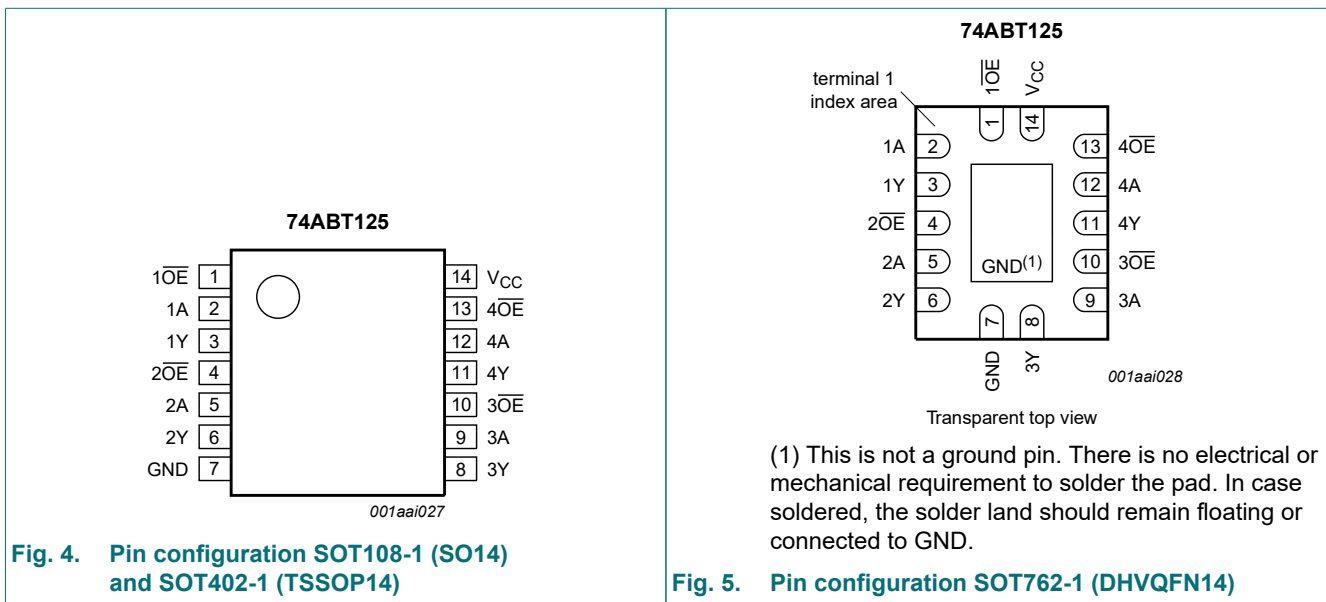


Fig. 4. Pin configuration SOT108-1 (SO14) and SOT402-1 (TSSOP14)

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

#### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function selection**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

Inputs		Output
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1] -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
$T_j$	junction temperature		[2] -	150	°C
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[3] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		4.5	5.5	V
$V_I$	input voltage		0	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	V
$V_{IL}$	LOW-level Input voltage		-	0.8	V
$I_{OH}$	HIGH-level output current		-32	-	mA
$I_{OL}$	LOW-level output current		-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5 \text{ V}$ ; $I_{IK} = -18 \text{ mA}$	-	-0.9	-1.2	-	-1.2	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IL}$ or $V_{IH}$						
		$V_{CC} = 4.5 \text{ V}$ ; $I_{OH} = -3 \text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0 \text{ V}$ ; $I_{OH} = -3 \text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5 \text{ V}$ ; $I_{OH} = -32 \text{ mA}$	2.0	2.4	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5 \text{ V}$ ; $I_{OL} = 64 \text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	-	0.35	0.55	-	0.55	V
$I_I$	input leakage current	$V_{CC} = 5.5 \text{ V}$ ; $V_I = \text{GND}$ or $5.5 \text{ V}$	-	$\pm 0.01$	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0.0 \text{ V}$ ; $V_I$ or $V_O \leq 4.5 \text{ V}$	-	$\pm 5.0$	$\pm 100$	-	$\pm 100$	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.1 \text{ V}$ ; $V_O = 0.5 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{OE} = \text{don't care}$ [1]	-	$\pm 5.0$	$\pm 50$	-	$\pm 50$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5 \text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$						
		$V_O = 2.7 \text{ V}$	-	1.0	50	-	50	$\mu\text{A}$
		$V_O = 0.5 \text{ V}$	-	-1.0	-50	-	-50	$\mu\text{A}$
$I_{CEX}$	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V}$ ; $V_{CC} = 5.5 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$	-	5.0	50	-	50	$\mu\text{A}$
$I_O$	output current	$V_{CC} = 5.5 \text{ V}$ ; $V_O = 2.5 \text{ V}$ [2]	-50	-100	-180	-50	-180	mA
$I_{CC}$	supply current	$V_{CC} = 5.5 \text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$						
		outputs HIGH-state	-	65	250	-	250	$\mu\text{A}$
		outputs LOW-state	-	12	15	-	30	mA
		outputs disabled	-	65	250	-	50	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per control pin; $V_{CC} = 5.5 \text{ V}$ ; one control input at $3.4 \text{ V}$ , other inputs at $V_{CC}$ or $\text{GND}$ [3]						
		outputs enabled	-	0.5	1.5	-	1.5	mA
		outputs disabled	-	50	250	-	250	mA
		one enable input at $3.4 \text{ V}$ and other inputs at $V_{CC}$ or $\text{GND}$ ; outputs disabled	-	0.5	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = 0 \text{ V}$ or $V_{CC}$	-	4	-	-	-	pF
$C_O$	output capacitance	outputs disabled; $V_O = 0 \text{ V}$ or $V_{CC}$	-	7	-	-	-	pF

[1] This parameter is valid for any  $V_{CC}$  between  $0 \text{ V}$  and  $2.1 \text{ V}$ , with a transition time of up to  $10 \text{ ms}$ .

From  $V_{CC} = 2.1 \text{ V}$  to  $V_{CC} = 5 \text{ V} \pm 10 \%$ , a transition time of up to  $100 \mu\text{s}$  is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at  $3.4 \text{ V}$ .

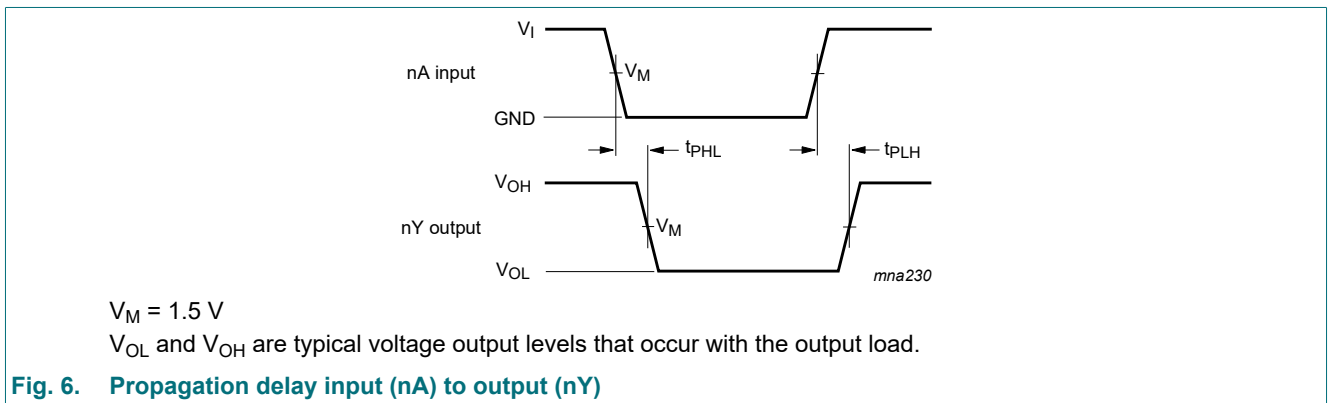
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ . Test circuit is shown in [Fig. 8](#).

Symbol	Parameter	Conditions	25 °C; $V_{CC} = 5.0\text{ V}$			-40 °C to +85 °C; $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$	LOW to HIGH propagation delay	nA to nY, see <a href="#">Fig. 6</a>	1.0	2.8	4.1	1.0	4.6	ns
$t_{PHL}$	HIGH to LOW propagation delay	nA to nY; see <a href="#">Fig. 6</a>	1.0	3.1	4.6	1.0	4.9	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$\overline{nOE}$ to nY; see <a href="#">Fig. 7</a>	1.0	3.2	5.0	1.0	5.9	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$\overline{nOE}$ to nY; see <a href="#">Fig. 7</a>	1.0	4.2	6.2	1.0	6.8	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$\overline{nOE}$ to nY; see <a href="#">Fig. 7</a>	1.0	4.1	5.4	1.0	6.2	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$\overline{nOE}$ to nY; see <a href="#">Fig. 7</a>	1.5	2.8	5.0	1.5	5.5	ns

### 10.1. Waveforms and test circuit



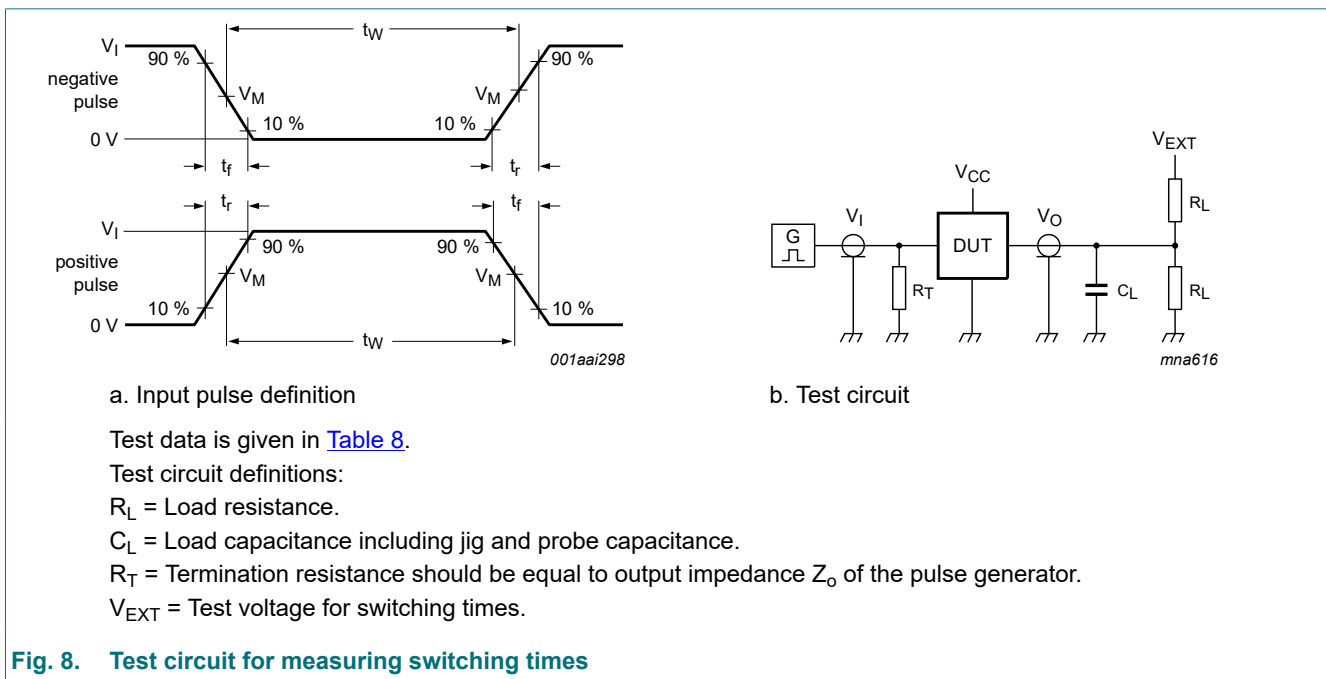
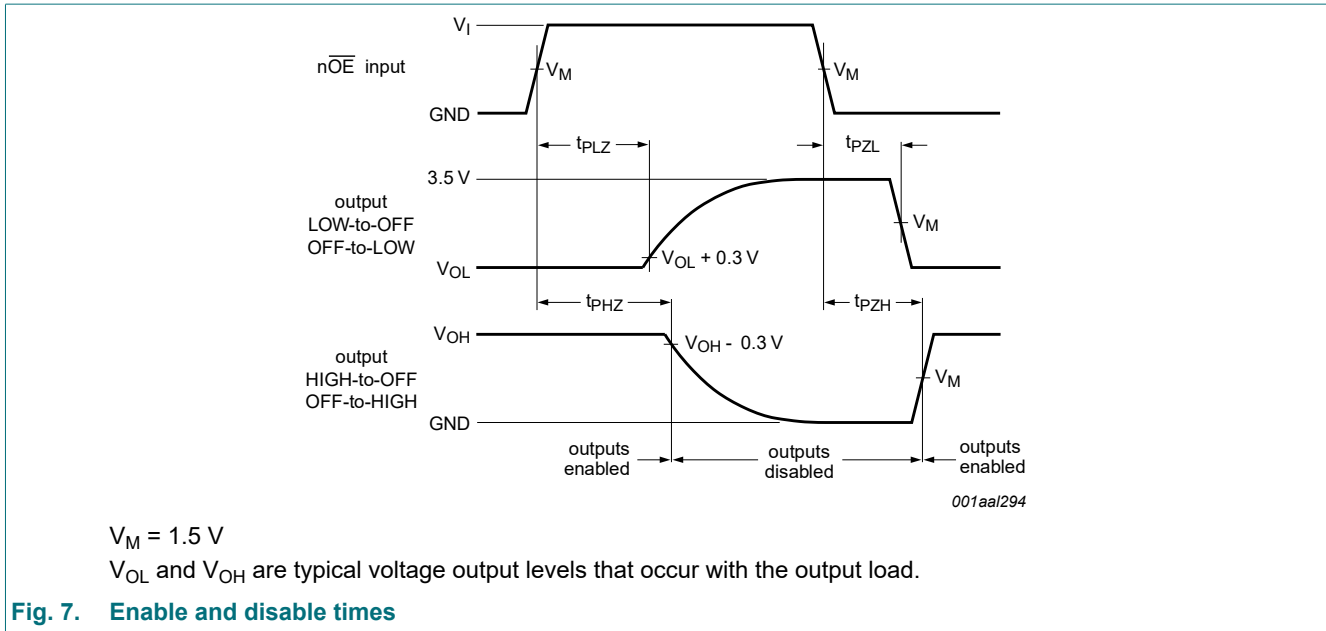


Table 8. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
3.0 V	1 MHz	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 $\Omega$	open	open	7.0 V

### 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 9. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 10. Package outline SOT402-1 (TSSOP14)



DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 11. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT125 v.8	20210630	Product data sheet	-	74ABT125 v.7
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74ABT125DB (SOT337-1/SSOP14) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74ABT125 v.7	20151125	Product data sheet	-	74ABT125 v.6
Modifications:	<ul style="list-style-type: none"> <li>Type number 74ABT125N (SOT27-1) removed.</li> </ul>			
74ABT125 v.6	20111103	Product data sheet	-	74ABT125 v.5
Modifications:	<ul style="list-style-type: none"> <li>Legal pages updated</li> </ul>			
74ABT125 v.5	20101124	Product data sheet	-	74ABT125 v.4
74ABT125 v.4	20100427	Product data sheet	-	74ABT125 v.3
74ABT125 v.3	20080429	Product data sheet	-	74ABT125 v.2
74ABT125 v.2	19980116	Product specification	-	74ABT125 v.1
74ABT125 v.1	19960305	-	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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