Preliminary

Am29C985

9-Bit x 4-Port Multiple Bus Exchange with Parity

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Four bidirectional I/O ports**
  - Replaces several bidirectional latched transceivers
  - Permits multiple bus communication
  - Allows two independent communication channels
  - TTL compatibility
- **9 bit-wide ports to handle byte parity**
- **Parity check/generate at all ports**
  - Odd parity
- **Additional output bus check**
  - Compares bus with driver inputs
- **Two selection inputs per port**
  - Independent port interconnect control
  - Increased flexibility in data routing
- **Matched port decoding**
  - Simplifies external decode logic
  - Easily cascadable for wider buses
- **Power-Up/Down disable**
  - No power-up sequencing needed
  - Ideal for card-edge interface
- **48 mA output drive**
  - High-capacitance bus driving
- **High-performance CMOS**
  - Low stand-by power consumption
  - 6 ns (typ.) port-to-port delay
  - 7 ns (typ.) select-to-port delay
- **Available in 68-pin PLCC, LCC and PGA packages**
  - Significant savings in board space
- **Proprietary output circuit minmizes ground bounce**
- **3-State during power off condition**

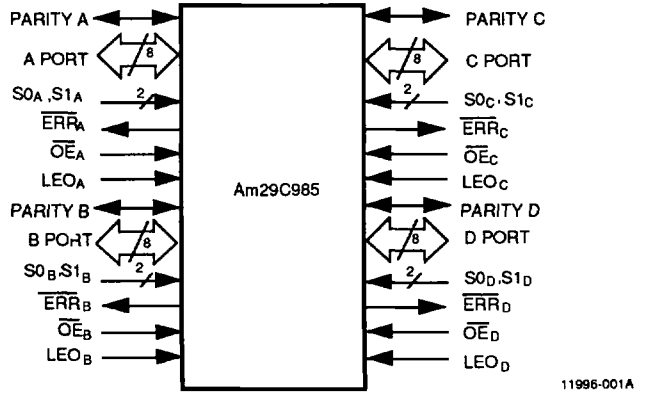
GENERAL DESCRIPTION

The Am29C985 is a high-speed Multiple Bus Exchange device. It is organized as four 9-bit wide TTL-compatible I/O ports with Output Enable control for each port. Any port can serve either as a source (Input) port or as a destination (Output) port. When the output drivers of a port are disabled (high-impedance state), the port serves as a source port. When the drivers are enabled, the port serves as a destination port. Source port selection is made by two independent Select inputs at each port. This organization offers flexibility in implementing the Am29C985 as a digital cross-point switch for multiple bus communication in a multiprocessing environment.

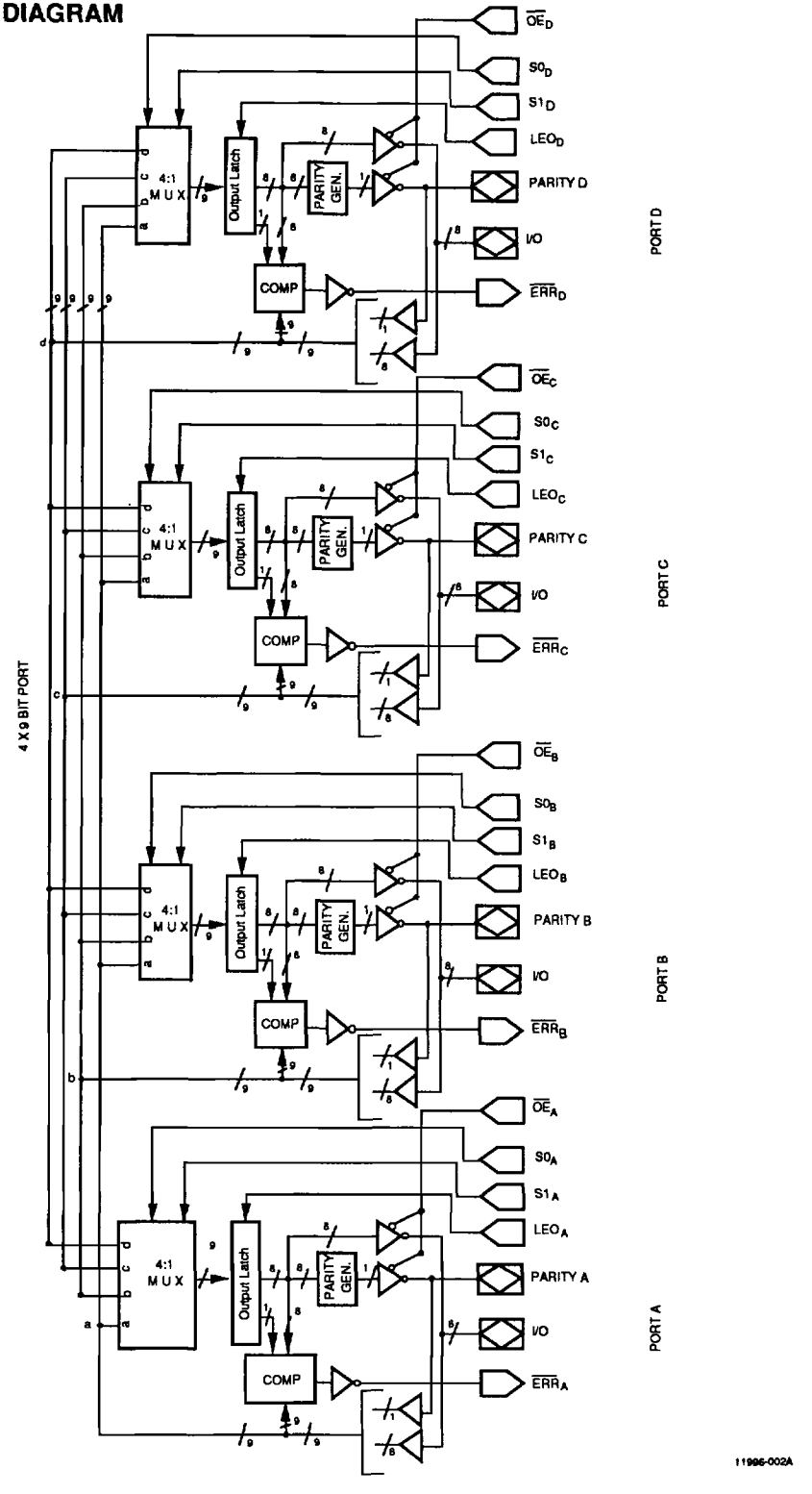
The Am29C985 incorporates parity check and generation capabilities on all four output ports. Each output port is capable of generating odd parity on byte-wide input data. Accordingly, parity check is accomplished at each output on incoming 9 bit parity data. A unique comparison scheme also performs a bus check by comparing the data driven onto the bus with the input data received at the internal multiplexers thus detecting stuck bus bits.

Each I/O port has an output latch to capture outgoing data. All output latches are independently controlled by active HIGH Output Latch Enable inputs. This feature can be used to perform stored operation for byte-word compression and expansion to communicate between buses of different widths. Independent port control permits cascading of Am29C985s for wide buses. All I/O ports go into high impedance state upon power down. This feature makes the device ideally suited for card-edge applications.

SIMPLIFIED BLOCK DIAGRAM



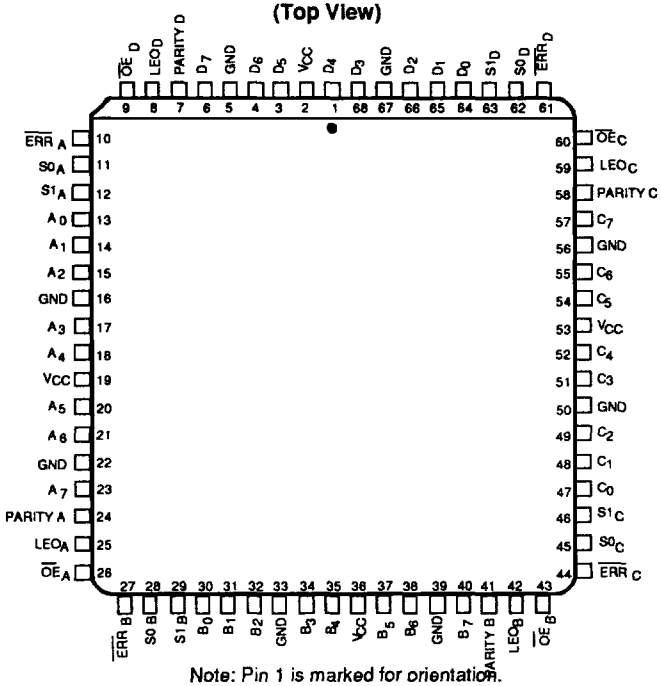
DETAILED BLOCK DIAGRAM



CONNECTION DIAGRAMS

PLCC*

(Top View)



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Note: Pin 1 is marked for orientation.

*Also available in 68-pin LCC; pinout identical to PLCC.

PGA

(Bottom View)

	A	B	C	D	E	F	G	H	J	K	L
1		PARITY D	GND	D_5	D_4	GND	D_2	D_0	$S0_D$	$\overline{OE}_C$	
2	$\overline{OE}_D$	LEO_D	D_7	D_6	V_{CC}	D_3	D_1	$S1_D$	$\overline{ERR}_D$	LEO_C	C_6
3	$S0_A$	$\overline{ERR}_A$								C_7	GND
4	A_0	$S1_A$							PARITY C		C_5
5	A_2	A_5								C_4	V_{CC}
6	A_3	GND								C_3	GND
7	A_4	V_{CC}								C_1	C_2
8	A_5	A_6								$S1_C$	C_0
9	GND	A_7								$\overline{ERR}_C$	$S0_C$
10	PARITY A	LEO_A	$\overline{ERR}_B$	$S1_B$	B_1	B_3	V_{CC}	B_6	B_7	LEO_B	$\overline{OE}_B$
11		$\overline{OE}_A$	$S0_B$	B_0	B_2	GND	B_4	B_5	GND	PARITY B	

Note: Notch indicates orientation.

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PGA PACKAGE

PIN DESIGNATIONS

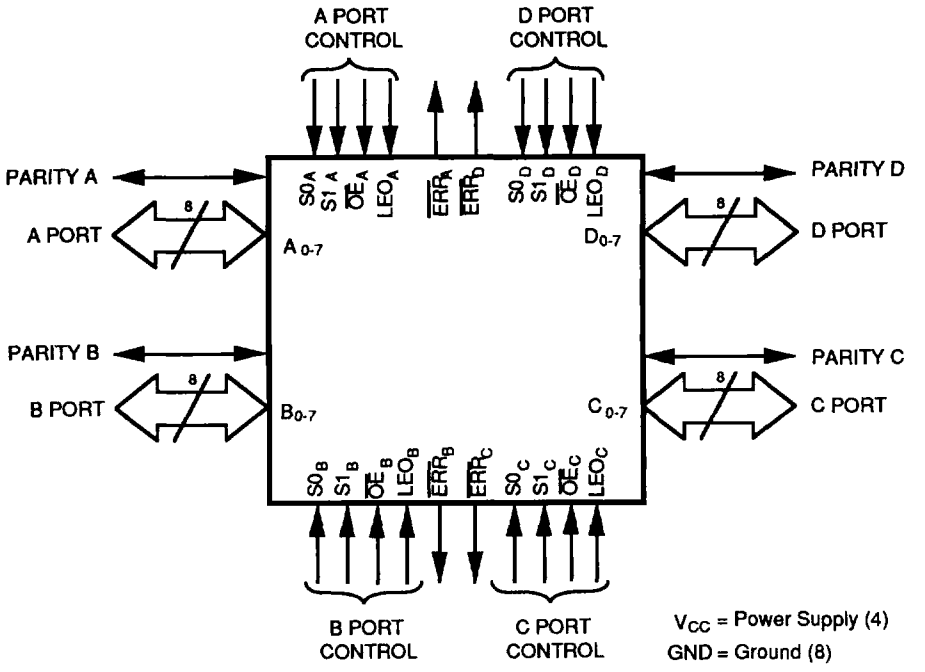
(Sorted by Pin Name)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A-4	A_0	K-11	PARITY B	C-2	D_7	B-2	LEO_D
B-5	A_1	L-8	C_0	B-1	PARITY D	B-11	$\overline{OE}_A$
A-5	A_2	K-7	C_1	A-9	GND	L-10	$\overline{OE}_B$
A-6	A_3	L-7	C_2	B-6	GND	K-1	$\overline{OE}_C$
A-7	A_4	K-6	C_3	C-1	GND	A-2	$\overline{OE}_D$
A-8	A_5	K-5	C_4	F-1	GND	A-3	$S0_A$
B-8	A_6	L-4	C_5	F-11	GND	C-11	$S0_B$
B-9	A_7	K-4	C_6	J-11	GND	L-9	$S0_C$
A-10	PARITY A	K-3	C_7	L-3	GND	J-1	$S0_D$
D-11	B_0	L-2	PARITY C	L-6	GND	B-4	$S1_A$
E-10	B_1	H-1	D_0	B-3	$\overline{ERR}_A$	D-10	$S1_B$
E-11	B_2	G-2	D_1	C-10	$\overline{ERR}_B$	K-8	$S1_C$
F-10	B_3	G-1	D_2	K-9	$\overline{ERR}_C$	H-2	$S1_D$
G-11	B_4	F-2	D_3	J-2	$\overline{ERR}_D$	B-7	V_{CC}
H-11	B_5	E-1	D_4	B-10	LEO_A	E-2	V_{CC}
H-10	B_6	D-1	D_5	K-10	LEO_B	G-10	V_{CC}
J-10	B_7	D-2	D_6	K-2	LEO_C	L-5	V_{CC}

(Sorted by Pin Number)

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A-2	$\overline{OE}_D$	B-9	A_7	F-10	B_3	K-4	C_6
A-3	$S0_A$	B-10	LEO_A	F-11	GND	K-5	C_4
A-4	A_0	B-11	$\overline{OE}_A$	G-1	D_2	K-6	C_3
A-5	A_2	C-1	GND	G-2	D_1	K-7	C_1
A-6	A_3	C-2	D_7	G-10	V_{CC}	K-8	$S1_C$
A-7	A_4	C-10	$\overline{ERR}_B$	G-11	B_4	K-9	$\overline{ERR}_C$
A-8	A_5	C-11	$S0_B$	H-1	D_0	K-10	LEO_B
A-9	GND	D-1	D_5	H-2	$S1_D$	K-11	PARITY B
A-10	PARITY A	D-2	D_6	H-10	B_6	L-2	PARITY C
B-1	PARITY D	D-10	$S1_B$	H-11	B_5	L-3	GND
B-2	LEO_D	D-11	B_0	J-1	$S0_D$	L-4	C_5
B-3	$\overline{ERR}_A$	E-1	D_4	J-2	$\overline{ERR}_D$	L-5	V_{CC}
B-4	$S1_A$	E-2	V_{CC}	J-10	B_7	L-6	GND
B-5	A_1	E-10	B_1	J-11	GND	L-7	C_2
B-6	GND	E-11	B_2	K-1	$\overline{OE}_C$	L-8	C_0
B-7	V_{CC}	F-1	GND	K-2	LEO_C	L-9	$S0_C$
B-8	A_6	F-2	D_3	K-3	C_7	L-10	$\overline{OE}_B$

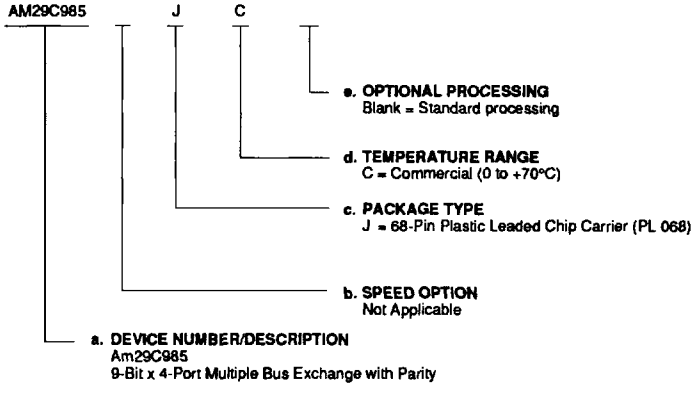
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range



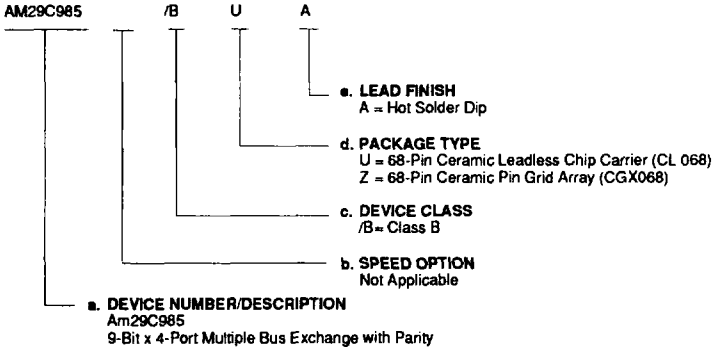
Valid Combinations

Valid Combinations	
AM29C985	JC

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations

Valid Combinations	
AM29C985	/BUA, /BZA

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A_I, B_I, C_I, and D_I (I = 0 through 7) Data Bus I/O Ports (Input/Output)
These four groups of eight I/O pins are defined as the A, B, C, and D ports respectively. Each port serves as a source (Input) or as a destination (Output).

PARITY A,PARITY B, PARITY C and PARITY D Parity Flag (Input/Output, Three-state)
As an input, parity and port are combined and checked for odd parity. As an output, parity is an active output indicating odd parity for port.

SI_A, SI_B, SI_C, and SI_D (I = 0, 1) Source Port Select (Inputs)
Each pair of inputs determines the source of data for the corresponding I/O port when used as a destination port.

$\overline{ERR}_A$, $\overline{ERR}_B$, $\overline{ERR}_C$ and $\overline{ERR}_D$ $\overline{ERROR}$ (Output, open drain)
Each output pin is used to flag Parity/Bus errors. Error is indicated by a LOW output.

LEO_A, LEO_B, LEO_C, and LEO_D Output Latch Enable (Inputs; Active HIGH)
Each LEO input controls a 9-bit wide latch on the output side of the corresponding I/O port. The latches are transparent when LEO is HIGH and are latched when LEO is LOW.

$\overline{OE}_A$, $\overline{OE}_B$, $\overline{OE}_C$, and $\overline{OE}_D$ Output Enable (Inputs; Active LOW)
Each $\overline{OE}$ input controls the bus drivers of the corresponding I/O port. When $\overline{OE}$ is LOW, data at the output of the Output latches is passed to the bus. When $\overline{OE}$ is HIGH, the bus outputs are in high-impedance state.

Am29C985 OPERATIONAL DESCRIPTION

Parity and bus checking are provided on the Am29C985. Parity checking and generation are both performed at the output. In order to preserve parity coverage through the part, the data driven onto the bus, including the generated parity, is compared to the data passing through the multiplexer, including the old parity. This has two effects: The comparison of the parity bits acts as a parity check. Also bus errors will be detected if the bus data does not agree with the data being driven.

Minimization of Ground Bounce through Output Edge-Rate Control

The Am29C985 incorporates AMD's proprietary edge controlled outputs in order to minimize simultaneous switching noise (ground bounce). By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in specified device propagation delay.

Power-Up/Down Disable

The Am29C985 contains a unique power up/down circuit to provide glitch free outputs during power-supply sequencing. This power-up circuit ensures that at low V_{CC} values (typically 0–2.0 V), the outputs are disabled and in 3-state. At V_{CC} values above this threshold, the outputs will remain disabled and not glitch to an active state if the appropriate output-enable inputs are conditioned for 3-state functionality. At V_{CC} values above the disable circuitry threshold, if the output-enable inputs are conditioned active (outputs enabled), the outputs will respond to a steady state input value. Additionally, the outputs will exhibit high impedance characteristics under power conditioning.

Input/Output Structures

Typical CMOS devices on the market today have maximum DC I/O voltage ratings that prevent some card edge applications, due to the uncertainty of the I/O voltage with respect to V_{CC}. This uncertainty occurs when extracting or replacing a card into a powered-on connector or when a powered-off device is sitting on an active bus. Under these conditions, the maximum rating of –0.5 V to V_{CC} + 0.5 V may be violated. This rating is derived from the presence of a parasitic diode from the input or output to V_{CC}. To prevent forward biasing the diode with an active signal, the 0.5 V limit above V_{CC} was adopted.

AMD has addressed this situation with unique input and output structures. These structures on the Am29C985 use an n-channel pull-up transistor. This results in a stacked n-channel output buffer and a proprietary ESD input cell.

These circuit modifications result in a maximum DC I/O voltage rating of –0.5 V to 7.0 V. The maximum rating is no longer a function of the V_{CC} voltage, thus allowing 3-state functionality under power off condition.

In addition, another benefit gained is that the n-channel pull-up reduces the output HIGH-level voltage for a lightly loaded output to 4.0 V, at V_{CC} = 5.0 Volts. This reduces switching noise and cross-talk associated with typical CMOS full rail-to-rail travel.

FUNCTIONAL DESCRIPTION

The Am29C985 Multiple Bus Exchange consists of four 9-bit I/O ports. Each port has a 9-bit output latch to capture outgoing data. There are four control pins associated with each port: two Select inputs for source port selection, one Output Latch Enable input (active HIGH) to control Output latches, and an active LOW Output Enable line to control the bus driver at the I/O port.

Port Selection and Control

Each port is independently controlled by these four control inputs. If the output drivers of a port are disabled (high-impedance state), that port is an input and can be used as a source port. At the same time, the data at one of the four internal buses can be transferred to the Output latch under the control of the appropriate Select inputs. If the output drivers are enabled, the port serves as a destination port, transporting the data at the output of its Output latch to the external bus connected to the I/O port. Independent control of the Output latch permits stored operation at any port.

Parity and Bus checking

In the Am29C985, parity checking and recognition are both performed at the output. To preserve parity coverage through the part, the data driven onto the bus, including the regenerated parity, is compared to the data passing through the switch, including the old parity. This has two effects: the comparison of parity bits acts as a parity check. Also bus errors will be detected if the bus data does not agree with data being driven to the output buffer.

Error Outputs

$\overline{ERR}$ pins are active LOW, open drain outputs. This allows easy combination of multiple bytes. When passing non-parity data through the part the output will have correct odd parity, but an error may be indicated due to the uncertainty of the 9th bit. Under this condition it is up to the user to ignore the error.

Multiple Bus Communication

Four internal buses serve as pathways for port-to-port connection. By proper choice of source select codes for the ports, the Am29C985 can be configured in different modes for multiple bus communication. In one mode of operation, two ports can be selected as source ports and the other two as destination ports; thus, two independent bidirectional communication channels are established. In another mode, one port can be selected as the source, and one or more of the other ports can serve as destination ports. Any port not intended as a destination port can be disabled (high-impedance state) by its Output Enable control.

TRUTH TABLES

A. Port Source Selection

$S1_n$	$S0_n$	Source
L	L	A Bus
L	H	B Bus
H	L	C Bus
H	H	D Bus

B. Output Latch Operation

LEO_n	Mode
H	Transparent
L	Latched

C. I/O Port Controls

LEO_n	$\overline{OE}_n$	I/O	Source of Data
L	L	Out	Contents of Output Latch
H	L	Out	Selected Source Port
X	H	In	

Key: n = A, B, C, or D
L = LOW
H = HIGH
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	–0.5 to 6.0 V
DC Input Diode Current	
(I_{IK}) (V_{IN} < 0 V)	–20 mA
(V_{IN} > V_{CC} if applicable)	+20 mA
DC Input Voltage (V_{IN})	–0.5 to 7.0 V
DC Output Diode Current	
(I_{OK}) (V_{OUT} < 0 V)	–50 mA
(V_{OUT} > V_{CC} if applicable)	+50 mA
DC Output Current per Output Pin:	
I_{SINK}	+70 mA
I_{SOURCE}	–30 mA
DC Output Voltage (V_{OUT})	–0.5 to 7.0 V
Total DC Ground Current (I_{GND})	1750 mA
Total DC V_{CC} Current (I_{CC})	575 mA
Storage Temperature	–65 to +150°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V
Military (M) and Extended Commercial (E) Devices	
Temperature (T_A)	–55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OH} = –15 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 48 mA COM'L		0.5	V
			I_{OL} = 32 mA MIL			
V_{IH}	Input HIGH Voltage	(Note 1)		2.0		V
V_{IL}	Input LOW Voltage	(Note 1)			0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = –18 mA			–1.2	V
I_{IL}	Input LOW Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 0 V			–10	µA
		V_{CC} = 5.5 V, V_{IN} = 0.4 V			–5	µA
I_{IH}	Input HIGH Current (Select Inputs)	V_{CC} = 5.5 V, V_{IN} = 2.7 V			5	µA
		V_{CC} = 5.5 V, V_{IN} = 5.5 V			10	µA
I_{OZL}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 0.4 V			–15	µA
		V_{CC} = 5.5 V, V_{OUT} = 0 V			–20	µA
I_{OZH}	Off-State Leakage Current (I/O Ports)	V_{CC} = 5.5 V, V_{OUT} = 2.7 V			15	µA
		V_{CC} = 5.5 V, V_{OUT} = 5.5 V			20	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		–60		mA
I_{CCQ}	Quiescent Power Supply Current (Note 4)	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND Outputs Open	MIL		TBD	mA
			COM'L		TBD	mA
I_{CCT}	Power Supply Current TTL Input HIGH (Note 4)	V_{CC} = 5.5 V, V_{IN} = 3.4 V Other Inputs at V_{CC} or GND	MIL		TBD	mA/ Input
			COM'L		TBD	

DC CHARACTERISTICS (Cont'd.)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{CCD}†	Dynamic Power Supply Current (Note 4)	V_{CC} = 5.5 V, Outputs Open One Output Toggling (Note 3)		TBD	µA MHz/Bit
C_{PD}†	Power Dissipation Capacitance	V_{CC} = 5.5 V (Note 5)		TBD	pF/bit

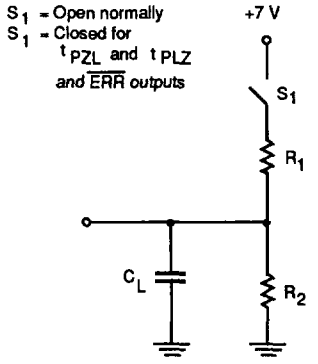
SWITCHING CHARACTERISTICS over operating range unless other specified (for APL products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	COM'L.		MIL.		Unit
				Min.	Max.	Min.	Max.	
1	t_{PLH}	Propagation Delay Port to Port	C_L = 50 pF R_1 = 500 Ohms R_2 = 500 Ohms	3	11	2	13	ns
2	t_{PHL}	LEO = HIGH		3	11	2	13	ns
3	t_{PLH}	Propagation Delay Select Input to Port		4	11	3	13	ns
4	t_{PHL}	LEO = HIGH		4	11	3	13	ns
5	t_{PLH}	Propagation Delay Port to Parity		4	14	3	16	ns
6	t_{PHL}	LEO = HIGH		4	14	3	16	ns
7	t_{PLH}	Propagation Delay		3	9	2	11	ns
8	t_{PHL}	LEO to Port		3	9	2	11	ns
9	t_{PZH}	Output Enable Time		3	8	2	10	ns
10	t_{PZL}	$\overline{OE}$ to Port		3	8	2	10	ns
11	t_{PHZ}	Output Disable Time		3	6	2	8	ns
12	t_{PLZ}	$\overline{OE}$ to Port		3	6	2	8	ns
13	t_{PLH}†	Propagation Delay		3	14	2	16	ns
14	t_{PHL}†	Port to $\overline{ERR}$		3	9	2	11	ns
15	t_{PLH}	Propagation Delay		5	15	4	17	ns
16	t_{PHL}	Select to Parity		5	15	4	17	ns
17	t_s	Port to LEO Setup		4.5		5.5		ns
18	t_h	Port to LEO Hold		0		1		ns
19	t_s	Select to LEO Setup		6.0		7.0		ns
20	t_h	Select to LEO Hold		0		1		ns
21	t_{PWH}†	LEO Pulse Width HIGH		3		4		ns

Notes:
1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time. Duration of short-circuit test not to exceed 100 ms.
3. Measured at a frequency of < 10 MHz with 50% duty cycle. Unused inputs are at V_{CC} or GND.
4. Calculation of total device I_{CC}: $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCO}(f_{CP}/2 + f_iN_i)$
   Where: D_H = Duty cycle for each TTL input HIGH
   N_T = Number of inputs at D_H
   f_{CP} = Clock frequency for clocked devices (Zero for non-clocked devices)
   f_i = Input frequency of the i^{th} input
   N_i = Number of inputs at f_i
5. C_{PD} in pF is calculated from I_{CCD} measurements using the formula
   $C_{PD} = I_{CCD}/V_{CC}$
   where I_{CCD} is expressed in µA/MHz/bit.

†Not included in Group A tests.

SWITCHING TEST CIRCUIT



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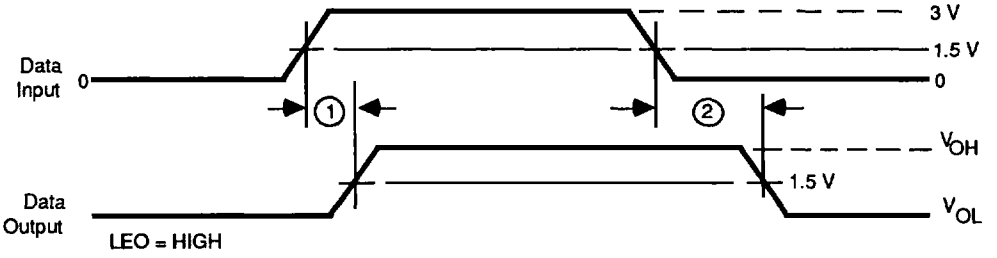
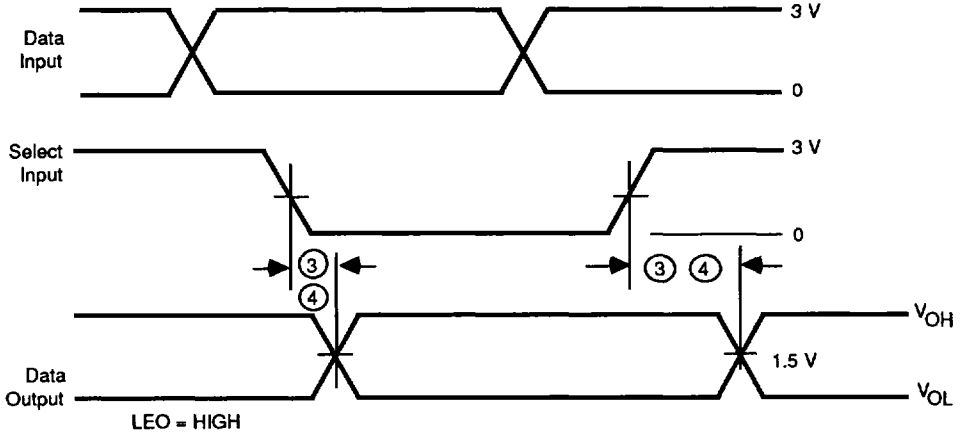
SWITCHING TEST WAVEFORMS



Propagation Delay—Port-to-Port

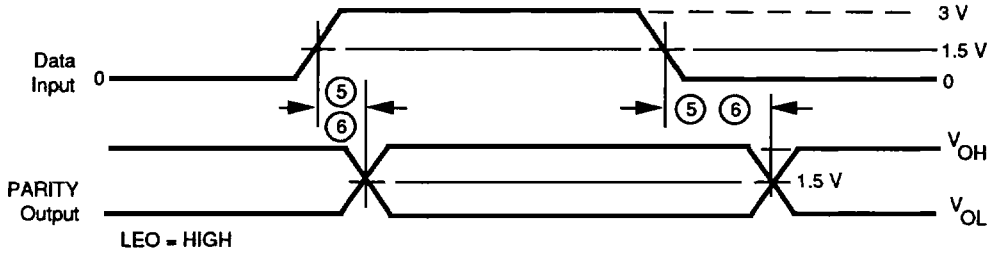
11996-007A



Propagation Delay—Select-to-Port

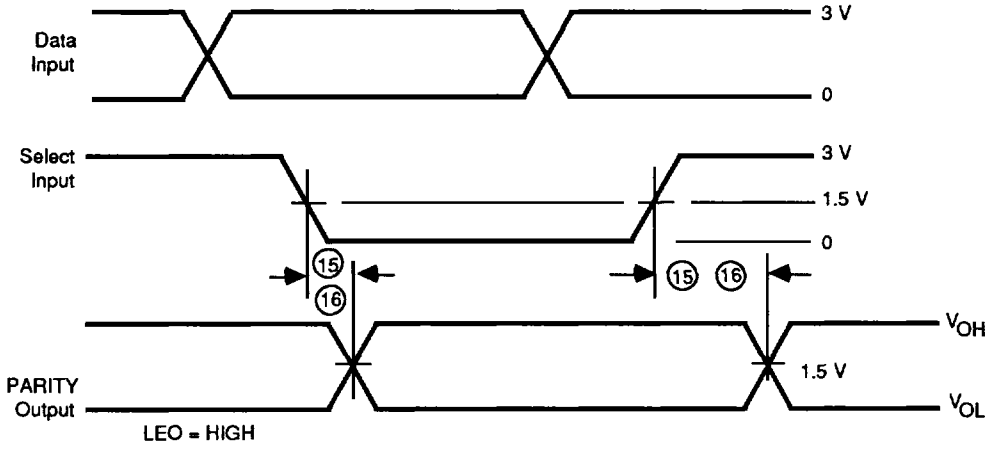
11996-008A

SWITCHING TEST WAVEFORMS (Cont'd.)



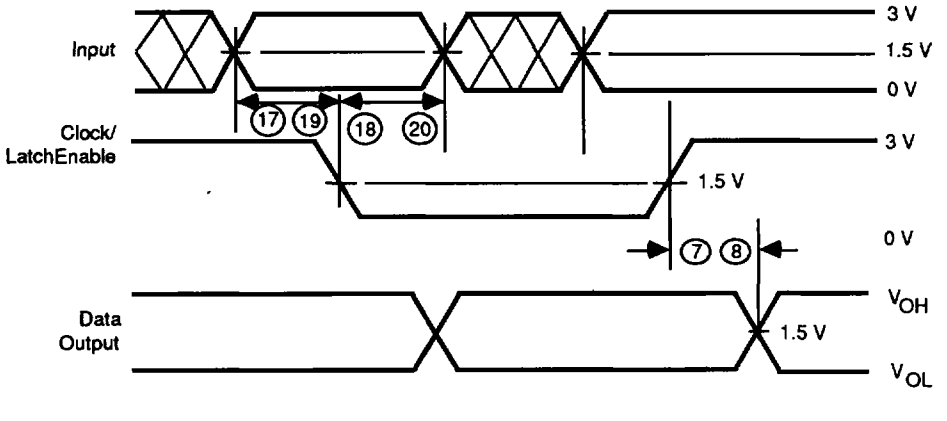
Propagation Delay — Port to Parity

11996-009A

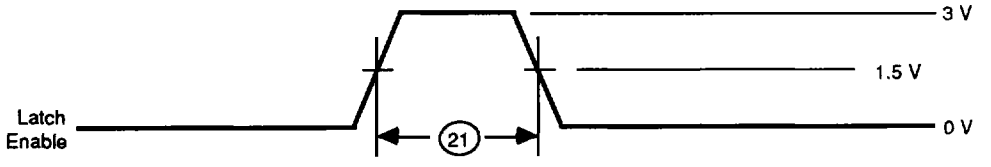


Propagation Delay — Select to Parity

11996-010A

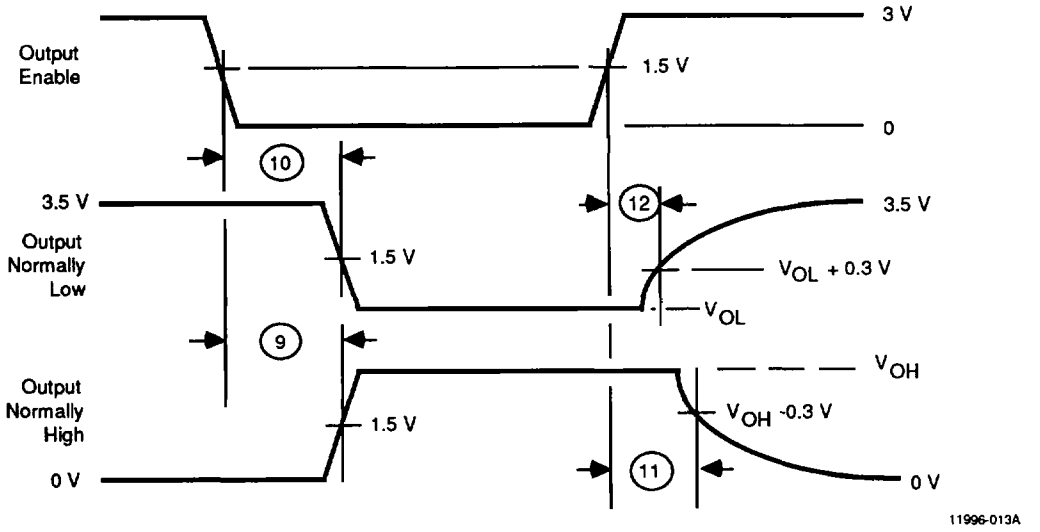


Output Latch Propagation Delay, Setup and Hold Times



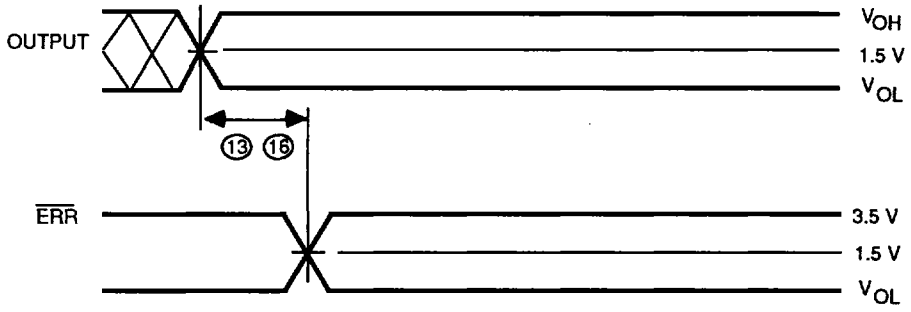
Minimum Latch Enable

11996-012A



Enable and Disable Times

SWITCHING TEST WAVEFORMS (Cont'd.)



11996-014A

Propagation Delay — Output Port to $\overline{ERR}$