

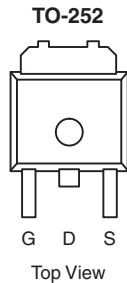


## P-Channel 40-V (D-S) 175 °C MOSFET

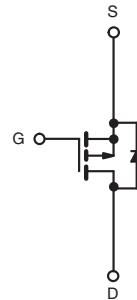
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
- 40	0.013 at $V_{GS} = - 10$ V	- 60 <sup>a</sup>
	0.022 at $V_{GS} = - 4.5$ V	- 48

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature



Drain Connected to Tab



Ordering Information: SUD50P04-13L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current <sup>b</sup>	$I_D$	$T_C = 25$ °C	- 60 <sup>c</sup>
		$T_C = 100$ °C	- 43
Pulsed Drain Current	$I_{DM}$	- 100	
Continuous Source Current (Diode Conduction)	$I_S$	- 60 <sup>c</sup>	
Avalanche Current	$I_{AS}$	L = 0.1 mH	- 40
Avalanche Energy,			$E_{AS}$
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25$ °C	93.7 <sup>b</sup>
		$T_A = 25$ °C	3 <sup>a</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	15	18
		Steady State	40	50
Maximum Junction-to-Case (Drain)	$R_{thJC}$	1.3	1.8	°C/W

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

b. Calculated based on maximum allowed Junction Temperature. Package limitation current is 50 A.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-40			V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.0		-3.0	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-50			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -30\text{ A}$		0.0105	0.013	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.020	
		$V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$		0.017	0.022	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -30\text{ A}$	15			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3120		pF
Output Capacitance	$C_{oss}$			440		
Reverse Transfer Capacitance	$C_{rss}$			320		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		4.3		$\Omega$
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -50\text{ A}$		63	95	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			13		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			16		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 0.4\text{ }\Omega$ $I_D \cong -50\text{ A}, V_{GEN} = -10\text{ V}, R_g = 2.5\text{ }\Omega$		15	25	ns
Rise Time <sup>c</sup>	$t_r$			18	30	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			60	90	
Fall Time <sup>c</sup>	$t_f$			47	70	
<b>Drain-Source Body Diode Characteristics</b>						
Pulse Current	$I_{SM}$				-100	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = -50\text{ A}, V_{GS} = 0\text{ V}$		-1.0	-1.5	V
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -50\text{ A}, di/dT = 100\text{ A}/\mu\text{s}$		36	55	ns

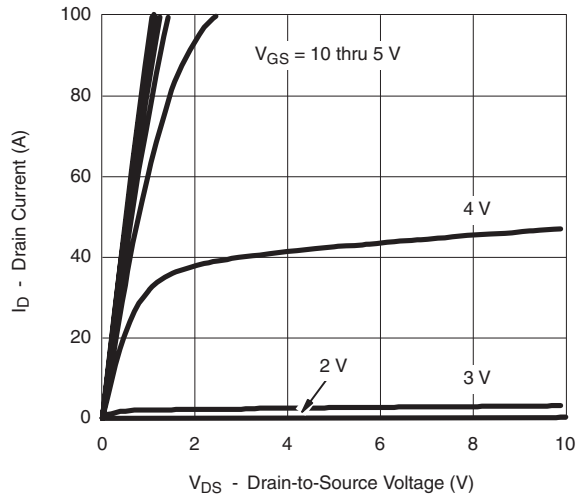
## Notes:

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

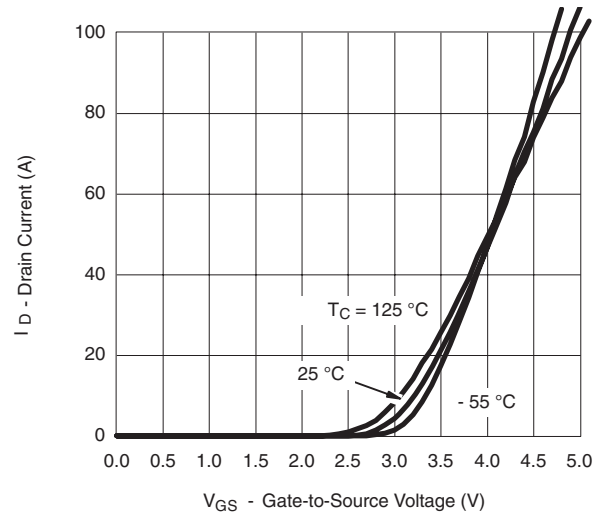
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



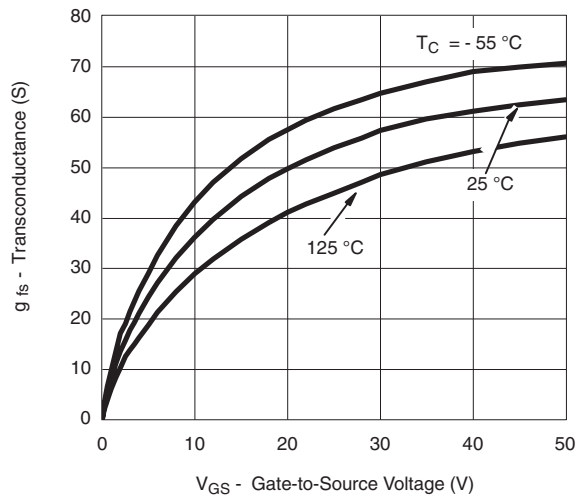
**TYPICAL CHARACTERISTICS** 25 °C unless noted



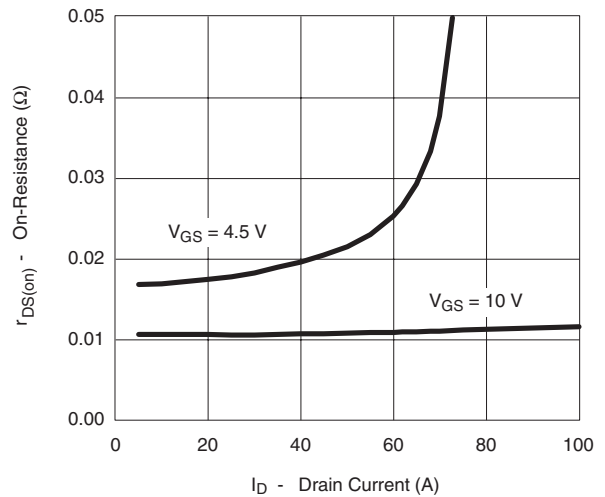
**Output Characteristics**



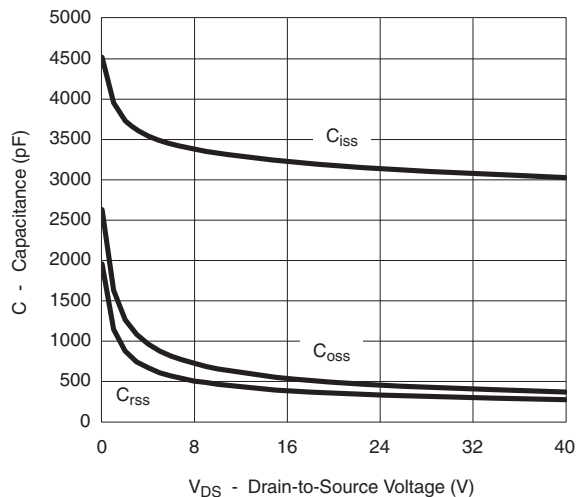
**Transfer Characteristics**



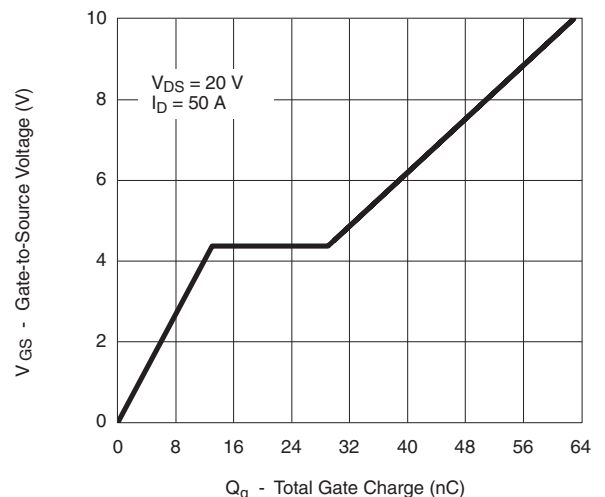
**Transconductance**



**On-Resistance vs. Drain Current**



**Capacitance**



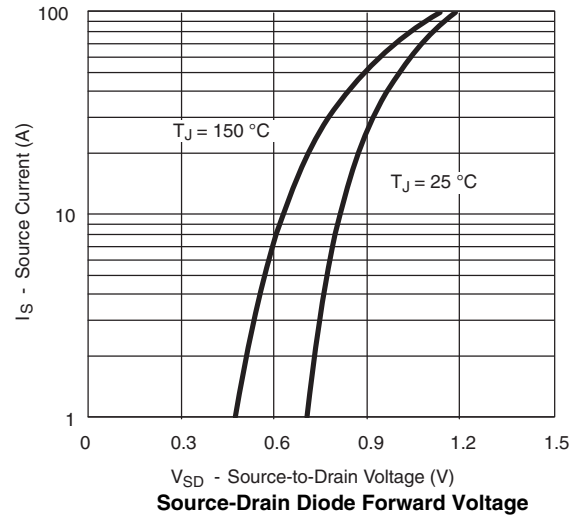
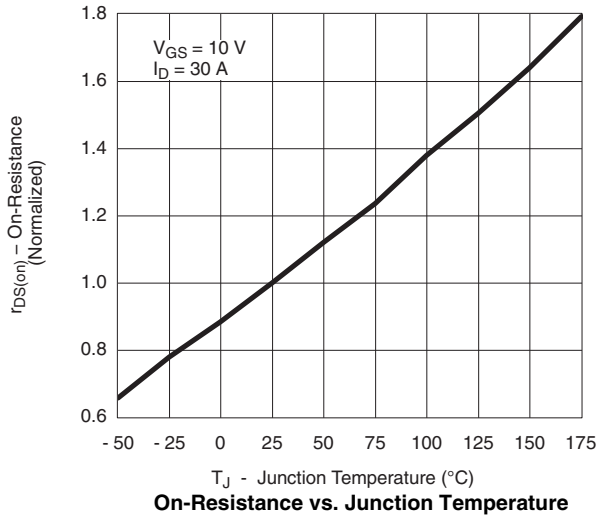
**Gate Charge**

# SUD50P04-13L

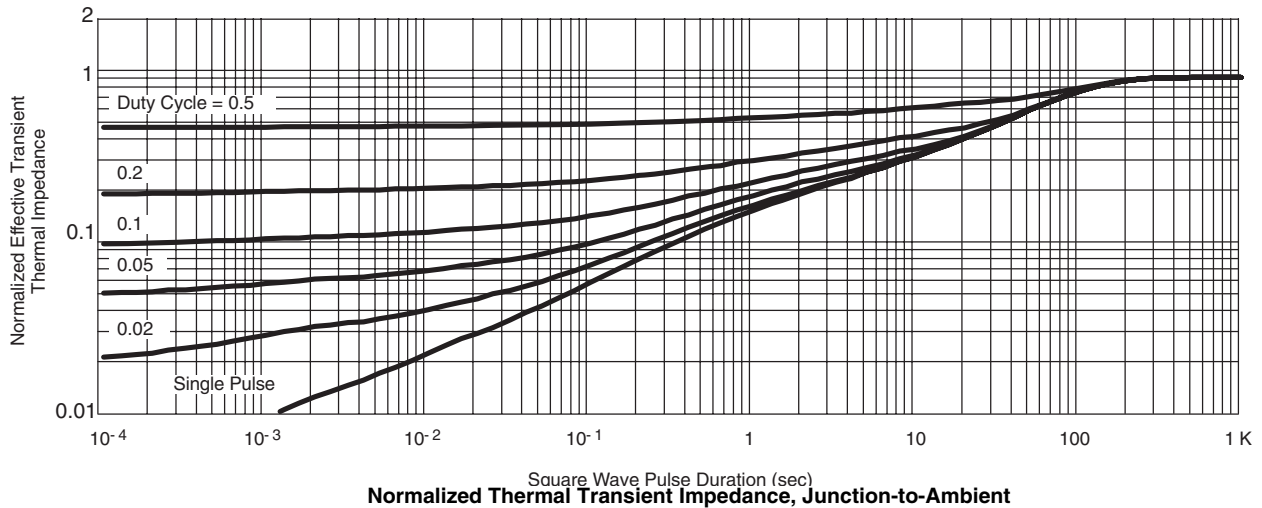
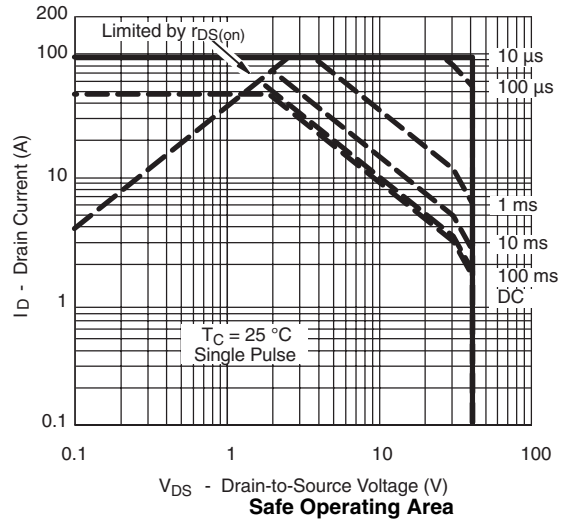
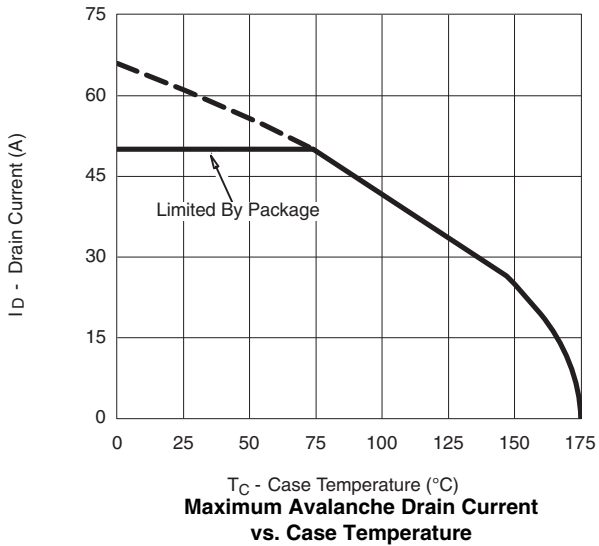


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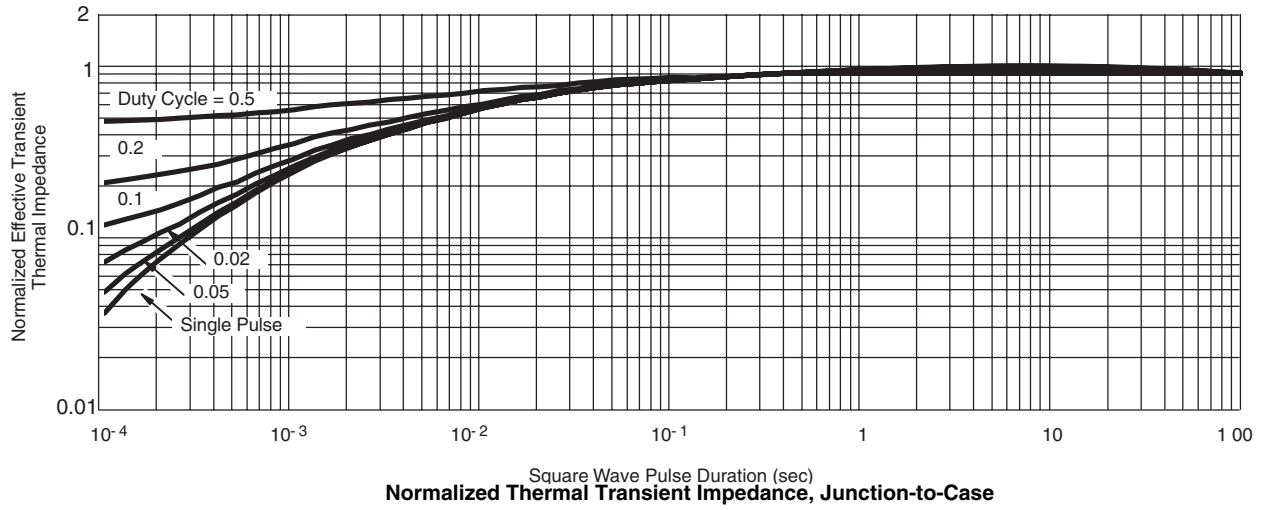
## TYPICAL CHARACTERISTICS 25 °C unless noted



## THERMAL RATINGS



**THERMAL RATINGS**



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73009>



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