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NCP5612

High Efficiency Ultra Small Thinnest White LED Driver

The NCP5612 product is a dual output LED driver dedicated to the LCD display backlighting.

The built−in DC/DC converter is based on a high efficient charge pump structure with operating mode 1x and 1.5x. It provides a peak 87% efficiency together with a 0.2% LED to LED matching.

Features

- Support the Single Wire Serial Link Protocol
- Peak Efficiency 90% with 1x and 1.5x Mode
- Programmable Dimming ICON Function
- Built−in Short Circuit Protection
- Provides 16 steps Current Control
- Controlled Start−up Inrush Current
- Built−in Automatic Open Load Protection
- Tight 0.2% Matching Tolerance
- Accurate 1% Output Current Tolerance
- Smallest Available Package on the Market
- This is a Pb−Free Device

Typical Applications

- Portable Back Light
- Digital Cellular Phone Camera Photo Flash
- LCD and Key Board Simultaneous Drive

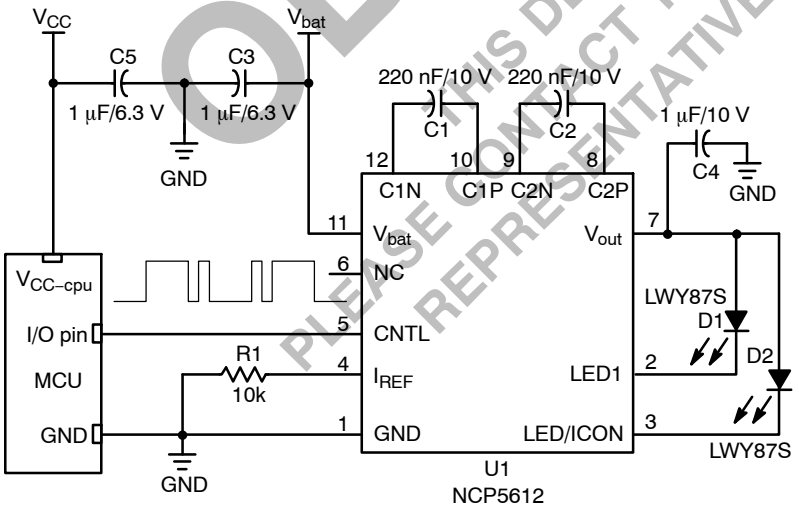

Figure 1. Typical Single Wire White LED Driver

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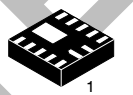
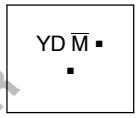
MARKING DIAGRAM

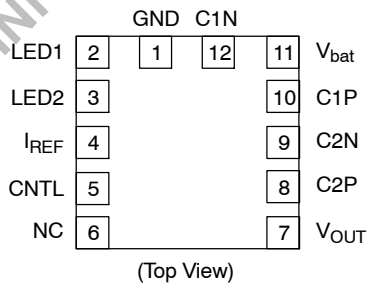


LLGA12 (2x2 mm)
MU SUFFIX
CASE 513AA



YD = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP5612MUTBG	LLGA12 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

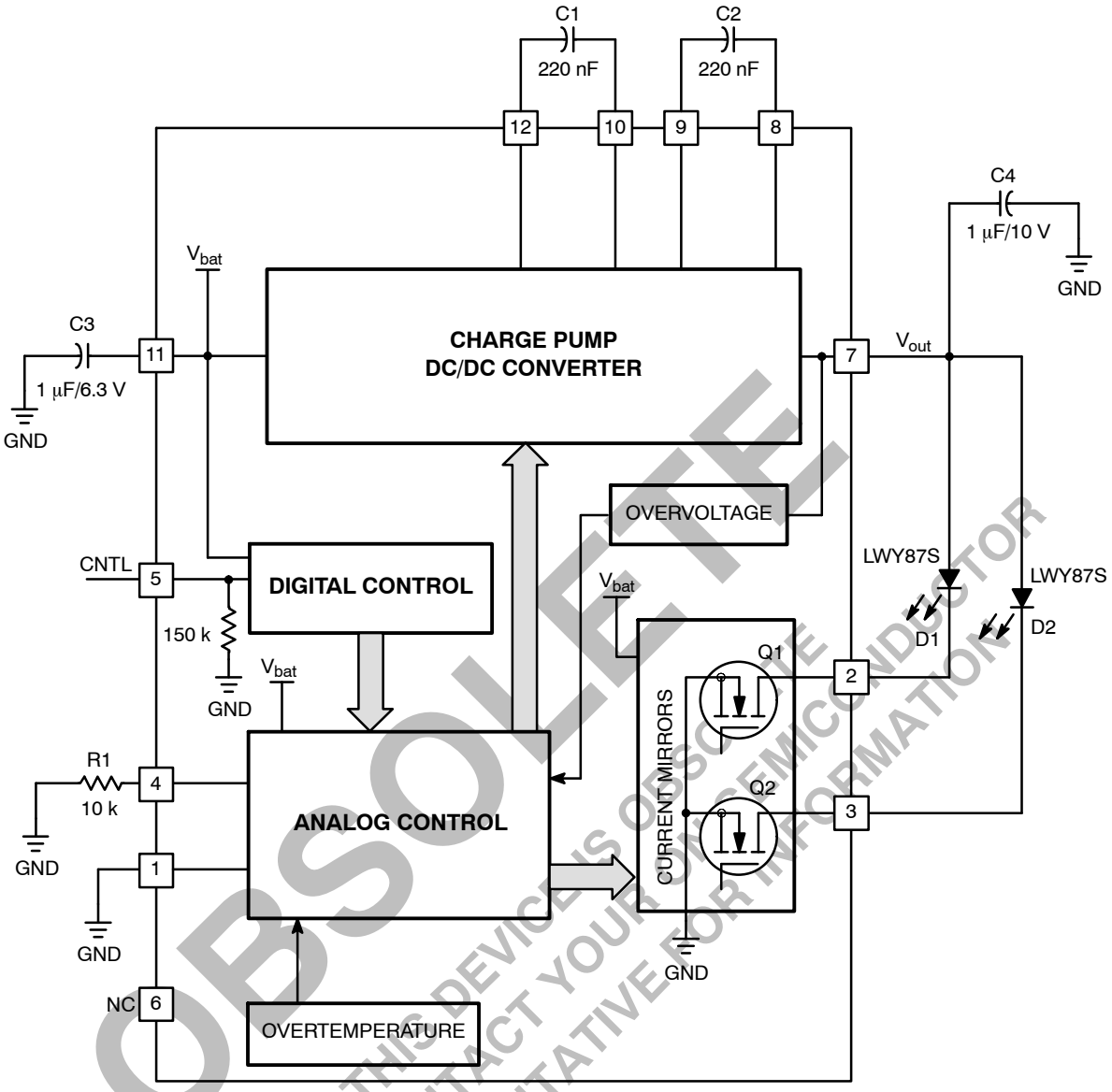


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1	GND	POWER	This pin is the GROUND signal for the power analog blocks and must be connected to the system ground. This pin is the GROUND reference for the DC/DC converter and the output current control. The pin must be connected to the system ground, a ground plane being strongly recommended.
2	LED1	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the first LED, intended to be used in backlight application. The current is limited to 30 mA maximum (Note 2). The LED1 is deactivated when the ICON bit of the LED−REG register is High. The LED1 is automatically disconnected when an open load is sensed pin 2 during the operation.
3	LED2	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the second LED, intended to be used in backlight application. The current is limited to 30 mA maximum (Note 2). The LED2 fulfills the ICON function, LED1 being deactivated, when the ICON bit of the LED−REG register is High. The LED2 is automatically disconnected when an open load is sensed pin 3 during the operation.
4	I_{REF}	INPUT, ANALOG	This pin provides the reference current, based on the internal band−gap voltage reference, to control the output current flowing in the LED. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the LED biases. An external current source can be used to bias this pin to dim the light coming out of the LED. In no case shall the voltage at pin 4 be forced either higher or lower than the 600 mV provided by the internal reference.
5	CNTL	INPUT, DIGITAL	This pin supports the flow of data between the external MCU and the NCP5612 internal registers. The protocol makes profit of a Single Wire structure associated to a Serial 8 bits format data flow.
6	NC	–	No internal connection
7	V_{OUT}	OUTPUT, POWER	This pin provides the output voltage supplied by the DC/DC converter. The V_{out} pin must be decoupled to ground by a 1 μF ceramic capacitor located as close as possible to the pin. Cares must be observed to minimize the parasitic inductance at this pin. The circuit shall not operate without such bypass capacitor connected across the V_{out} pin and ground. The output voltage is internally clamped to 5.5 V maximum in the event of no load situation. On the other hand, the output current is limited to 40 mA (typical) in the event of a short circuit to ground.
8	C2P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2N (Note 1)
9	C2N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2P (Note 1)
10	C1P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1N (Note 1)
11	V_{BAT}	INPUT, POWER	Input Battery voltage to supply the analog and digital blocks. The pin must be decoupled to ground by a 1.0 μF minimum ceramic capacitor.
12	C1N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1P (Note 1)

1. Using low ESR ceramic capacitor, 50 mΩ maximum, is mandatory to optimize the Charge Pump efficiency.
2. Total DC/DC output current is limited to 60 mA.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{BAT}	7.0	V
Output Power Supply	Vout	7.0	V
Digital Input Voltage Digital Input Current	CNTL	−0.3 < V < V_{BAT} 1.0	V mA
Human Body Model: R = 1500 Ω, C = 100 pF (Note 3) Machine Model	ESD	2.0 200	kV V
LLGA12 Package Power Dissipation @ T_A = +85°C (Note 4) Thermal Resistance, Junction−to−Case Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JC}$ $R_{\theta JA}$	 200 51 200	 mW °C/W °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Latch−up Current Maximum Rating per JEDEC Standard: JESD78	−	±100	mA
Moisture Sensitivity (Note 5)	−	1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
4. The maximum package power dissipation limit must not be exceeded.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
Power Supply	11	V_{bat}	2.7	−	5.5	V
Continuous DC Current in the Load @ V_f = 3.8 V, 3.2 V < V_{bat} < 5.5 V, ICON = L (30 mA per LED)	7	I_{out}	60	−	−	mA
Output ICON Current (ICON bit = H) @ 3.2 V < V_{bat} < 4.2 V, T_A = +25°C	7	$I_{ICONTOL}$	−	450	550	μA
Continuous Output Short Circuit Current	7	I_{sch}	−	40	100	mA
Output Voltage Compliance (OVP)	7	V_{out}	4.8	−	5.7	V
DC/DC Start Time (C_{out} = 1.0 μF) from end of the CNTL T_{dst} delay to full load operation, @ V_{bat} = 3.6 V	12	T_{start}	−	150	−	μs
Output Voltage Turn−off (C_{out} = 1 μF) From Last Low Level at CNTL pin to V_{out} = 5%	12	T_{off}	−	500	−	μs
Standby Current, 0°C < T_A < +85°C V_{bat} = 3.6 V, I_{out} = 0 mA, ICON = L	11	I_{stdb}	−	−	1.0	μA
Operating Current, @ I_{out} = 0 mA, ICON = H, V_{bat} = 3.6 V	11	I_{op}	−	600	−	μA
Output LED to LED Current Matching, V_{bat} = 3.6 V, I_{LED} = 10 mA, LED1 & LED2 are Identical −25°C < T_A < 85°C	2, 3	I_{MAT}	−	±0.2	±1.0	%
Output Current Tolerance @ V_{bat} = 3.6 V, I_{LED} = 10 mA −25°C < Ta < 85°C	2, 3	I_{TOL}	−	±1.0	−	%
Charge Pump Operating Frequency	−	F_{pwr}	−	1.0	−	MHz
Thermal Shutdown Protection	−	T_{SD}	−	160	−	°C
Thermal Shutdown Protection Hysteresis	−	T_{SDH}	−	30	−	°C
Efficiency − LED1 = LED2 = 10 mA, V_f = 3.2 V, V_{bat} = 3.8 V (Total = 20 mA) − LED1 = LED2 = 30 mA, V_f = 3.75 V, V_{bat} = 3.8 V (Total = 60 mA)	− −	E_{PWR}	− −	87 84	− −	%

ANALOG SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
Reference Current @ V_{ref} = 600 mV (Note 7)	4	I_{REF}	1.0	–	60	μA
Reference Voltage (Note 7) 0°C < T_A < +85°C	4	V_{REF}	−3%	600	+3%	mV
Base Reference Current (I_{REF}) Current Ratio	–	I_{LEDR}	–	500	–	–

6. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.
7. The external circuit must not force the I_{REF} pin voltage either higher or lower than the 600 mV specified.

DIGITAL PARAMETERS SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, operating conditions 2.85 V < V_{bat} < 5.5 V, unless otherwise noted.) Note: Digital inputs undershoot < – 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{BAT}.

Rating	Pin	Symbol	Min	Typ	Max	Unit
Positive going Input High Voltage Threshold, CNTL signals	5	V_{IH}	1.4	–	V_{BAT}	V
Negative going Input Low Voltage Threshold, CNTL signals	5	V_{IL}	–	–	0.6	V
Pull Down Resistor	5	R_{cntl}	–	150	–	kΩ
Delay between two consecutive frame (Note 9)	5	t_{idle}	10	–	–	μs
Wake up delay (Note 9)	5	t_{wkp}	–	–	1.0	μs
CNTL signal rise and fall time (Note 9)	5	t_r, t_f	–	–	200	ns
Clocked CNTL High (Note 9)	5	t_{on}	–	–	75	μs
CNTL Low (Note 9)	5	t_{on}, t_{off}	1.0	–	–	μs
CNTL Store data delay (Note 9)	5	T_{dst}	–	200	300	μs
Input CNTL frequency (Note 9)	5	F_{CNTL}	–	–	400	kHz

8. see Timings Reference
9. Parameter not tested in production, guaranteed by design.

APPLICATION INFORMATION

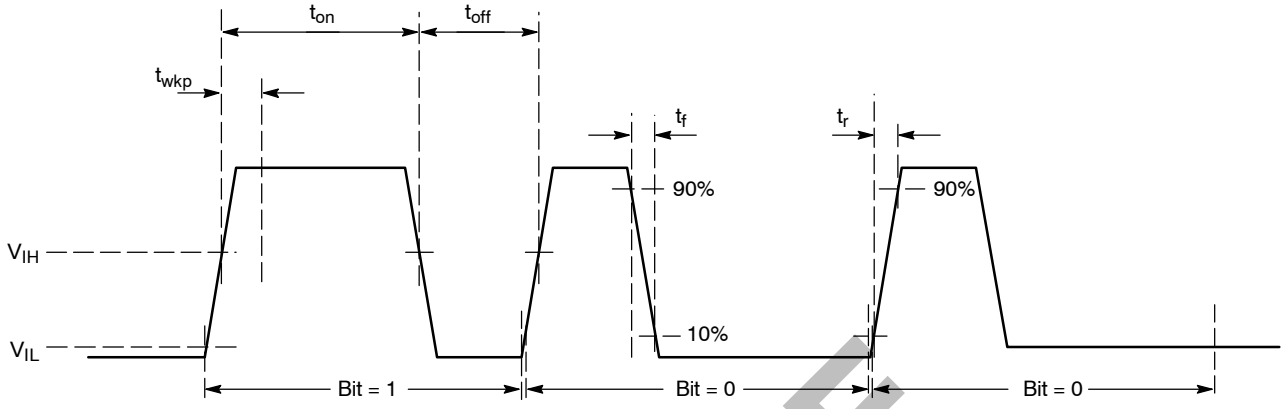


Figure 3. Timings Reference

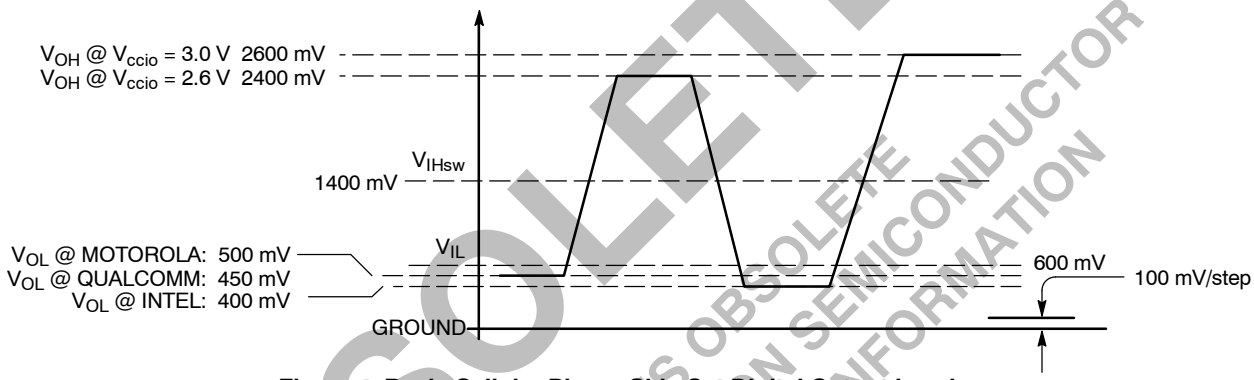


Figure 4. Basic Cellular Phone Chip Set Digital Output Levels

DC/DC Operation

The converter is based on a charge pump technique to generate a DC voltage capable to supply the White LED load. The system regulates the current flowing into each LED by means of internal current mirrors associated with the white diodes. Consequently, the output voltage will be equal to the V_f of the LED, plus the drop voltage (ranging from 150 mV to 400 mV, depending upon the output current and V_{bat} / V_f ratio) developed across the internal NMOS mirror. Typically, assuming a standard white LED forward biased at 10 mA, the output voltage will be 3.6 V.

The built−in OVP circuit continuously monitors the output voltage and stops the converter when the voltage is above 5.0 V typical. The converter resumes to normal operation when the voltage drops below the typical 5.0 V (no latch−up mechanism). Consequently, the chip can operate with no load during any test procedures.

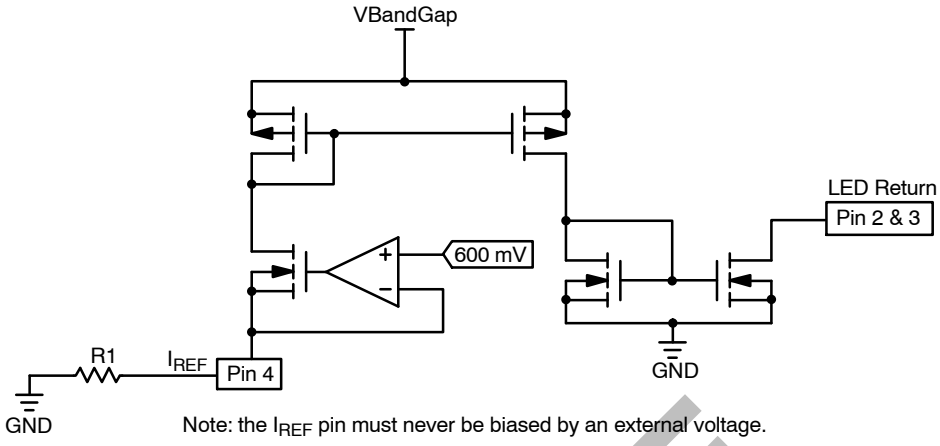
Load Current Calculation

The load current is derived from the 600 mV reference voltage provided by the internal Band Gap associated to the external resistor connected across I_{REF} pin and Ground (see Figure 5). In any case, no voltage shall be forced at I_{REF} pin, either downward or upward.

The reference current is multiplied by the internal current mirror, associated to the number of pulses as depicted Figure 9, to yield the output load current. Since the reference voltage is based on a temperature compensated Band Gap, a tight tolerance resistor will provide a very accurate load current. The resistor is calculated from the Ohm's law (R_{bias} = V_{ref}/I_{REF}) and define the maximum current flowing into the LED when 20 pulses have been counted at the CNTL pin.

Since the reference current must be between the minimum and maximum specified, the resistor value will range between R_{bias} = 300/30 mA = 10 kΩ and R_{bias} = 300/0.5 mA = 600 kΩ. Obviously, the tolerance of such a resistor must be 1% or better, with a 100 ppm thermal coefficient, to get the expected overall tolerance.

Typical applications will run with R_{bias} = 10 kΩ to make profit of the full dynamic range provided by the S−Wire DATA byte.



Note: the I_{REF} pin must never be biased by an external voltage.

Figure 5. Basic Reference Current Source

Load Connection

The NCP5612 is capable to drive the two LED simultaneously, as depicted (see Figure 1), but the load can be arranged to accommodate one or two LED if necessary in the application (see Figure 6). In this case, the two current mirrors can be connected in parallel to drive a single powerful LED, thus yielding 60 mA current capability in a single LED.

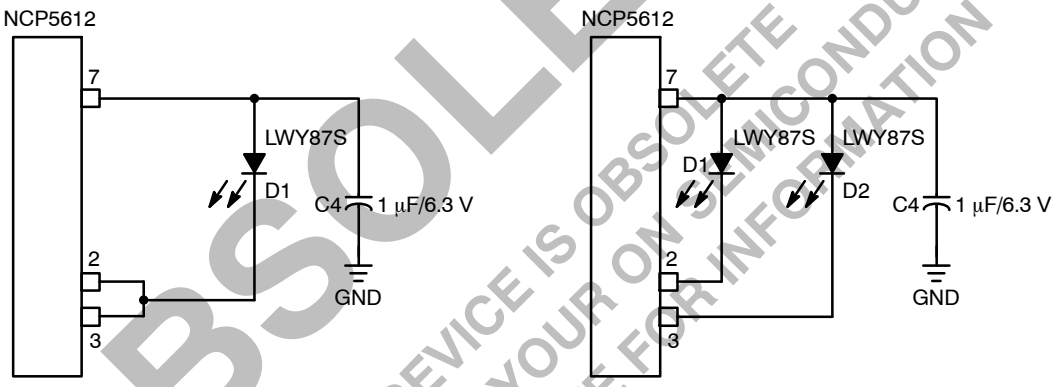


Figure 6. Typical Single and Double LED Connections

Finally, an external network can be connected across V_{out} and ground, but the current through such network will not be regulated by the NCP5612 chip (see Figure 7). On top of that, the total current out of the V_{out} pin shall be limited to 60 mA.

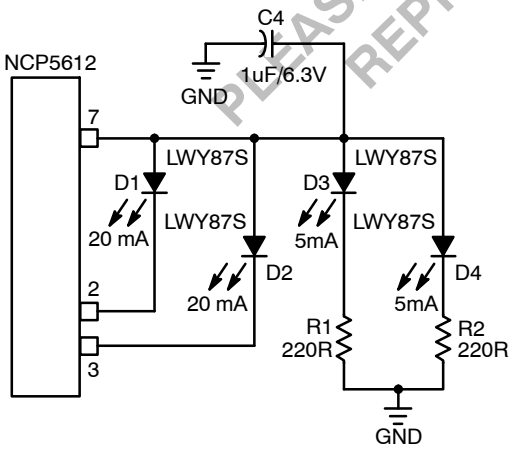


Figure 7. Extra Load Connected to V_{out}

Single Wire Serial Link Protocol

The proposed S−WIRE uses a pulse count technique already existing in the data exchange systems. The protocol supports broken transmission, assuming the hold time is shorter than the maximum 200 µs typical specified in the data sheet. The S−WIRE details are provided in the AND8264 application note.

Based on the two examples provided in Figure 8, the CNTL pin supports two digital level:

CNTL = Low → the system is shut−off and no current flow in either LED1 or LED2.

CNTL = High → the system is active and the two LED are powered according to the selected sequence.

There is no time delay associated with the Low state and the LED are switched Off when the CNTL signal drops to Low. To program a new LED configuration, one shall send the number of pulses on the CNTL pin according to the true table:

- The internal counter is reset to zero on the first negative going transient present on the CNTL pin

- The first four positive going pulses are used to control the ICON (LED2):
  1. Pulse #1 → ICON = 100 μA
  2. Pulse #2 → ICON = 150 μA
  3. Pulse #3 → ICON = 250 μA
  4. Pulse #4 → ICON = 450 μA
- The fifth positive pulse will clear the ICON and activate the normal operation of LED1 and LED2
- The pulses from the fifth to the twentieth will increase the LED current according to a pseudo logarithmic scale (see Figure 9).
- Any pulses beyond the twentieth will not make change to the LED current if the delay between the pulses is shorter than 75 μs.
- The system returns to zero if a pulse, delayed by 200 μs – T_{dst} – , follows the twentieth one and the cycle restart from the beginning.

Once the expected LED current value is reached, the CNTL pin must stay High to store the new data and maintain the LED active.

The contain of the counter is stored into the internal LED registers at the end of the built−in 200 μs typical delay: no action will take place during the end of the last positive going pulse and the end of the T_{dst} delay. Such a protocol prevent the system for broken transmission.

On the other hand, in order to avoid corrupted data transmission, the High level shall be 75 μs maximum during a given data frame. Consequently, the pulse frequency is bounded by a 13 kHz minimum and a 400 kHz maximum.

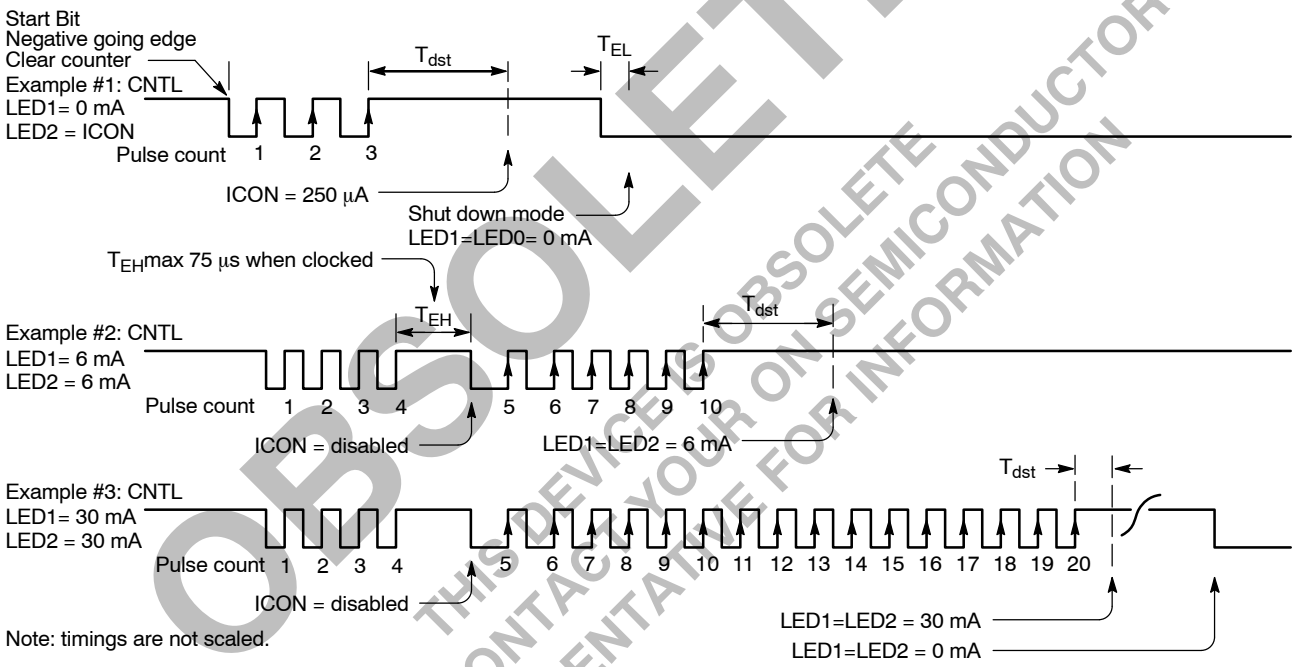


Figure 8. Basic NCP5612 Programming Sequence

DIMMING

The built−in Single Wire Serial Link interface provides a simple way to accurately control the output current flowing in the two LED. Provision have been made, at silicon level, to provide a full dimming of the backlight (NORMAL mode of operation), the ICON current being adjustable in four steps when it is activated.

Table 1. LED Dimming Configuration

Pulse Count	LED activity
Pulse 1	LED#2 = 100 μA, LED#1 de−activated
Pulse 2	LED#2 = 150 μA, LED#1 de−activated
Pulse 3	LED#2 = 250 μA, LED#1 de−activated
Pulse 4	LED#2 = 450 μA, LED#1 de−activated
Pulse 5 to Pulse 20	ICON de−activated, NORMAL back-light takes place

The DC/DC converter is switched OFF and the two LED are disconnected when LED−REG=$00.

When the ICON mode is activated, the DC/DC converter is switched OFF, LED#1 is deactivated from the LED current sense and the programmed bias current (powered from the V_{bat} source) is forced into LED#2.

Bit Clock	I−LED(mA)	Bit Clock	I−LED(mA)
1	1	9	12
2	2	10	14
3	3	11	16
4	4	12	19
5	5	13	22
6	6	14	25
7	8	15	28
8	10	16	31

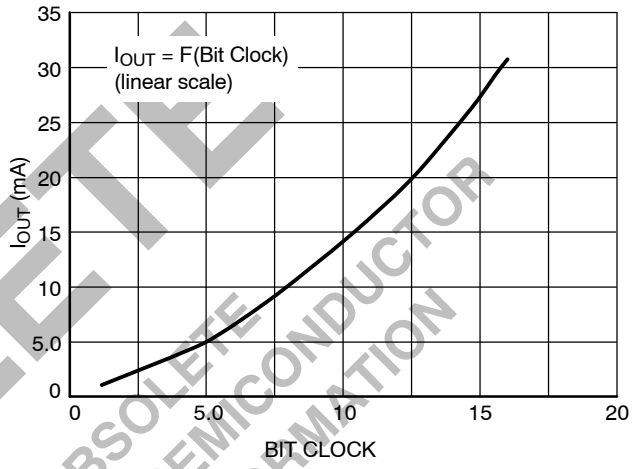


Figure 9. Typical Output Current Slope

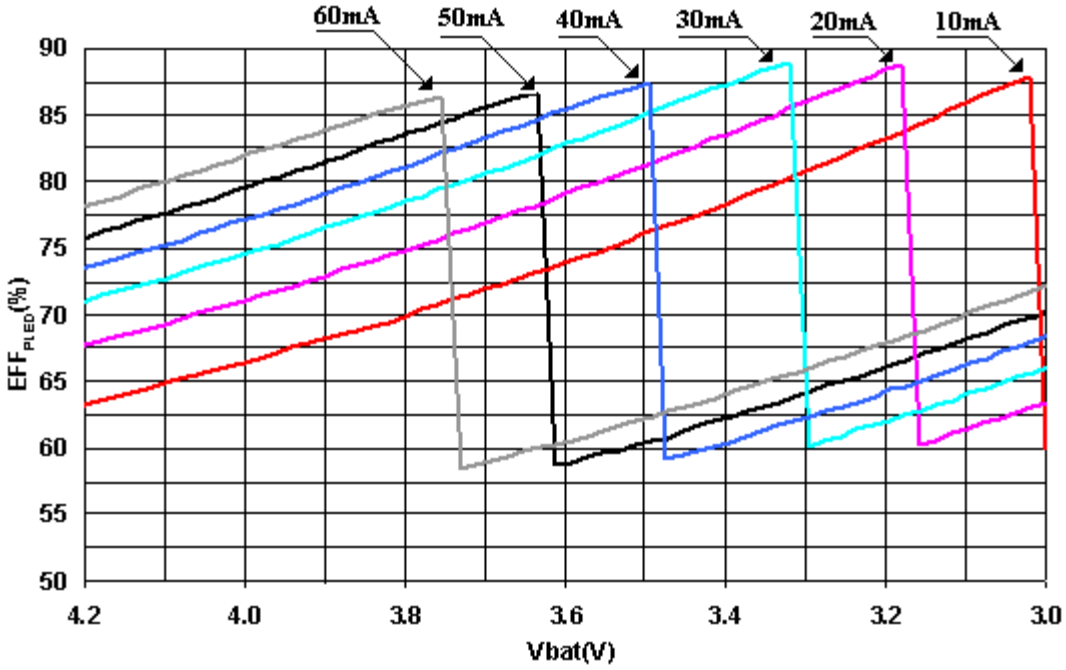


Figure 10. Typical Efficiency

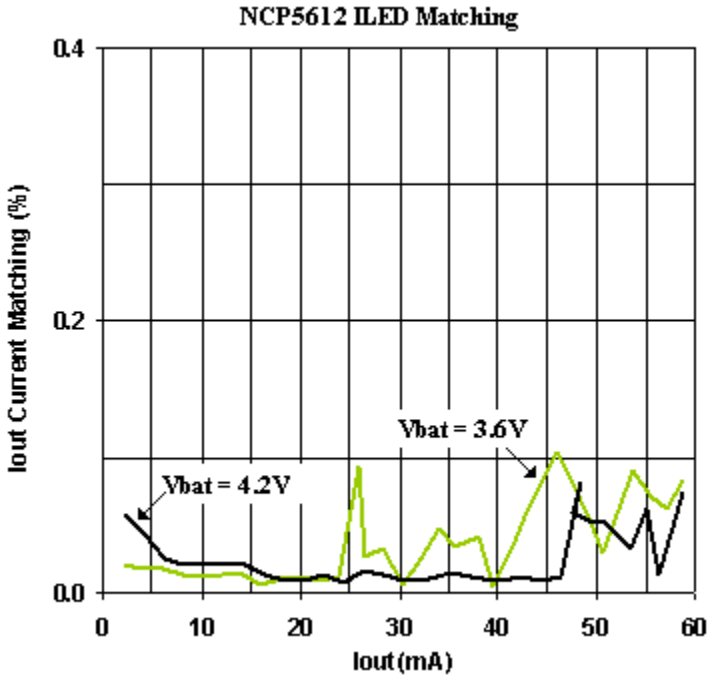


Figure 11. Typical LED to LED Current Matching

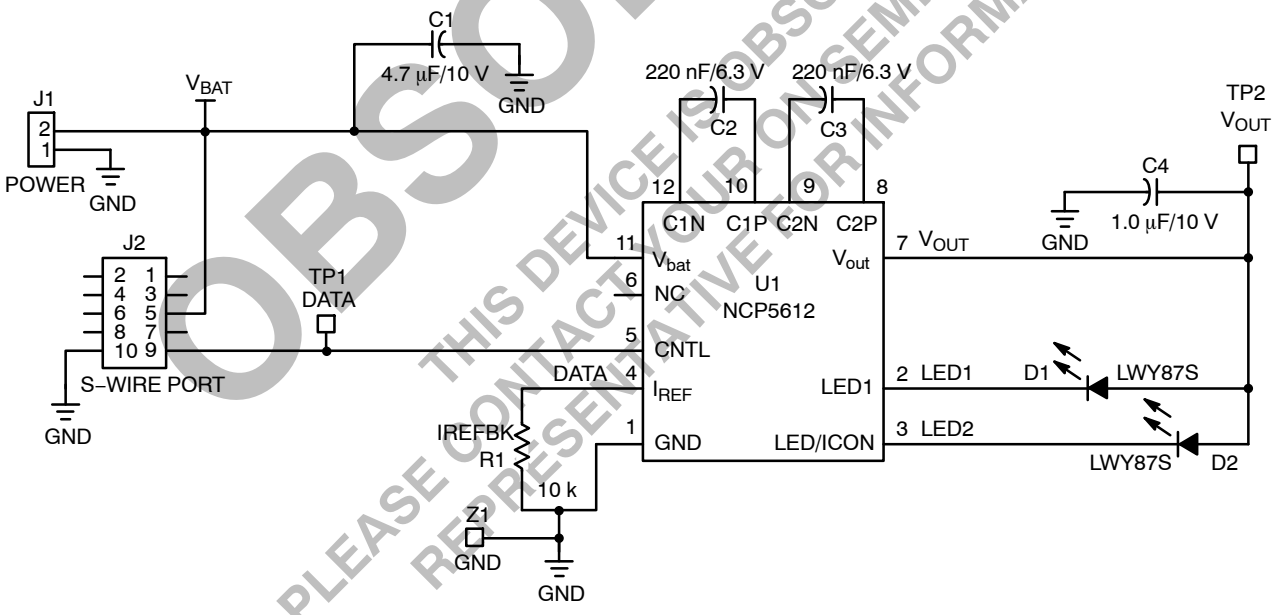
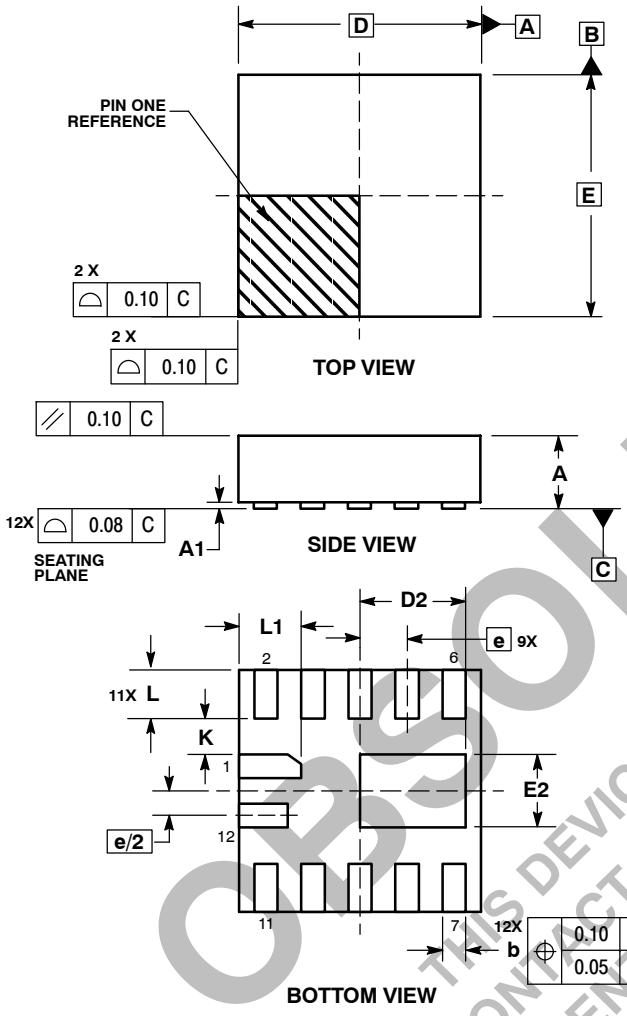


Figure 12. Demo Board Schematic Diagram

PACKAGE DIMENSIONS

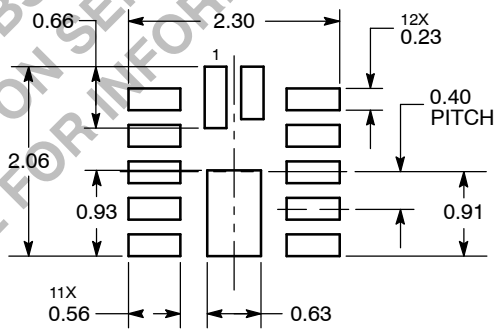
LLGA12
MU SUFFIX
CASE 513AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.15	0.25
D	2.00 BSC	
D2	0.80	1.00
E	2.00 BSC	
E2	0.55	0.65
e	0.40 BSC	
K	0.25	−−−
L	0.30	0.50
L1	0.40	0.60

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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