PNX9530; PNX9531; PNX9535

Software enabled video and multimedia entertainment platform

Rev. 01.11C — 1 October 2009 Preliminary data sheet

1. General description

The PNX9530; PNX9531; PNX9535 is a software enabled video and multimedia entertainment platform that provides video playback from a wide range of video sources and different video formats. The PNX9530; PNX9531; PNX9535 has an outstanding array of proprietary video post processing algorithms.

The PNX9530; PNX9531; PNX9535 is a true multimedia platform enabling Graphical User Interface (GUI), connectivity and advanced audio processing, qualified for automotive applications.

2. Features

2.1 Software enabled video and multimedia entertainment platform

- Fixed basic hardware platform
  - Digital video input and output
  - Digital audio output
  - DDR2 SDRAM interface (JEDEC compliant)
  - USB 2.0
  - I^2C-bus
- Built-in flexibility for multimedia processing through programmable GPIO interfaces
  - Digital video input and output
  - Digital audio input and output
- Built-in flexibility for connectivity through programmable GPIO interfaces
  - EXtended I/O functions (XIO) for Hard Disc Drives (HDD), CD or DVD
  - Host interface
  - PCI 2.2
  - USB High-Speed On-The-Go (OTG)
  - Clocks and generic signals

founded by Philips

2.2 Dual video MPEG decoding and rendering

- Decodes two video streams in parallel
- Renders each video stream on different video screens
- Independent control of each video stream
- Independent On-Screen Display (OSD) for each video stream

2.3 Video quality

- Outstanding array of proprietary video post-processing algorithms (available on dedicated request and commercial agreement; please contact NXP; see Section 22) for:
  - Color correction
  - Image noise reduction
  - Sharpness enhancement
  - Natural motion
  - Error concealment
  - MPEG artifact reduction
  - Film detection
  - Deinterlacing and edge dependent deinterlacing
  - Panorama scaling
  - Contrast enhancement
  - Blue stretch, green enhancement and skin tone control
  - Adaptive backlight dimming
  - Auto picture control
  - Video format scaling

2.4 Memory

- External DDR2 SDRAM memory configuration options

  Remark: The DDR interface is capable to operate DDR1 memories also, but this function will not be guaranteed.
  - 32-bit data width
  - 16-bit data width
  - Footprint up to 1 Gb
  - Data rate up to 533 MHz
  - Recommended device MT47H16M16BG-37E
- EEPROM for external booting
- FLASH memory through XIO interface

2.5 Miscellaneous

- Only one external quartz crystal required
- Several power modes
- 5 V tolerant interface pins for GPIO, PCI, XIO, I^2C-bus, USB and host interface
- Qualified automotive grade 3 according to *AEC-Q100*

3. Applications

3.1 Benefits from using PNX9530; PNX9531; PNX9535

- Experience:
  - Enables the consumer to enjoy music and movies that they bring into their car on portable media and personal devices
  - Displays of up to two video sources in-car (dual video)
  - High-quality processing of video from a range of sources and in different formats
  - Turns even problematic video sources into high-quality video experience
- Product design:
  - Software enabled processor flexible enough to address a wide variety of use case combinations, including dual video decoding
  - Design various differentiating in-car multimedia products with the same entertainment platform
  - Use available ecosystem of independent software partners to enable fast time-to-market of new features
  - Synergistic integration with other in-car digital systems
  - Significantly reduces system Bill Of Materials (BOM)

3.2 Typical applications with PNX9530; PNX9531; PNX9535

- Front Seat Entertainment (FSE) system
- Rear Seat Entertainment (RSE) system
- DVD or CD playback device, including SoftWare (SW) navigator
- USB, SD card or HDD audio/video playback device
- JPEG viewer for digital camera images
- Dual video decoding and rendering device
- In-car video source decoding
- Video broadcast source decoding
- WiFi audio/video streaming (DLNA compliant)
- Bluetooth audio streaming to headphones
- Extensive library of picture improvement algorithms

4. Ordering information

Table 1. Ordering information

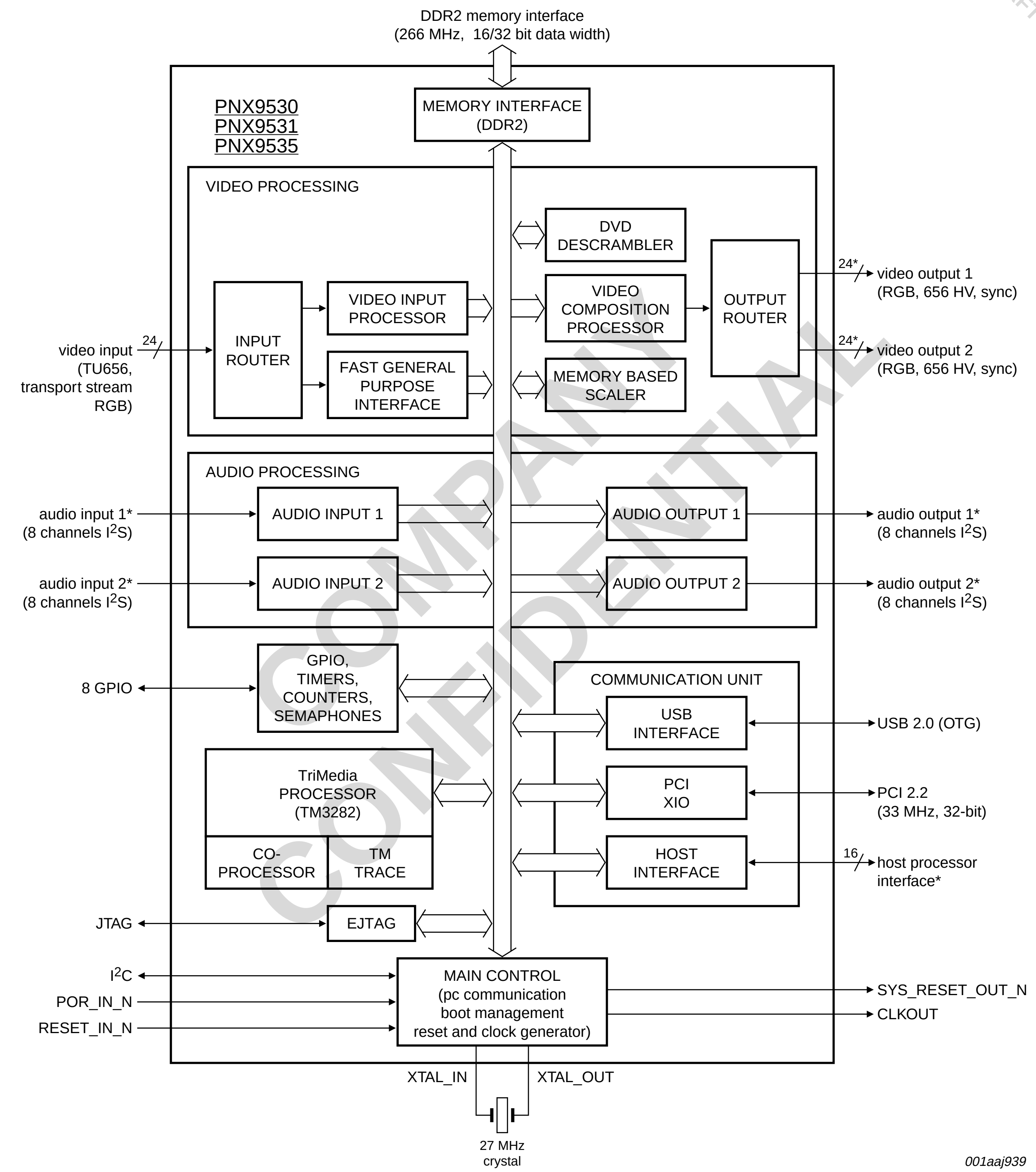
Type number	Package		
	Name	Description	Version
PNX9530E	BGA456	plastic ball grid array package; 456 balls; body 27 × 27 × 1.75 mm	SOT795-1
PNX9531E	BGA456	plastic ball grid array package; 456 balls; body 27 × 27 × 1.75 mm	SOT795-1
PNX9535E	BGA456	plastic ball grid array package; 456 balls; body 27 × 27 × 1.75 mm	SOT795-1

4.1 Ordering options

Table 2. Main type differences

Parameter	PNX9530	PNX9531	PNX9535	Unit
Maximum internal TM clock frequency	351	450	243	MHz
Width of DDR2 interface	32	32	16	bit
Video input channels	up to 3	up to 3	1	-

5. Block diagram



Showing the maximum configuration of the multifunctional GPIO interface. Not all choices may be possible at the same time (see Section 8.1).

Fig 1. Block diagram of PNX9530; PNX9531; PNX9535

6. Pinning information

6.1 Pinning

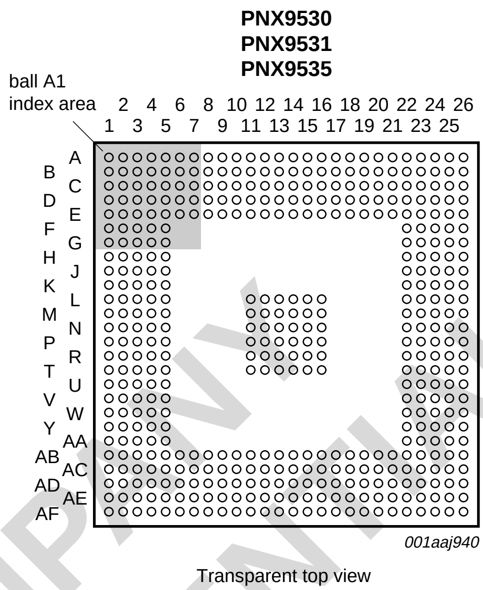


Fig 2. Pin configuration for BGA456

Table 3. Pin allocation table[1][2][3]

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
A1	VDI_D2	A2	MM_D0	A3	MM_D3	A4	MM_D5
A5	MM_DS_P0	A6	MM_DS_N0	A7	MM_DM0	A8	MM_D12
A9	MM_BA1	A10	MM_A6	A11	MM_BA2	A12	MM_A4
A13	MM_A8	A14	MM_VREF	A15	MM_CKE	A16	MM_CLK_P
A17	MM_CLK_N	A18	MM_RAS_N	A19	MM_D17	A20	MM_D16
A21	MM_DS_P3	A22	MM_DS_N3	A23	MM_D22	A24	MM_D29
A25	MM_DM3	A26	MM_D31	-	-	-	-
Row B							
B1	VDI_D1	B2	MM_D4	B3	MM_D1	B4	MM_D6
B5	MM_D8	B6	MM_D10	B7	MM_D13	B8	MM_D15
B9	MM_D11	B10	MM_A2	B11	MM_A5	B12	MM_A1
B13	MM_A7	B14	MM_A9	B15	MM_CAS_N	B16	MM_A13
B17	MM_PVT	B18	MM_ODT	B19	MM_D19	B20	MM_D20
B21	MM_DS_P2	B22	MM_DS_N2	B23	MM_D21	B24	MM_D25
B25	MM_D24	B26	MM_D28	-	-	-	-

Table 3. Pin allocation table[1][2][3] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row C							
C1	VDI_D3	C2	MM_D2	C3	MM_DM1	C4	MM_D9
C5	MM_D7	C6	MM_DS_P1	C7	MM_DS_N1	C8	MM_D14
C9	MM_BA0	C10	n.c.	C11	MM_A0	C12	MM_A3
C13	MM_A10	C14	MM_A11	C15	MM_A12	C16	MM_CS_N
C17	MM_WE_N	C18	MM_D18	C19	$V_{SSA(DLL2)}$	C20	$V_{DDA(DLL2)}$
C21	MM_D23	C22	MM_DM2	C23	MM_D30	C24	MM_D26
C25	MM_D27	C26	n.c.	-	-	-	-
Row D							
D1	VDI_D4	D2	VDI_D0	D3	V_{SS}	D4	$V_{SSA(DDR/PLL)}$
D5	$V_{DDD(C)}$	D6	$V_{DDD(IO)(DDR)}$	D7	$V_{DDD(IO)(DDR)}$	D8	$V_{DDA(DLL0)}$
D9	$V_{DDD(IO)(DDR)}$	D10	$V_{DDD(IO)(DDR)}$	D11	$V_{DDD(IO)(DDR)}$	D12	$V_{DDD(C)}$
D13	$V_{DDD(IO)(DDR)}$	D14	$V_{DDA(DLL1)}$	D15	$V_{DDD(IO)(DDR)}$	D16	$V_{DDD(IO)(DDR)}$
D17	$V_{DDD(IO)(DDR)}$	D18	$V_{DDD(IO)(DDR)}$	D19	$V_{DDD(C)}$	D20	$V_{DDD(IO)(DDR)}$
D21	$V_{DDD(IO)(DDR)}$	D22	$V_{DDD(IO)(DDR)}$	D23	$V_{DDD(C)}$	D24	V_{SS}
D25	n.c.	D26	n.c.	-	-	-	-
Row E							
E1	VDI_D6	E2	VDI_D5	E3	$V_{DDD(IO)}$	E4	$V_{DDA(DDR/PLL)}$
E5	V_{SS}	E6	V_{SS}	E7	V_{SS}	E8	$V_{SSA(DLL0)}$
E9	V_{SS}	E10	V_{SS}	E11	V_{SS}	E12	V_{SS}
E13	V_{SS}	E14	$V_{SSA(DLL1)}$	E15	V_{SS}	E16	V_{SS}
E17	V_{SS}	E18	V_{SS}	E19	V_{SS}	E20	V_{SS}
E21	V_{SS}	E22	V_{SS}	E23	$V_{DDD(IO)(DDR)}$	E24	V_{SS}
E25	n.c.	E26	n.c.	-	-	-	-
Row F							
F1	VDI_D7	F2	VDI_D8	F3	CLKOUT	F4	V_{SS}
F5	$V_{DDD(C)}$	F22	V_{SS}	F23	$V_{DDD(IO)(DDR)}$	F24	V_{SS}
F25	n.c.	F26	n.c.	-	-	-	-
Row G							
G1	GPIO15	G2	GPIO38	G3	VDI_D9	G4	VDI_D10
G5	$V_{DDD(IO)}$	G22	V_{SS}	G23	V_{SS}	G24	VDO_D0
G25	VDO_D3	G26	VDO_D1	-	-	-	-
Row H							
H1	VDI_CLK1	H2	VDI_D11	H3	VDI_D13	H4	GPIO14
H5	$V_{DDD(C)}$	H22	$V_{DDD(IO)(DDR)}$	H23	V_{SS}	H24	VDO_D4
H25	VDO_D2	H26	VDO_D5	-	-	-	-
Row J							
J1	VDI_D14	J2	VDI_D15	J3	VDI_D12	J4	GPIO34
J5	V_{SS}	J22	V_{SS}	J23	V_{SS}	J24	VDO_D6
J25	VDO_D7	J26	VDO_D8	-	-	-	-

Table 3. Pin allocation table[1][2][3] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row K							
K1	GPIO10	K2	GPIO11	K3	GPIO12	K4	V_{SS}
K5	$V_{DDD(IO)}$	K22	$V_{DDD(IO)(DDR)}$	K23	V_{SS}	K24	VDO_D9
K25	VDO_D12	K26	VDO_D11	-	-	-	-
Row L							
L1	VDI_CLK0	L2	GPIO32	L3	GPIO33	L4	GPIO13
L5	$V_{DDD(IO)}$	L11	V_{SS}	L12	V_{SS}	L13	V_{SS}
L14	V_{SS}	L15	V_{SS}	L16	V_{SS}	L22	$V_{DDD(C)}$
L23	V_{SS}	L24	VDO_D10	L25	VDO_D13	L26	VDO_D14
Row M							
M1	GPIO30	M2	GPIO29	M3	GPIO28	M4	GPIO31
M5	$V_{DDD(C)}$	M11	V_{SS}	M12	V_{SS}	M13	V_{SS}
M14	V_{SS}	M15	V_{SS}	M16	V_{SS}	M22	V_{SS}
M23	V_{SS}	M24	VDO_D15	M25	VDO_D16	M26	VDO_D17
Row N							
N1	VDI_CLK2	N2	GPIO17	N3	GPIO39	N4	GPIO27
N5	V_{SS}	N11	V_{SS}	N12	V_{SS}	N13	V_{SS}
N14	V_{SS}	N15	V_{SS}	N16	V_{SS}	N22	$V_{DDD(IO)}$
N23	V_{SS}	N24	VDO_D18	N25	VDO_D20	N26	VDO_D19
Row P							
P1	$V_{DDA(OSC)}$	P2	$V_{SSA(CGU/PLL)}$	P3	$V_{DDA(CGU/PLL)}$	P4	$V_{SSA(CAB/DDS)}$
P5	$V_{DDA(CAB)(3V3)}$	P11	V_{SS}	P12	V_{SS}	P13	V_{SS}
P14	V_{SS}	P15	V_{SS}	P16	V_{SS}	P22	V_{SS}
P23	V_{SS}	P24	VDO_D21	P25	VDO_CLK	P26	VDO_D23
Row R							
R1	XTAL_O	R2	$V_{SSA(CAB)}$	R3	$V_{DDA(CAB)(1V2)}$	R4	$V_{DDA(CAB/DDS)}$
R5	V_{SS}	R11	V_{SS}	R12	V_{SS}	R13	V_{SS}
R14	V_{SS}	R15	V_{SS}	R16	V_{SS}	R22	$V_{DDD(IO)}$
R23	VDO_D22	R24	VDO_D24	R25	V_{SS}	R26	VDO_D25
Row T							
T1	XTAL_I	T2	$V_{SSA(OSC)}$	T3	$V_{SSA(CAB/DDS)}$	T4	$V_{DDD(IO)}$
T5	$V_{DDD(C)}$	T11	V_{SS}	T12	V_{SS}	T13	V_{SS}
T14	V_{SS}	T15	V_{SS}	T16	V_{SS}	T22	$V_{DDD(C)}$
T23	VDO_D27	T24	VDO_D26	T25	VDO_D28	T26	VDO_D29
Row U							
U1	GPIO50	U2	AO12_BCK	U3	GPIO49	U4	AO12_OSCLK
U5	V_{SS}	U22	V_{SS}	U23	VDO_D32	U24	VDO_D30
U25	$V_{DDD(IO)}$	U26	VDO_D31	-	-	-	-

Table 3. Pin allocation table[1][2][3] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row V							
V1	AO12_WS	V2	GPIO51	V3	GPIO52	V4	GPIO44
V5	$V_{DDD(IO)}$	V22	$V_{DDD(C)}$	V23	VDO_AUX	V24	VDO_D33
V25	VDO_D34	V26	VDO_D35	-	-	-	-
Row W							
W1	GPIO40	W2	GPIO41	W3	GPIO45	W4	$V_{DDD(C)}$
W5	V_{SS}	W22	$V_{DDD(IO)}$	W23	$V_{DDD(IO)}$	W24	VDO_HOR
W25	VDO_VER	W26	SYS_RST_OUT_N	-	-	-	-
Row Y							
Y1	GPIO9	Y2	GPIO46	Y3	GPIO42	Y4	GPIO43
Y5	$V_{DDD(IO)(PCI)}$	Y22	$V_{DDD(C)}$	Y23	GPIO1	Y24	GPIO2
Y25	GPIO0	Y26	GPIO3	-	-	-	-
Row AA							
AA1	V_{SS}	AA2	V_{SS}	AA3	$V_{SSA(TERM)(USB)}$	AA4	USB_VBUS
AA5	V_{SS}	AA22	$V_{DDD(C)}$	AA23	GPIO7	AA24	GPIO6
AA25	GPIO5	AA26	GPIO4	-	-	-	-
Row AB							
AB1	USB_DM	AB2	$V_{SSA(REF)(USB)}$	AB3	$V_{SSA(USB)}$	AB4	USB_ID
AB5	$V_{DDD(IO)(PCI)}$	AB6	V_{SS}	AB7	V_{SS}	AB8	$V_{DDD(C)}$
AB9	$V_{DDD(IO)(PCI)}$	AB10	V_{SS}	AB11	$V_{DDD(C)}$	AB12	V_{SS}
AB13	$V_{DDD(C)}$	AB14	V_{SS}	AB15	$V_{DDD(IO)(PCI)}$	AB16	V_{SS}
AB17	$V_{DDD(C)}$	AB18	V_{SS}	AB19	$V_{DDD(IO)(PCI)}$	AB20	V_{SS}
AB21	$V_{DDD(IO)(PCI)}$	AB22	V_{SS}	AB23	$V_{DDD(C)}$	AB24	$V_{DDD(IO)}$
AB25	V_{SS}	AB26	n.c.	-	-	-	-
Row AC							
AC1	USB_DP	AC2	$V_{DDA(USB)}$	AC3	$V_{DDA(DRV)(USB)}$	AC4	V_{SS}
AC5	$V_{DDD(IO)(PCI)}$	AC6	PCI_AD31	AC7	$V_{DDD(IO)(PCI)}$	AC8	V_{SS}
AC9	PCI_IRDY_N	AC10	$V_{DDD(IO)(PCI)}$	AC11	PCI_AD7	AC12	$V_{DDD(IO)(PCI)}$
AC13	PCI_PAR	AC14	V_{SS}	AC15	PCI_AD8	AC16	$V_{DDD(IO)(PCI)}$
AC17	PCI_AD2	AC18	$V_{DDD(IO)(PCI)}$	AC19	GPIO21	AC20	GPIO58
AC21	GPIO56	AC22	GPIO16	AC23	$V_{DDD(IO)}$	AC24	$V_{DDD(IO)}$
AC25	V_{SS}	AC26	n.c.	-	-	-	-
Row AD							
AD1	GPIO48	AD2	GPIO47	AD3	USB_RREF	AD4	PCI_SYS_CLK
AD5	GPIO18	AD6	PCI_AD27	AD7	PCI_CLK	AD8	PCI_CBE3_N
AD9	PCI_AD21	AD10	PCI_AD18	AD11	PCI_TRDY_N	AD12	PCI_SERR_N
AD13	PCI_AD14	AD14	PCI_AD10	AD15	PCI_AD15	AD16	PCI_AD11
AD17	PCI_CBE0_N	AD18	GPIO37	AD19	GPIO35	AD20	GPIO26
AD21	GPIO22	AD22	GPIO54	AD23	V_{SS}	AD24	V_{SS}
AD25	TCK	AD26	RESET_IN_N	-	-	-	-

Table 3. Pin allocation table[1][2][3] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row AE							
AE1	USB_RPU	AE2	$V_{DDD(C)}$	AE3	PCI_AD30	AE4	GPIO60
AE5	PCI_AD28	AE6	PCI_IDSEL	AE7	PCI_AD23	AE8	PCI_AD24
AE9	PCI_AD19	AE10	PCI_AD16	AE11	PCI_AD13	AE12	PCI_CBE2_N
AE13	PCI_STOP_N	AE14	PCI_AD0	AE15	PCI_AD1	AE16	PCI_AD4
AE17	GPIO59	AE18	PCI_AD6	AE19	GPIO25	AE20	GPIO23
AE21	GPIO19	AE22	GPIO8	AE23	GPIO53	AE24	TDO
AE25	TDI	AE26	POR_IN_N	-	-	-	-
Row AF							
AF1	V_{SS}	AF2	V_{SS}	AF3	PCI_AD29	AF4	PCI_INTA_N
AF5	PCI_AD26	AF6	$V_{DDA(FB)(1V2)}$	AF7	PCI_AD25	AF8	PCI_AD22
AF9	PCI_AD20	AF10	PCI_AD17	AF11	PCI_DEVSEL_N	AF12	PCI_FRAME_N
AF13	PCI_PERR_N	AF14	PCI_CBE1_N	AF15	GPIO36	AF16	PCI_AD12
AF17	PCI_AD9	AF18	PCI_AD5	AF19	PCI_AD3	AF20	GPIO24
AF21	GPIO20	AF22	GPIO57	AF23	GPIO55	AF24	TMS
AF25	SDA	AF26	SCL	-	-	-	-

[1] See Section 8.1 for more functions available through the multiplexed GPIO interface and its default configuration. This interface extends functionality for digital video, extended I/O, host access, PCI-bus, USB-bus, digital audio, clocks and generic functions. Please keep in mind that some combinations may be mutually exclusive, depending on the specific application.

[2] See Table 6 for type specific availability of DDR SDRAM pins MM_x.

[3] n.c. indicate pins, which aren't connected internally to the die. Those pins have no electrical function; see Table 17.

6.2 Pin description

Table 4. Pin description overview

Pin category[1]	Table number
Power supply pins	Table 5
DDR SDRAM memory interface pins	Table 6
Digital video input interface pins	Table 7
Digital video output interface pins	Table 8
Digital audio interface pins	Table 9
Multifunctional GPIO interface pins	Table 10
PCI-bus interface pins	Table 11
USB-bus interface pins	Table 12
JTAG interface pins	Table 13
I^2C-bus interface pins	Table 14
Main control pins	Table 15
Crystal oscillator pins	Table 16
Not connected pins	Table 17

[1] See Section 8.1 for multiplexed GPIO functionality for video, XIO, host interface, PCI-bus, USB-bus, audio, clocks and generic functions.

Table 5. Pin description (power supplies)

Symbol	Pin	Type[1]	Description
Analog supply voltage pins			
$V_{DDA(CAB)(1V2)}$	R3	PS	CAB analog supply voltage (1.2 V)
$V_{DDA(CAB)(3V3)}$	P5	PS	CAB analog supply voltage (3.3 V)
$V_{DDA(CAB/DDS)}$	R4	PS	CAB/DDS analog supply voltage
$V_{DDA(CGU/PLL)}$	P3	PS	CGU/PLL analog supply voltage
$V_{DDA(DDR/PLL)}$	E4	PS	DDR/PLL analog supply voltage
$V_{DDA(DLL0)}$	D8	PS	DLL0 analog supply voltage
$V_{DDA(DLL1)}$	D14	PS	DLL1 analog supply voltage
$V_{DDA(DLL2)}$	C20	PS	DLL2 analog supply voltage
$V_{DDA(OSC)}$	P1	PS	oscillator analog supply voltage
$V_{DDA(DRV)(USB)}$	AC3	PS	USB driver analog supply voltage
$V_{DDA(FB)(1V2)}$	AF6	PS	FB analog supply voltage (1.2 V)
$V_{DDA(USB)}$	AC2	PS	USB analog supply voltage
Digital supply voltage pins			
$V_{DDD(C)}$	D5, D12, D19, D23, F5, H5, L22, M5, T5, T22, V22, W4, Y22, AA22, AB8, AB11, AB13, AB17, AB23 and AE2	PS	core digital supply voltage
$V_{DDD(IO)}$	E3, G5, K5, L5, N22, R22, T4, U25, V5, W22, W23, AB24, AC23 and AC24	PS	I/O digital supply voltage
$V_{DDD(IO)(DDR)}$	D6, D7, D9 to D11, D13, D15 to D18, D20 to D22, E23, F23, H22 and K22	PS	DDR input/output digital supply voltage
$V_{DDD(IO)(PCI)}$	Y5, AB5, AB9, AB15, AB19, AB21, AC5, AC7, AC10, AC12, AC16 and AC18	PS	PCI input/output digital supply voltage, 5 Volt tolerant
Ground supply voltage pins			
V_{SS}	D3, D24, E5 to E7, E9 to E13, E15 to E22, E24, F4, F22, F24, G22, G23, H23, J5, J22, J23, K4, K23, L11 to L16, L23, M11 to M16, M22, M23, N5, N11 to N16, N23, P11 to P16, P22, P23, R5, R11 to R16, R25, T11 to T16, U5, U22, W5, AA1, AA2, AA5, AB6, AB7, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AB25, AC4, AC8, AC14, AC25, AD23, AD24, AF1 and AF2	G	ground supply voltage
$V_{SSA(CAB)}$	R2	G	CAB analog ground supply voltage
$V_{SSA(CAB/DDS)}$	P4 and T3	G	CAB/DDS analog ground supply voltage
$V_{SSA(CGU/PLL)}$	P2	G	CGU/PLL analog ground supply voltage
$V_{SSA(DDR/PLL)}$	D4	G	DDR/PLL analog ground supply voltage
$V_{SSA(DLL0)}$	E8	G	DLL0 analog ground supply voltage
$V_{SSA(DLL1)}$	E14	G	DLL1 analog ground supply voltage
$V_{SSA(DLL2)}$	C19	G	DLL2 analog ground supply voltage
$V_{SSA(OSC)}$	T2	G	oscillator analog ground supply voltage

Table 5. Pin description (power supplies) *...continued*

Symbol	Pin	Type[1]	Description
$V_{SSA(REF)(USB)}$	AB2	G	USB reference analog ground supply voltage
$V_{SSA(TERM)(USB)}$	AA3	G	USB termination analog ground supply voltage
$V_{SSA(USB)}$	AB3	G	USB analog ground supply voltage

[1] Table 18 defines the pin type.

Table 6. Pin description (DDR SDRAM memory interface)

Symbol	Pin		Type[1]		Description
	PNX9530; PNX9531	PNX9535			
MM_A13	B16	B16	A-O	-	address bit 13
MM_A12	C15	C15	A-O	-	address bit 12
MM_A11	C14	C14	A-O	-	address bit 11
MM_A10	C13	C13	A-O	-	address bit 10
MM_A9	B14	B14	A-O	-	address bit 9
MM_A8	A13	A13	A-O	-	address bit 8
MM_A7	B13	B13	A-O	-	address bit 7
MM_A6	A10	A10	A-O	-	address bit 6
MM_A5	B11	B11	A-O	-	address bit 5
MM_A4	A12	A12	A-O	-	address bit 4
MM_A3	C12	C12	A-O	-	address bit 3
MM_A2	B10	B10	A-O	-	address bit 2
MM_A1	B12	B12	A-O	-	address bit 1
MM_A0	C11	C11	A-O	-	address bit 0
MM_BA2	A11	A11	A-O	-	bank address bit 2
MM_BA1	A9	A9	A-O	-	bank address bit 1
MM_BA0	C9	C9	A-O	-	bank address bit 0
MM_CAS_N	B15	B15	A-O	PU	column address selector (active LOW)
MM_CKE	A15	A15	AF-O	PD	clock enable
MM_CLK_N	A17	A17	C-O	PU	negative clock
MM_CLK_P	A16	A16	C-O	PU	positive clock
MM_CS_N	C16	C16	A-O	-	chip select (active LOW)
MM_D31	A26	-	D-IO	-	data bit 31
MM_D30	C23	-	D-IO	-	data bit 30
MM_D29	A24	-	D-IO	-	data bit 29
MM_D28	B26	-	D-IO	-	data bit 28
MM_D27	C25	-	D-IO	-	data bit 27
MM_D26	C24	-	D-IO	-	data bit 26
MM_D25	B24	-	D-IO	-	data bit 25
MM_D24	B25	-	D-IO	-	data bit 24
MM_D23	C21	-	D-IO	-	data bit 23
MM_D22	A23	-	D-IO	-	data bit 22
MM_D21	B23	-	D-IO	-	data bit 21

Table 6. Pin description (DDR SDRAM memory interface) *…continued*

Symbol	Pin		Type[1]		Description
	PNX9530; PNX9531	PNX9535			
MM_D20	B20	-	D-IO	-	data bit 20
MM_D19	B19	-	D-IO	-	data bit 19
MM_D18	C18	-	D-IO	-	data bit 18
MM_D17	A19	-	D-IO	-	data bit 17
MM_D16	A20	-	D-IO	-	data bit 16
MM_D15	B8	B8	D-IO	-	data bit 15
MM_D14	C8	C8	D-IO	-	data bit 14
MM_D13	B7	B7	D-IO	-	data bit 13
MM_D12	A8	A8	D-IO	-	data bit 12
MM_D11	B9	B9	D-IO	-	data bit 11
MM_D10	B6	B6	D-IO	-	data bit 10
MM_D9	C4	C4	D-IO	-	data bit 9
MM_D8	B5	B5	D-IO	-	data bit 8
MM_D7	C5	C5	D-IO	-	data bit 7
MM_D6	B4	B4	D-IO	-	data bit 6
MM_D5	A4	A4	D-IO	-	data bit 5
MM_D4	B2	B2	D-IO	-	data bit 4
MM_D3	A3	A3	D-IO	-	data bit 3
MM_D2	C2	C2	D-IO	-	data bit 2
MM_D1	B3	B3	D-IO	-	data bit 1
MM_D0	A2	A2	D-IO	-	data bit 0
MM_DM3	A25	-	A-O	-	data write enable for byte 3, i.e. MM_D[31:24]
MM_DM2	C22	-	A-O	-	data write enable for byte 2, i.e. MM_D[23:16]
MM_DM1	C3	C3	A-O	-	data write enable for byte 1, i.e. MM_D[15:8]
MM_DM0	A7	A7	A-O	-	data write enable for byte 0, i.e. MM_D[7:0]
MM_DS_N3	A22	-	R-IO	-	negative data strobe for byte 3, i.e. MM_D[31:24]
MM_DS_N2	B22	-	R-IO	-	negative data strobe for byte 2, i.e. MM_D[23:16]
MM_DS_N1	C7	C7	R-IO	-	negative data strobe for byte 1, i.e. MM_D[15:8]
MM_DS_N0	A6	A6	R-IO	-	negative data strobe for byte 0, i.e. MM_D[7:0]
MM_DS_P3	A21	-	R-IO	-	positive data strobe for byte 3, i.e. MM_D[31:24]
MM_DS_P2	B21	-	R-IO	-	positive data strobe for byte 2, i.e. MM_D[23:16]
MM_DS_P1	C6	C6	R-IO	-	positive data strobe for byte 1, i.e. MM_D[15:8]
MM_DS_P0	A5	A5	R-IO	-	positive data strobe for byte 0, i.e. MM_D[7:0]
MM_ODT	B18	B18	AF-O	-	on-die termination
MM_PVT	B17	B17	AR	-	process voltage temperature compensation
MM_RAS_N	A18	A18	A-O	PU	row address selector (active LOW)
MM_VREF	A14	A14	AI	-	reference voltage[2]
MM_WE_N	C17	C17	A-O	-	write enable (active LOW)

[1] Table 18 defines the pin type.

[2] Connect to $V_{DDD(IO)(DDR)}$ through a 130 Ω ± 1 % voltage divider.

Table 7. Pin description (digital video input interface)[1]

Symbol	Pin	Type[2]		Description
VDI_CLK2	N1	H-IO	PU	clock 2
VDI_CLK1	H1	H-IO	PU	clock 1
VDI_CLK0	L1	H-IO, H-OZ	PU	clock 0
VDI_D15	J2	F-I	PU	data bit 15
VDI_D14	J1	F-I	PU	data bit 14
VDI_D13	H3	F-I	PU	data bit 13
VDI_D12	J3	F-I	PU	data bit 12
VDI_D11	H2	F-I	PU	data bit 11
VDI_D10	G4	F-I	PU	data bit 10
VDI_D9	G3	F-I	PU	data bit 9
VDI_D8	F2	F-I	PU	data bit 8
VDI_D7	F1	F-I	PU	data bit 7
VDI_D6	E1	F-I	PU	data bit 6
VDI_D5	E2	F-I	PU	data bit 5
VDI_D4	D1	F-I	PU	data bit 4
VDI_D3	C1	F-I	PU	data bit 3
VDI_D2	A1	F-I	PU	data bit 2
VDI_D1	B1	F-I	PU	data bit 1
VDI_D0	D2	F-I	PU	data bit 0

[1] See Section 8.1 for more digital video input functions available through the multiplexed GPIO interface.

[2] Table 18 defines the pin type.

Table 8. Pin description (digital video output interface)[1]

Symbol	Pin	Type[2]		Description
VDO_AUX	V23	F-OZ	PD	auxiliary video output
VDO_CLK	P25	H-IO	PD	video clock input and output
VDO_D35	V26	F-OZ	PD	data bit 35
VDO_D34	V25	F-OZ	PD	data bit 34
VDO_D33	V24	F-OZ	PD	data bit 33
VDO_D32	U23	F-OZ	PD	data bit 32
VDO_D31	U26	F-OZ	PD	data bit 31
VDO_D30	U24	F-OZ	PD	data bit 30
VDO_D29	T26	F-OZ	PD	data bit 29
VDO_D28	T25	F-OZ	PD	data bit 28
VDO_D27	T23	F-OZ	PD	data bit 27
VDO_D26	T24	F-OZ	PD	data bit 26
VDO_D25	R26	F-OZ	PD	data bit 25
VDO_D24	R24	F-OZ	PD	data bit 24
VDO_D23	P26	F-OZ	PD	data bit 23
VDO_D22	R23	F-OZ	PD	data bit 22

Table 8. Pin description (digital video output interface)[1] *...continued*

Symbol	Pin	Type[2]		Description
VDO_D21	P24	F-OZ	PD	data bit 21
VDO_D20	N25	F-OZ	PD	data bit 20
VDO_D19	N26	F-OZ	PD	data bit 19
VDO_D18	N24	F-OZ	PD	data bit 18
VDO_D17	M26	F-OZ	PD	data bit 17
VDO_D16	M25	F-OZ	PD	data bit 16
VDO_D15	M24	F-OZ	PD	data bit 15
VDO_D14	L26	F-OZ	PD	data bit 14
VDO_D13	L25	F-OZ	PD	data bit 13
VDO_D12	K25	F-OZ	PD	data bit 12
VDO_D11	K26	F-OZ	PD	data bit 11
VDO_D10	L24	F-OZ	PD	data bit 10
VDO_D9	K24	F-OZ	PD	data bit 9
VDO_D8	J26	F-OZ	PD	data bit 8
VDO_D7	J25	F-OZ	PD	data bit 7
VDO_D6	J24	F-OZ	PD	data bit 6
VDO_D5	H26	F-OZ	PD	data bit 5
VDO_D4	H24	F-OZ	PD	data bit 4
VDO_D3	G25	F-OZ	PD	data bit 3
VDO_D2	H25	F-OZ	PD	data bit 2
VDO_D1	G26	F-OZ	PD	data bit 1
VDO_D0	G24	F-OZ	PD	data bit 0
VDO_HOR	W24	F-OZ	PD	horizontal synchronization
VDO_VER	W25	F-IO	PD	vertical synchronization

[1] See Section 8.1 for more digital video output functions available through the multiplexed GPIO interface.

[2] Table 18 defines the pin type.

Table 9. Pin description (digital audio interface)[1]

Symbol	Pin	Type[2]		Description
AO12_BCK	U2	L-IO	PD	audio bit clock
AO12_OSCLK	U4	L-OZ	PU	audio oscillator clock
AO12_WS	V1	F-IO	PD	audio word select

[1] See Section 8.1 for more digital audio functions available through the multiplexed GPIO interface.

[2] Table 18 defines the pin type.

Table 10. Pin description (multifunctional GPIO interface)[1]

Symbol	Pin	Type[2]		Description
GPIO60	AE4	P-IO	-	general purpose input or output 60
GPIO59	AE17	P-I	-	general purpose input or output 59
GPIO58	AC20	P-O	-	general purpose input or output 58
GPIO57	AF22	P-O	-	general purpose input or output 57

Table 10. Pin description (multifunctional GPIO interface)[1] *…continued*

Symbol	Pin	Type[2]		Description
GPIO56	AC21	P-I	-	general purpose input or output 56
GPIO55	AF23	P-O	-	general purpose input or output 55
GPIO54	AD22	P-O	-	general purpose input or output 54
GPIO53	AE23	P-O	-	general purpose input or output 53
GPIO52	V3	S-O	PD	general purpose input or output 52
GPIO51	V2	S-O	PD	general purpose input or output 51
GPIO50	U1	S-O	PD	general purpose input or output 50
GPIO49	U3	S-O	PD	general purpose input or output 49
GPIO48	AD1	T-O	PD	general purpose input or output 48
GPIO47	AD2	T-I	PD	general purpose input or output 47
GPIO46	Y2	L-OZ	PU	general purpose input or output 46
GPIO45	W3	L-IO	PD	general purpose input or output 45
GPIO44	V4	F-IO	PD	general purpose input or output 44
GPIO43	Y4	S-IO	PD	general purpose input or output 43
GPIO42	Y3	S-IO	PD	general purpose input or output 42
GPIO41	W2	F-IO	PD	general purpose input or output 41
GPIO40	W1	L-IO	PD	general purpose input or output 40
GPIO39	N3	S-I, S-O	PD	general purpose input or output 39
GPIO38	G2	S-I	PD	general purpose input or output 38
GPIO37	AD18	P-I	-	general purpose input or output 37
GPIO36	AF15	P-IO	-	general purpose input or output 36
GPIO35	AD19	P-IO, P-I	-	general purpose input or output 35
GPIO34	J4	L-IO, L-I	PU	general purpose input or output 34
GPIO33	L3	F-IO	PU	general purpose input or output 33
GPIO32	L2	S-IO	PU	general purpose input or output 32
GPIO31	M4	S-IO	PU	general purpose input or output 31
GPIO30	M1	S-IO	PU	general purpose input or output 30
GPIO29	M2	S-IO	PU	general purpose input or output 29
GPIO28	M3	L-IO	PU	general purpose input or output 28
GPIO27	N4	F-IO	PU	general purpose input or output 27
GPIO26	AD20	T-IO	PU	general purpose input or output 26
GPIO25	AE19	T-IO	PU	general purpose input or output 25
GPIO24	AF20	T-IO	PU	general purpose input or output 24
GPIO23	AE20	T-IO	PU	general purpose input or output 23
GPIO22	AD21	T-IO	PU	general purpose input or output 22
GPIO21	AC19	T-IO	PU	general purpose input or output 21
GPIO20	AF21	T-IO	PU	general purpose input or output 20
GPIO19	AE21	T-IO	PU	general purpose input or output 19
GPIO18	AD5	P-IO	-	general purpose input or output 18
GPIO17	N2	S-IO	PU	general purpose input or output 17

Table 10. Pin description (multifunctional GPIO interface)[1] *…continued*

Symbol	Pin	Type[2]		Description
GPIO16	AC22	T-O, T-OD	PU	general purpose input or output 16
GPIO15	G1	S-I	PU	general purpose input or output 15
GPIO14	H4	S-I	PD	general purpose input or output 14
GPIO13	L4	S-O	PD	general purpose input or output 13
GPIO12	K3	IO, OZ	PD	general purpose input or output 12
GPIO11	K2	L-O	PD	general purpose input or output 11
GPIO10	K1	F-O	PD	general purpose input or output 10
GPIO9	Y1	L-OZ	PU	general purpose input or output 9
GPIO8	AE22	T-O, T-I	PU	general purpose input or output 8
GPIO7	AA23	T-IO, T-D	PD	general purpose input or output 7
GPIO6	AA24	F-IO, F-D	PD	general purpose input or output 6
GPIO5	AA25	F-IO, F-D	PD	general purpose input or output 5
GPIO4	AA26	F-IO, F-D	PD	general purpose input or output 4
GPIO3	Y26	F-IO, F-D	PD	general purpose input or output 3
GPIO2	Y24	F-IO, F-D	PU	general purpose input or output 2
GPIO1	Y23	F-IO, F-D	PU	general purpose input or output 1
GPIO0	Y25	F-IO, F-D	PU	general purpose input or output 0

[1] See Section 8.1 for all functions and the default configuration of the multiplexed, multifunctional GPIO interface. GPIO[6:0] can be selecteds as clocks. Data may only appear at GPIO[60:0].

[2] Table 18 defines the pin type.

Table 11. Pin description (PCI-bus interface)[1]

Symbol	Pin	Type[2]		Description
PCI_AD31	AC6	P-IO	-	bit 31 of the PCI address and data bus
PCI_AD30	AE3	P-IO	-	bit 30 of the PCI address and data bus
PCI_AD29	AF3	P-IO	-	bit 29 of the PCI address and data bus
PCI_AD28	AE5	P-IO	-	bit 28 of the PCI address and data bus
PCI_AD27	AD6	P-IO	-	bit 27 of the PCI address and data bus
PCI_AD26	AF5	P-IO	-	bit 26 of the PCI address and data bus
PCI_AD25	AF7	P-IO	-	bit 25 of the PCI address and data bus
PCI_AD24	AE8	P-IO	-	bit 24 of the PCI address and data bus
PCI_AD23	AE7	P-IO	-	bit 23 of the PCI address and data bus
PCI_AD22	AF8	P-IO	-	bit 22 of the PCI address and data bus
PCI_AD21	AD9	P-IO	-	bit 21 of the PCI address and data bus
PCI_AD20	AF9	P-IO	-	bit 20 of the PCI address and data bus
PCI_AD19	AE9	P-IO	-	bit 19 of the PCI address and data bus
PCI_AD18	AD10	P-IO	-	bit 18 of the PCI address and data bus
PCI_AD17	AF10	P-IO	-	bit 17 of the PCI address and data bus
PCI_AD16	AE10	P-IO	-	bit 16 of the PCI address and data bus
PCI_AD15	AD15	P-IO	-	bit 15 of the PCI address and data bus

Table 11. Pin description (PCI-bus interface)[1] *…continued*

Symbol	Pin	Type[2]		Description
PCI_AD14	AD13	P-IO	-	bit 14 of the PCI address and data bus
PCI_AD13	AE11	P-IO	-	bit 13 of the PCI address and data bus
PCI_AD12	AF16	P-IO	-	bit 12 of the PCI address and data bus
PCI_AD11	AD16	P-IO	-	bit 11 of the PCI address and data bus
PCI_AD10	AD14	P-IO	-	bit 10 of the PCI address and data bus
PCI_AD9	AF17	P-IO	-	bit 9 of the PCI address and data bus
PCI_AD8	AC15	P-IO	-	bit 8 of the PCI address and data bus
PCI_AD7	AC11	P-IO	-	bit 7 of the PCI address and data bus
PCI_AD6	AE18	P-IO	-	bit 6 of the PCI address and data bus
PCI_AD5	AF18	P-IO	-	bit 5 of the PCI address and data bus
PCI_AD4	AE16	P-IO	-	bit 4 of the PCI address and data bus
PCI_AD3	AF19	P-IO	-	bit 3 of the PCI address and data bus
PCI_AD2	AC17	P-IO	-	bit 2 of the PCI address and data bus
PCI_AD1	AE15	P-IO	-	bit 1 of the PCI address and data bus
PCI_AD0	AE14	P-IO	-	bit 0 of the PCI address and data bus
PCI_CBE3_N	AD8	P-IO	-	bus command and byte enable 3 of the PCI-bus interface (active LOW)
PCI_CBE2_N	AE12	P-IO	-	bus command and byte enable 2 of the PCI-bus interface (active LOW)
PCI_CBE1_N	AF14	P-IO	-	bus command and byte enable 1 of the PCI-bus interface (active LOW)
PCI_CBE0_N	AD17	P-IO	-	bus command and byte enable 0 of the PCI-bus interface (active LOW)
PCI_CLK	AD7	P-I	-	clock signal of the PCI-bus interface
PCI_DEVSEL_N	AF11	P-I	-	device select signal of the PCI-bus interface (active LOW)
PCI_FRAME_N	AF12	P-I	-	frame signal of the PCI-bus interface (active LOW)
PCI_IDSEL	AE6	P-I	-	initialization device select signal of the PCI-bus interface
PCI_INTA_N	AF4	P-I, P-OD	-	interrupt signal of the PCI-bus interface (active LOW)
PCI_IRDY_N	AC9	P-IO	-	initiator ready signal of the PCI-bus interface (active LOW)
PCI_PAR	AC13	P-IO	-	parity signal of the PCI-bus interface
PCI_PERR_N	AF13	P-IO	-	parity error signal of the PCI-bus interface (active LOW)
PCI_SERR_N	AD12	P-OD	-	system error signal of the PCI-bus interface (active LOW)
PCI_STOP_N	AE13	P-IO	-	stop signal of the PCI-bus interface (active LOW)
PCI_SYS_CLK	AD4	P-IO	PU	system clock signal of the PCI-bus interface
PCI_TRDY_N	AD11	P-IO	-	target ready signal of the PCI-bus interface (active LOW)

[1] See Section 8.1 for more PCI-bus functions available through the multiplexed GPIO interface.

[2] Table 18 defines the pin type.

Table 12. Pin description (USB-bus interface)[1]

Symbol	Pin	Type[2]		Description
USB_DM	AB1	U-IO	-	minus data I/O of the USB-bus interface
USB_DP	AC1	U-IO	-	positive data I/O of the USB-bus interface
USB_ID	AB4	U-I	-	type identification input of the USB-bus interface
USB_RPU	AE1	U-I	-	pull-up resistor of the USB-bus interface
USB_RREF	AD3	U-IO	-	resistor reference of the USB-bus interface[3]
USB_VBUS	AA4	U-IO	-	bus voltage of the USB-bus interface

[1] See Section 8.1 for more USB-bus functions available through the multiplexed GPIO interface.

[2] Table 18 defines the pin type.

[3] Connect through a 12 kΩ ± 1 % resistance to the analog ground plane, which connects to pin $V_{SSA(USB)}$.

Table 13. Pin description (JTAG interface)

Symbol	Pin	Type[1]		Description
TCK	AD25	T-I	PU	test clock input
TDI	AE25	T-I	PU	test serial data input
TDO	AE24	L-OZ	-	test serial data output
TMS	AF24	T-I	PU	test mode select input

[1] Table 18 defines the pin type.

Table 14. Pin description (I²C-bus interface)

Symbol	Pin	Type[1]		Description
SCL	AF26	I2-I, I2-OD	-	serial clock input and output
SDA	AF25	I2-I, I2-OD	-	serial data input and output

[1] Table 18 defines the pin type.

Table 15. Pin description (main control pins)

Symbol	Pin	Type[1]		Description
CLKOUT	F3	H-IO	PU	clock output
POR_IN_N	AE26	T-I	PU	power-on reset input (active LOW)
RESET_IN_N	AD26	T-I	PU	master reset input (active LOW)
SYS_RST_OUT_N	W26	H-O	PU	system reset output (active LOW)

[1] Table 18 defines the pin type.

Table 16. Pin description (crystal oscillator pins)

Symbol	Pin	Type[1]		Description
XTAL_I	T1	AI	-	crystal oscillator analog input
XTAL_O	R1	AO	-	crystal oscillator analog output

[1] Table 18 defines the pin type.

Table 17. Pin description (not connected pins)

Symbol	Pin	Type	Description
PNX9530, PNX9531 and PNX9535			
n.c.	C10, C26, D25, D26, E25, E26, F25, F26, AB26 and AC26	-	not connected
PNX9535 only			
n.c.	A19 to A26, B19 to B26, C18 and C21 to C25	-	not connected

Table 18. Pin type description

Pin types are either generic or a combination of type and function. Examples are AO and P-OD.

Type	Description
Generic	
AI	analog input pin
AO	analog output pin
AR	analog reference pin
G	ground pin
PS	power supply pin
Combined	
Type	
A	Address pin
AF	Address pin with Forced low output during power-down
C	Clock pin
D	Data pin
F	Fast pin (1 ns slew rate)
H	High-speed clock pin
I2	I^2C-bus pin; 3.3 V signaling, 5 V tolerant
L	Low-speed clock pin
P	PCI Local Bus 2.2 specification compliant pin; 3.3 V signaling, 5 V tolerant
R	stRobe pin
S	Slow pin (3 ns slew rate)
T	5 V Tolerant input
U	5 V tolerant USB-bus pin
Function	
I	Input
O	Output
IO	Input and Output
I/O	Input or Output
I/OD	Input or Output with open Drain
I/O/D	Input or Output or open Drain output with input
OD	Open Drain output
OZ	3-state Output
Resistor	
PD	pull-down
PU	pull-up

7. Functional description

7.1 Digital video

7.1.1 Video input

The PNX9530; PNX9531; PNX9535 has a versatile ViDeo Input (VDI) module with a:

- Video Input Processor (VIP) for 8-bit, 10-bit, 16-bit or 20-bit YUV capture
- Fast General Purpose Interface (FGPI) for 8-bit, 16-bit or 24-bit capture.

See Section 8 for configuration examples of these multiplexed interfaces.

7.1.1.1 VIP

The VIP module accept a wides range of different video formats. The VIP interface is composed of 24 data pins VDI_D[23:0], five control pins VDI_V[2:0], VDI_HOR, VDI_VER and three video input clock pins VDI[2:0]_CLK. The VIP captures 8-bit or 10-bit streaming digital video from a parallel interface port.

Two parallel Digital Video (DV) ports are connected to the input of the VIP. The digital video is provided in an *ITU-R 656* compliant format, in a VESA compliant format or in a format with explicit synchronization signals. Typically, the digital video is YUV 4 : 2 : 2 encoded. Additionally, support is provided for RGB Bayer encoded video. Although only two DV ports are connected to the VIP, it is capable of capturing up to 8 digital video streams in parallel. This can be achieved by utilizing digital video decoders that time-multiplex 4 digital video streams into one stream, utilizing only one single DV port.

The VIP provided functionality is divided into the following steps, from capture to writing the video streams into main memory:

- Generate video stream test pattern
- Capture streams on the DV ports
- Decode streams
- Windowing of video streams; this step generates both a primary and an auxillary video stream
- Simple horizontal scaling (half resolution); co-sited or interspersed sampling of video data
- Dithering, to support translation of 10-bit video into 8-bit video
- Writing the video stream to main memory; support is provided for packed, semi-planar and planar memory layouts and 2-bit, 8-bit, 10-bit and 16-bit video data.

Decoding streams includes demultiplexing of multiple time-multiplexed video streams on a single logical DV port, combining the streams of two logical DV ports into a single High-Definition (HD) video stream and video image extraction. This step also includes the extraction of ancillary data that may be encoded in video blanking regions.

The windowing, scaling, dithering and writing to main memory steps are performed on each of the 8 video streams, each of which may be composed of a primary video stream, an auxillary video stream and an anicillary stream.

7.1.1.2 FGPI

In addition to the VIP module is the FGPI interface which shares the VDI pins. The FGPI module is a high-bandwidth input data channel. The FGPI packs four 8-bit samples, two 16-bit samples or one 32-bit sample of data into one 32-bit word, which is sent to main memory via DMA. 30-bit video input formats like RGB/YUV(4 : 4 : 4) can be cpatured using the FGPI.

The full bandwidth capabilities of FGPI are not used since there are only 24 data pins allocated to FGPI in the PNX9530; PNX9531; PNX9535 device.

The FGPI operates in two main modes, record capture or message passing:

- Can be used as a versatile interface with streaming data sources
- Can be used as a receiver port for inter-TriMedia unidirectional message passing
- Permits optional synchronization with external control signals like h-sync and v-sync to capture video data
- POptionally inserts timestamp information into packet sent to memory
- Optionally inserts information, like message or record length, into packet sent to memory
- Permits continuous data transfer using DMA transfers to two main memory buffers.

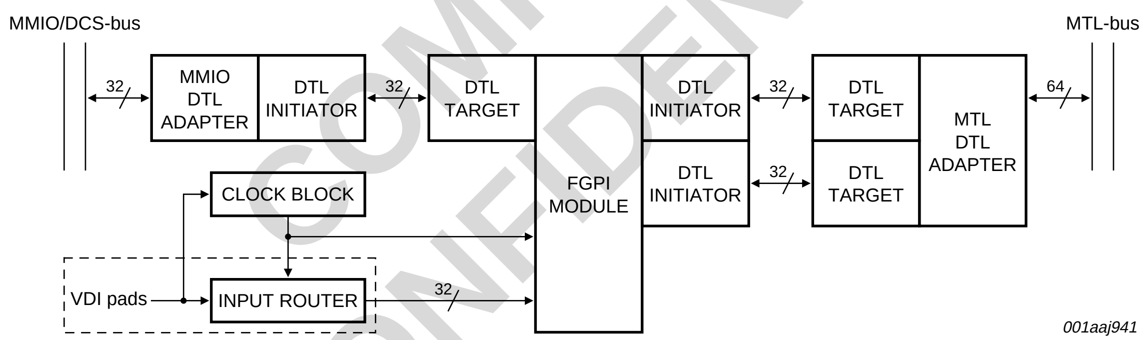


Fig 3. FPGI top level block diagram

7.1.2 Video output

The PNX9530; PNX9531; PNX9535 has a versatile ViDeo Output (VDO) module with a:

- DVD-Descrambler (DVD-D) module
- Quality video Composition Processor (QVCP) module
- Memory Based Scaler (MBS) module.

See Section 8 for configuration examples of these multiplexed interfaces.

The video output stream of the QVCP can be connected directly to the ViDeo Output (VDO) port VDO_D[35:0] of the PNX9530; PNX9531; PNX9535 in order to provide one video stream, but the PNX9530; PNX9531; PNX9535 can be used also to provide two different video streams to operate two LCD screens (i.e. for rear-seat entertainmant).

Therefore the user can configure the QVCP to provide a multiplexed video output stream to the VDO buffer. The VDO buffer is used to demultiplex two combined video streams from the QVCP into two 18-bit RGB or two 24-bit RGB video output streams.

The PNX9530; PNX9531; PNX9535 has a ViDeo Out Buffer (VDOB) for 2 × 24-bit RGB output mode. For restrictions see Table 19.

7.1.2.1 DVD-D

The PNX9530; PNX9531; PNX9535 provides Digital Versatile Disc-Descrambler (DVD-D) module providing the major processes:

- Authentiction process
- Key conversion process
- Main data descrambling process.

A DVD player system consists then of a DVD-ROM drive which accepts the DVD-ROM disc and reads the information from the disc to the drive controller. The drive controller connects the disc transport with an interconnecting bus (PCI-XIO) and hence to the host system (PNX9530; PNX9531; PNX9535). The host system interacts with the DVDD module to send authorization requests, receive authorization, replies, and transfer data between the DVD-ROM Drive and the DVDD module.

7.1.2.2 QVCP

The Quality video Composition Processor (QVCP) module is a high-resolution image composition and processing pipeline that facilitates both graphics and video processing. In combination with several other modules, it provides a new generation of graphics and video capability. QVCP provides its advanced functionality using a series of layers and mixers; a series of display-data layers (pixel streams) are created and logically mixed in sequence to render the composite output picture.

The QVCP module contains a total number of two layers and is mainly intended to be connected to a TV, a monitor or LCD panel. Due to the independence of the layers, a number of different scenarios is possible. However, in general, the QVCP has been designed to mix one video plane and one graphic plane. It can therefore be used to display a fully composited video image consisting of graphical information, lik ePIP or menu.

QVCP supports a whole range of progressive and interlaced display standards: for televisions, from standard-definition resolutions such as PAL or NTSC to all eighteen ATSC display formats such as 1080i or 720p, and for computer and LCD displays at 60 Hz and up to 1080p resolutions. The wide variety of output modes guarantees the compatibility with most present display-processor chips.

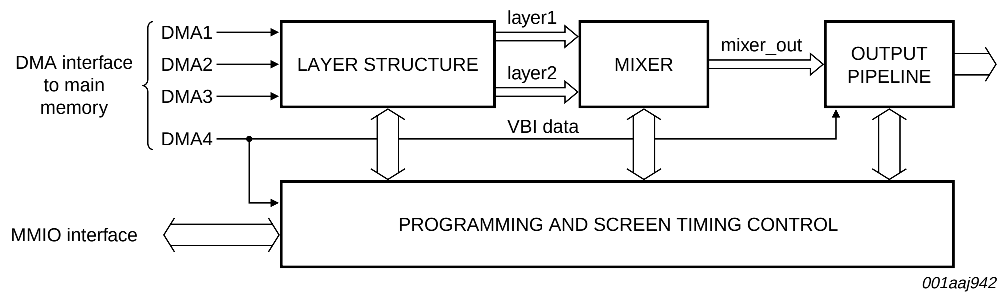


Fig 4. QVCP top level block diagram

In order to achieve high-quality video and graphics as demanded by future consumer products, a number of complex tasks need to be performed by the QVCP. The main functions of the video and graphics output pipeline are:

- Fetching of up to two video streams from memory
- Color expansion in case of non-full color or indexed data formats
- Reverse-gamma correction
- Video quality enhancement such as luminance sharpening, chroma transient improvement, histogram modification, skin-tone correction, blue stretch, and green enhancement
- Horizontal up-scaling for video and graphics images in both linear and panorama mode
- Adapting screen timing generation to the connected display requirements (SDTV standards, HDTV standards, progressive and interlaced formats)
- Color space uniqueness of all video streams
- Merging of thevideo streams (blend, invert and exchange)
- Positioning of the various video streams (including finer positioning)
- Brightness and contrast control on a for each video output stream
- Gamma correction and noise shaping of the final composited image
- Output format generation.

7.1.2.3 MBS

The captured data of the the VIP and the FPGI will get stored in main memory in the user defined address spaces. In order to enlarge or reduce the captured video images the PNX9530; PNX9531; PNX9535 has a Memory Based Scaler (MBS). Memory based scaling is done independent of any video clocks by reading the video data from memory and writing the scaled pictures back to the memory. A single scaler can therefore be used to scale more than one video stream sequentially.

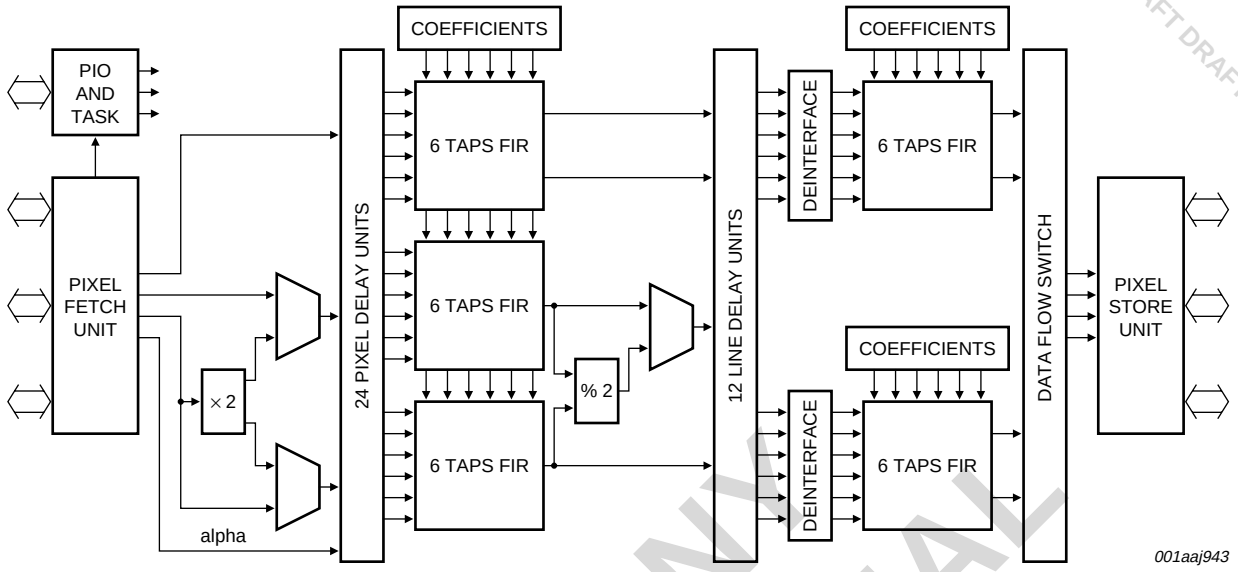


Fig 5. MBS block diagram

The memory-based scaler can perform the following operations:

- Vertical and horizontal scaling
  - Linear and non-linear aspect-ratio conversion (panorama scaling)
- De-interlacing
  - Simple median
  - Majority-selection (median filtering with previous field, spatial temporal average of 2 fields, same position from next or previous field depending on whether three or two field majority selection)

    Remark: Majority selection is done on luma only
  - Field insertion and line doubling (i.e., repeating the same line twice)
  - Edge-Dependent De-interlacing (EDDI), a post-processing step done on luma only
- Anti-flicker filtering
- Conversions between 4 : 2 : 0, 4 : 2 : 2 and 4 : 4 : 4
- Indexed to true color conversion
- Color expansion and compression (different quantizations for color components, e.g. RGB565 to RGB32)
- Deplanarization and planarization
- Variable color space conversion with programmable matrix coefficients (mutually exclusive with horizontal scaling)
- Color-key and alpha processing
  - Conversion between color-key and alpha
  - Alpha scaling
- Measurements
  - Histogram measurement

- Noise estimation
- Blackbar detection
- Blacklevel measurement
- UV bandwidth measurement
- Task list based programming.

Most of the above functions can be performed during a single pass, though the filter quality (length) may vary depending on the performed operations.

Special modes and features:

- Color key to alpha and alpha to color key conversion (color re-keying)
- Non-linear phase interpolation (phase LUT).

7.2 Digital audio

The PNX9530; PNX9531; PNX9535 has digital audio inputs and outputs:

- Audio Input 2 (AI2) for 8 channels and master of the synchronization
- Audio Output 2 (AO2) for 8 channels and master of the synchronization.

For restrictions see Table 19 and Section 7.1.1.

7.2.1 Audio input

The PNX9530; PNX9531; PNX9535 device has an Audio Input (AI) module to receive digital audio input streams.

The AI module can activate up to four audio input ports. Each audio input port processes single-channel or dual-channel sources. Hence the AI module can capture up to 8 channels of audio input (4 stereo channels).

The AI module includes four major subsystems: a programmable sample clock generator, a serial-to-parallel converter, a Device Transaction Level (DTL) initiator interface that initiates transfer of parallel data to a DTL-to-memory bus adapter and a MMIO type low latency DTL target interface for MMIO configuration registers.

The sampling clock can be used as either master or slave to the external audio. The sampling clock synchronizes the serial-to-parallel converter with the source data stream. The samples enter the serial-to-parallel converter, which reformats the data for the initiator. The initiator streams the parallel data in to the DTL-to-memory bus adapter.

The AI module provides a DMA-driven serial interface to an off-chip stereo Analog-to-Digital Converter (ADC), I^2S subsystem or other serial data source. AI provides all signals needed to connect to high-quality, low-cost oversampling ADCs. The AI module and external ADC (or I^2S subsystem) together are capable of generating a programmable sample clock by dividing a precise oversampling clock, which will be provided by the internal clock factory of the PNX9530; PNX9531; PNX9535.

The AI module has the following features:

- Four channels of audio input per port
- 16-bit or 32-bit samples per channel

- Programmable 1 Hz to 192 kHz sampling rate

  Remark: This is a practical range; the actual sample rate is application dependent
- Internal or external sampling clock source
- AI autonomously writes sampled audio data to memory using the internal DMA network
- 16-bit and 32-bit mono and stereo PC standard memory data formats
- Raw mode where the bits from all the active inputs are sampled by bit clock along with the frame sync signal (pin AI1_WS or AI2_WS) and stored in memory
- Little-endian or big-endian memory formats.

Remark: AC-97 codecs are not supported.

The PNX9530; PNX9531; PNX9535 includes 2 identical AI modules. The pins available may however differ depending on the PNX9530; PNX9531; PNX9535 configuration being used.

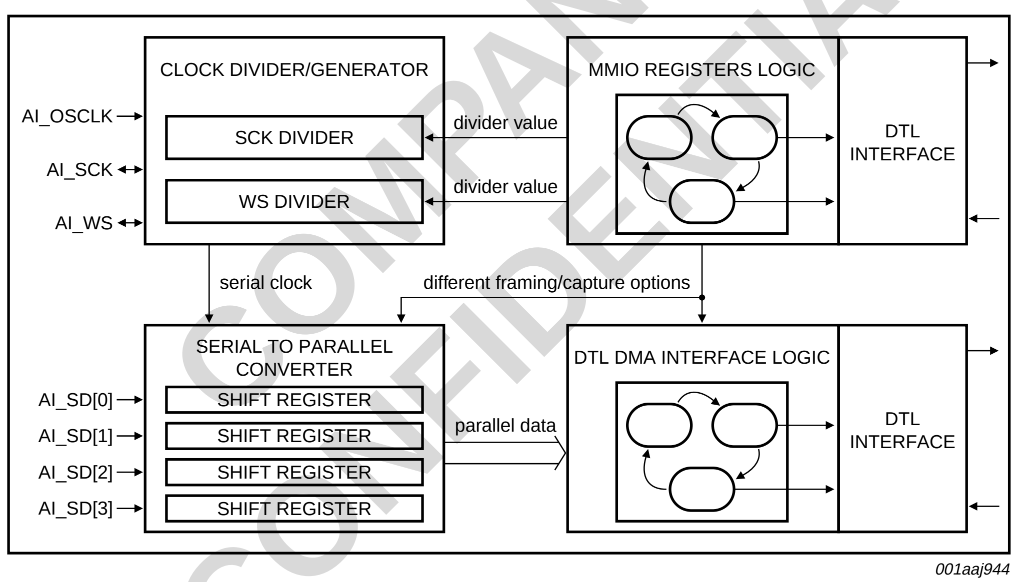


Fig 6. Audio in block diagram

7.2.2 Audio output

The PNX9530; PNX9531; PNX9535 device has an Audio Output (AO) module providing a DMA-driven serial interface designed to support stereo audio Digital-to-Analog Converters (DAC). The AO module can support up to eight PCM audio channels by driving up to four external stereo DACs. The AO module provides a direct connection interface to high-quality, low-cost oversampling DACs. A precise programmable oversampling clock is featured.

The AO module has four major subsystems: a programmable sample clock generator, a DMA engine, a parallel to serial converter and memory mapped registers for configuration and control. The AO connectors provide the digital audio stream, clock and control signals to external D/A converters. A block diagram of AO is illustrated in Figure 7.

The AO module, along with the external DACs, has the following capabilities:

- Up to 8 channels of audio output
- 16-bit or 32-bit samples per channel
- Programmable 1 Hz to 192 kHz sampling rate

  Remark: This is a practical range; the actual sample rate is application dependent
- Internal or external bit clock source
- Autonomously retrieves processed audio data from dual DMA buffers in memory
- 16-bit mono and stereo PC standard memory data formats
- Control capability for highly integrated PC codecs.

Remark: AC-97 codecs are not supported.

The DMA engine reads 16-bit or 32-bit samples from memory using dual DMA buffers in memory. Software initially assigns two full sample buffers in memory containing an integral number of samples for all active channels. The DMA engine retrieves samples from the first buffer in memory until exhausted and continues from the second buffer in memory as a request for a new first sample buffer in memory is issued to the system controller. This is a continuous process.

The samples are given to the data serializer (parallel-to-serial converter), which sends them out in a MSB first or LSB first serial frame format that can also contain one or two codec control words of up to 16 bits. The output frame structure is programmable.

PNX9530; PNX9531; PNX9535 includes 2 identical AO modules. The pins available may however differ depending on the PNX9530; PNX9531; PNX9535 configuration being used.

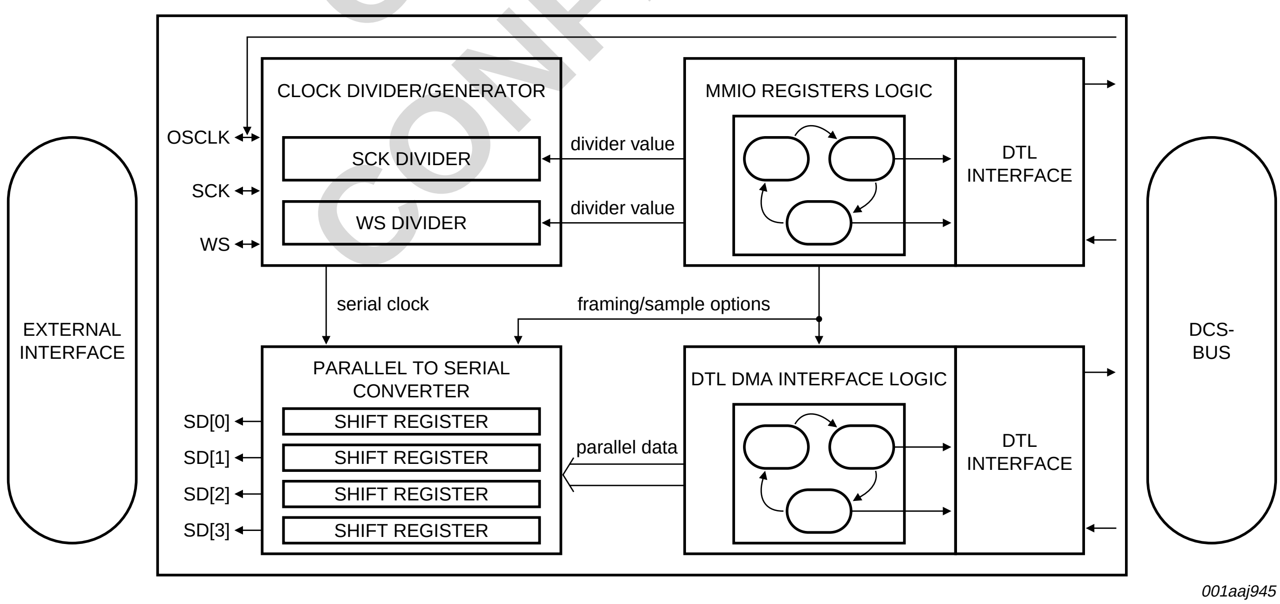


Fig 7. AO block diagram

7.3 Peripheral interfaces

7.3.1 DDR SDRAM memory interface

The PNX9530; PNX9531; PNX9535 has a DDR controller which is used to interface to off-chip DDR2 memory devices.

Remark: The DDR interface is capable to operate DDR1 memories also, but this function will not be guaranteed

The primary features of the DDR SDRAM controller include:

- 16-bit or 32-bit wide data bus on DDR SDRAM memory side
- Three MTL ports (one for the DMA memory traffic, two for the CPU)
- Supports × 8 and × 16, 4 and 8 banks memory devices
- Supports up to 2 Gb DDR SDRAM memory devices
- Supports 1 rank (physical banks) of memory devices
- Maximum of 8 open pages for a maximum address range of 256 MB
- Halt modes and clock gating for power consumption reduction
- Programmable DDR SDRAM timing parameters that support different DDR SDRAM memory devices up to 266 MHz, i.e. 533 MHz data rate
- Programmable bank mapping scheme to potentially improve bandwidth utilization
- Programmable arbitration with latency or deadline guarantees with built-in performance monitors
- JEDEC compliant limited to burst length of 8.

The DDR controller module includes an arbiter which arbitrates between the DDR burst commands coming from the three different MTL ports. After arbitration, the DDR burst command selected by the arbiter is stored in a FIFO with 5 entries. The DDR module has a refresh counter to keep track of the refresh timing. The DDR module keeps track of the open pages in the DDR memories. The DDR command generator decides upon which command (refresh, precharge, activate, read or write) to generate based on the information in the FIFO with 5 entries, the state of the refresh counter, and the state of the DDR memories as indicated by the open page table.

7.3.2 Multifunctional GPIO interface

The PNX9530; PNX9531; PNX9535 has a 61-bit wide GPIO interface, which multiplexes various functions.

7.3.2.1 GPIO

The PNX9530; PNX9531; PNX9535 has 61 pins that are capable of operating as software controlled General Purpose Input Output (GPIO) pins. Eight of them are dedicated GPIO pins. The other 53 pins are assigned to the other PNX9530; PNX9531; PNX9535 modules, like the AO module, but they can be re-used as GPIO pins, see Section 8.1. So these are designated as optional GPIO pins that can either operate in regular mode or in GPIO mode. All 61 pins have common features:

- Software I/O, which sets a pin or pin group, enables a pin or a pin group and inspects pin values
- Precise timestamping of internal and external events (up to 12 signals simultaneously)
- Signal event sequence monitoring or signal generation (up to 4 signals simultaneously)
- Timer source selection for TM3282.

The 61 pins have the same GPIO capabilities. However some of the dedicated GPIO pins have additional features like:

- Clocks: these pins are possible clock source for pattern generation or sampling mode or they are simply used to provide a clock to peripherals on the PNX9530; PNX9531; PNX9535 system board
- Wake-up event: used to wake-up PNX9530; PNX9531; PNX9535 from deep-sleep mode
- Boot option: determines the boot settings of PNX9530; PNX9531; PNX9535
- Watchdog: this is a subset of the software I/O mode since the TM3282 CPU would toggle this pin at regular intervals in order to prevent an external watchdog to reset the entire system; alternately the internal watchdog timer of PNX9530; PNX9531; PNX9535 system can be used.

After a PNX9530; PNX9531; PNX9535 system reset has occured all the GPIO pins are set to GPIO mode and in input mode (3-state).

A simplified block diagram of the GPIO module can be found in Figure 8. It presents the major interfaces of the GPIO module:

- The GPIO pins
- The MTL interface used to fetch data when operating in pattern generation mode or used to store data when the GPIO module is used in sampling mode.; in both cases up to 4 FIFO memory buffers are available for one of the modes
- The DCS-bus interface used to convey the MMIO register read and writes issued by the TM3282 CPU or any other master connected to PNX9530; PNX9531; PNX9535 through the PCI-bus interface
- The 5 interrupt lines which are routed directly to the TM3282 CPU; 4 lines are associated with the signal monitoring while the last interrupt line is linked to the event monitoring.

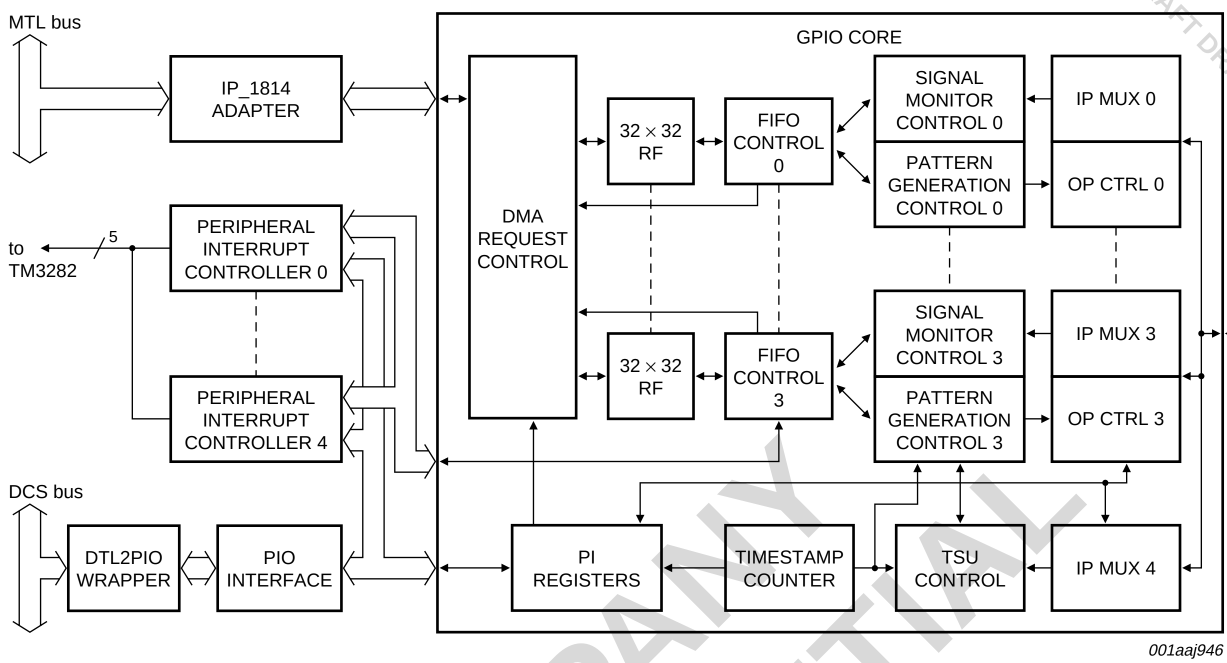


Fig 8. GPIO module block diagram

7.3.2.2 PCI-bus and XIO interface

The arbiter can control up to three external PCI masters, when the host interface is not used (see Table 19).

The XIO interface accepts up to five chip select signals and up to 16 data pins, when the host interface is not used (see Table 19).

For a full featured list of all PCI 2.2 configurations please contact NXP; see Section 22.

7.3.2.3 PCI-bus interface

PNX9530; PNX9531; PNX9535 includes a PCI-bus interface for easy integration into personal computer applications (where the PCI-bus is the standard for high-speed peripherals). In embedded applications the PCI-bus can interface to peripheral devices that implement functions not provided by the on-chip modules or to connected several CPUs together.

The PCI-XIO module supports 33 MHz and 66 MHz according to *PCI specification version 2.2*. It can operate as a configuration manager or it can also act as a target to external configuration cycles when an external processor and north bridge are used in the system.

Features:

- Three base addresses, i.e. apertures, are supported: DRAM, MMIO and XIO
- Option to enable internal PCI system arbiter which can support up to three external PCI masters
- As a PCI master, it can generate all non-reserved types of single transaction PCI cycles: I/O, memory, interrupt acknowledge and configuration cycle

- Linear burst mode is supported on memory transactions; other burst mode transfers are terminated after a single data transfer
- A DMA engine provides high-speed transfer to and from SDRAM and an external PCI device; the DMA can also be used to transfer data to and from XIO devices
- The PCI clock (at pin PCI_SYS_CLK) and PCI_RST_N (at pin RESET_IN_N) are generated externally and input to this module
- In PCI terminology it is a single function device.

The following general PCI-bus features are not implemented in the PCI-XIO module:

- As a PCI target, the device only responds to memory and configuration cycles
- Subtractive decoding is not supported
- There is no hard-coded legacy decoding of address space (such as VGA I/O and memory)
- Burst to configuration space is not supported.

The main function of the PCI-bus interface is to connect the PNX9530; PNX9531; PNX9535 on-chip MTL bus (and therefore its main memory) and its internal registers to external devices on the PCI-bus. A bus cycle on PCI that targets an address mapped into PNX9530; PNX9531; PNX9535 memory space will cause the PCI-bus interface to create a MTL bus cycle targeted at DRAM. From PNX9530; PNX9531; PNX9535, only the TM3282 CPU can cause the PCI-bus interface to create PCI-bus cycles; the other on-chip modules cannot access external hardware through the PCI-bus interface. From PCI, DRAM and most of the registers in MMIO space can be accessed by external PCI initiators.

The PCI-bus interface implements DMA (also called block or burst transfers) and non-DMA transfers. DMA transfers are interruptible on 64-byte boundaries.

The following classes of operations invoked by PNX9530; PNX9531; PNX9535 cause the PCI-bus interface to act as a PCI initiator:

- Transparent, single-word (or smaller) transactions caused by TM3282 loads and stores to one of the two available the PCI-bus address aperture, PCI1 and PCI2 ???
- Explicitly programmed single-word I/O or configuration read or write transactions
- Explicitly programmed multi-word DMA transactions.

The PNX9530; PNX9531; PNX9535 PCI-bus interface responds as a target to external initiators for a limited set of PCI transaction types:

- Configuration R/W
- Memory R/W, read line, and read multiple to the PNX9530; PNX9531; PNX9535 DRAM or MMIO apertures.

PNX9530; PNX9531; PNX9535 ignores PCI transactions other than the above.

The PCI-XIO module also includes an XIO interface. Both interfaces don’t execute simultaneously, see Table 19. The XIO interface uses PCI cycle to run XIO transfers before giving control back to PCI-bus. The XIO interface supports IDE, NAND and NOR

type Flash and Motorola devices, in an 8-bit or 16-bit wide datapath. Maximum NAND FLASH supported per profile is 128 MB. Maximum NOR FLASH supported per profile is 128 MB. PCI-XIO supports up to 5 profiles.

7.3.2.4 USB-bus interface

An USB-bus interface on dedicated I/O pins have been implemented in the PNX9530; PNX9531; PNX9535 fulfilling the *USB 2.0 HS OTG specification*. USB 2.0 offers the user a larger bandwidth increasing data throughput by a factor of 40 compared to USB 1.1. All the peripherals used with the previous versions of USB work perfectly with USB 2.0 while also offering a larger choice of higher performance peripherals, such as video cameras, fast storages devices, GPS receiver, etc. In addition to the 1.5 Mb/s and 12 Mb/s data rates of USB 1.1, the evolution from USB 1.1 to USB 2.0 adds an additional data rate of 480 MB/s.

Additionaly the PNX9530; PNX9531; PNX9535 provides the OTG functionality of USB 2.0. The On-The-Go (OTG) supplement to the USB Specification extends USB to peer-to-peer application. Using USB OTG technology the PNX9530; PNX9531; PNX9535 can be directly connected to a storeage device or host to exchange data. The OTG state machines determine the role of the device based on connector signals, and then initializes the device in the appropriate mode of operation (host or peripheral) based on how it is connected. After connecting the devices can negotiate using the OTG protocols to assume the role of host or peripheral based on the task to be accomplished.

The USB-bus interface supports the USB 2.0 HS OTG standard. It has two optional LED pins at pins USB_LED[1:0]. For availability and restrictions see Table 19.

7.3.2.5 Host interface

Parts of the multiplexed GPIO interface can operate as the host interface. For effect on other PNX9530; PNX9531; PNX9535 features see Table 19.

The PNX9530; PNX9531; PNX9535 provides a high-speed interface for I^2C-bus communication with a host processor to exchange data as well as command messages. Two separated channels are implemented to ease the software development by providing separated data buffers in the PNX9530; PNX9531; PNX9535 for data and command messages. The command message structure can be defined freely by the user to adapt the PNX9530; PNX9531; PNX9535 to the target system. The data/command buffer sizes can be defined independent of each other from 16 byte to several kB or MB depending on the available main memmory space. The host interface can be used in transaction modes with a data width of 16-bit or 8-bit by providing data transfer rates of up to 400 Mb/s (16-bit mode) or 200 Mb/s (8-bit mode).

7.3.3 I^2C-bus interface

The PNX9530; PNX9531; PNX9535 has a 5 V tolerant standard I^2C-bus interface, which can work as slave or master on the bus configurable during run time. The PNX9530; PNX9531; PNX9535 can load the boot code via an external connected I^2C EEPROM after reset and switch into slave mode if an external master requests the I^2C-bus. The interface can run on 100 kHz as well as on 400 kHz.

7.3.4 JTAG interface

The PNX9530; PNX9531; PNX9535 has a dedicated JTAG interface for software development.

8. Application design-in information

8.1 Multiplexed GPIO functionality

The PNX9530; PNX9531; PNX9535 has a versatile, software programmable GPIO interface for enhanced video and multimedia functionality. Applications can use the GPIO interface for general purpose input and output. Table 19 lists extended functionality from the GPIO interface for:

- Digital video input functions
- Digital video output functions
- Digital audio functions
- Extended I/O functions
- Host interface functions
- PCI-bus functions extension
- USB-bus functions extension
- Clock signals
- Generic signals.

Remark: The PNX9530; PNX9531; PNX9535 uses the GPIOs in boot mode. After finishing the boot process the GPIOs are available for the multiplexed functions (see Table 19).

Remark: Please note that these multiplexed functions are mutually exclusive, i.e. they may not be available at the same time depending on the software enabled configuration of the PNX9530; PNX9531; PNX9535.

Remark: For default configuration of GPIO pins and functionality see Table 20.

Table 19. Multiplexed GPIO functionality[1]

GPIO pin	Interfaces with mutually exclusive functionality								
	Video input	Video output	Extended I/O	Host	PCI	USB	Audio[2]	Clocks	Generic
GPIO0	-	-	-	-	-	-	-	CLOCK0	BOOT_MODE0
GPIO1	-	-	-	-	-	-	-	CLOCK1	BOOT_MODE1
GPIO2	-	-	-	-	-	-	-	CLOCK2	BOOT_MODE2
GPIO3	-	-	-	-	-	-	-	CLOCK3	BOOT_MODE3
GPIO4	-	-	-	-	-	-	-	CLOCK4	BOOT_MODE4
GPIO5	-	-	-	-	-	-	-	CLOCK5	-
GPIO6	-	-	-	-	-	-	-	CLOCK6	-
GPIO7	-	-	-	-	-	-	-	-	WAKEUP
GPIO8	-	-	XIO_SEL4	HOSTIF_CLE	-	-	-	-	-
GPIO9	-	-	-	-	-	-	AI2_OSCLK	-	-
GPIO10	-	VDO_D47	-	-	-	-	AO2_SD3/AO2_WS	-	-
GPIO11	-	VDO_D46	-	-	-	-	AO2_SD2/AO2_BCK	-	-
GPIO12	-	VDO_D45	-	-	-	-	AO2_SD1/AO2_OSCLK	-	-
GPIO13	-	VDO_D44	-	-	-	-	AO2_SD0	-	-
GPIO14	VDI_HOR	-	-	-	-	-	-	-	-
GPIO15	VDI_VER	-	-	-	-	-	-	-	-
GPIO16	-	-	XIO_SEL3	HOSTIF_INT_N	-	-	-	-	-
GPIO17	VDI_V0	-	-	HOSTIF_RESET_N	-	USB_LED0	-	-	-
GPIO18	-	-	-	-	PCI_REQ_N	-	-	-	-
GPIO19	-	-	XIO_D15	HOSTIF_D15	-	-	-	-	-
GPIO20	-	-	XIO_D14	HOSTIF_D14	-	-	-	-	-
GPIO21	-	-	XIO_D13	HOSTIF_D13	-	-	-	-	-
GPIO22	-	-	XIO_D12	HOSTIF_D12	-	-	-	-	-
GPIO23	-	-	XIO_D11	HOSTIF_D11	-	-	-	-	-
GPIO24	-	-	XIO_D10	HOSTIF_D10	-	-	-	-	-
GPIO25	-	-	XIO_D9	HOSTIF_D9	-	-	-	-	-
GPIO26	-	-	XIO_D8	HOSTIF_D8	-	-	-	-	-

Table 19. Multiplexed GPIO functionality[1] *…continued*

GPIO pin	Interfaces with mutually exclusive functionality								
	Video input	**Video output**	**Extended I/O**	**Host**	**PCI**	**USB**	**Audio[2]**	**Clocks**	**Generic**
GPIO27	VDI_D23	VDO_D43	-	HOSTIF_D7	-	-	AO2_WS	-	-
GPIO28	VDI_D22	VDO_D42	-	HOSTIF_D6	-	-	AO2_BCK	-	-
GPIO29	VDI_D21	VDO_D41	-	HOSTIF_D5	-	-	AI2_SD3	-	-
GPIO30	VDI_D20	VDO_D40	-	HOSTIF_D4	-	-	AI2_SD2	-	-
GPIO31	VDI_D19	VDO_D39	-	HOSTIF_D3	-	-	AI2_SD1	-	-
GPIO32	VDI_D18	VDO_D38	-	HOSTIF_D2	-	-	AI2_SD0	-	-
GPIO33	VDI_D17	VDO_D37	-	HOSTIF_D1	-	-	AI2_WS	-	-
GPIO34	VDI_D16	VDO_D36	-	HOSTIF_D0	-	-	AI2_BCK	-	-
GPIO35	-	-	-	HOSTIF_RD_OE_N	PCI_GNT_B_N	-	-	-	-
GPIO36	-	-	-	HOSTIF_WR_N	PCI_GNT_A_N	-	-	-	-
GPIO37	-	-	-	HOSTIF_CS_N	PCI_REQ_A_N	-	-	-	-
GPIO38	VDI_V2	-	-	-	-	-	-	-	-
GPIO39	VDI_V1	-	-	-	-	USB_LED1	-	-	-
GPIO40	-	-	-	-	-	-	AI1_SD3/AI2_BCK	-	-
GPIO41	-	-	-	-	-	-	AI1_SD2/AI2_WS	-	-
GPIO42	-	-	-	-	-	-	AI1_SD1/AI2_SD0	-	-
GPIO43	-	-	-	-	-	-	AI1_SD0	-	-
GPIO44	-	-	-	-	-	-	AI1_WS	-	-
GPIO45	-	-	-	-	-	-	AI1_BCK	-	-
GPIO46	-	-	-	-	-	-	AI12_OSCLK	-	-
GPIO47	-	-	-	-	-	USB_VBUS_FLT	-	-	-
GPIO48	-	-	-	-	-	USB_VBUS_PWE	-	-	-
GPIO49	-	-	-	-	-	-	AO1_SD3	-	-
GPIO50	-	-	-	-	-	-	AO1_SD2	-	-
GPIO51	-	-	-	-	-	-	AO1_SD1	-	-
GPIO52	-	-	-	-	-	-	AO1_SD0	-	-

Table 19. Multiplexed GPIO functionality[1] *…continued*

GPIO pin	Interfaces with mutually exclusive functionality								
	Video input	Video output	Extended I/O	Host	PCI	USB	Audio[2]	Clocks	Generic
GPIO53	-	-	XIO_SEL2	-	-	-	-	-	-
GPIO54	-	-	XIO_SEL1	-	-	-	-	-	-
GPIO55	-	-	XIO_SEL0	-	-	-	-	-	-
GPIO56	-	-	XIO_ACK	-	-	-	-	-	-
GPIO57	-	-	XIO_AD26	-	-	-	-	-	-
GPIO58	-	-	XIO_AD25	-	-	-	-	-	-
GPIO59	-	-	-	-	PCI_REQ_B_N	-	-	-	-
GPIO60	-	-	-	-	PCI_GNT_N	-	-	-	-

[1] See running text of this section for the boot process. For default configuration of GPIO pins and functionality see Table 20.

[2] Additional flexible configuration is possible through dedicated register settings for the audio interface.

Table 20. Default configuration

Default configuration		Default configuration		Default configuration		Default configuration	
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
GPIO0	GPIO0	GPIO16	XIO_SEL3	GPIO32	VDI_D18	GPIO48	USB_VBUS_PWE
GPIO1	GPIO1	GPIO17	VDI_V0	GPIO33	VDI_D17	GPIO49	AO1_SD3
GPIO2	GPIO2	GPIO18	PCI_REQ_N	GPIO34	VDI_D16	GPIO50	AO1_SD2
GPIO3	GPIO3	GPIO19	XIO_D15	GPIO35	PCI_GNT_B_N	GPIO51	AO1_SD1
GPIO4	GPIO4	GPIO20	XIO_D14	GPIO36	PCI_GNT_A_N	GPIO52	AO1_SD0
GPIO5	GPIO5	GPIO21	XIO_D13	GPIO37	PCI_REQ_A_N	GPIO53	XIO_SEL2
GPIO6	GPIO6	GPIO22	XIO_D12	GPIO38	VDI_V2	GPIO54	XIO_SEL1
GPIO7	GPIO7	GPIO23	XIO_D11	GPIO39	VDI_V1	GPIO55	XIO_SEL0
GPIO8	XIO_SEL4	GPIO24	XIO_D10	GPIO40	AI1_SD3	GPIO56	XIO_ACK
GPIO9	AI2_OSCLK	GPIO25	XIO_D9	GPIO41	AI1_SD2	GPIO57	XIO_AD26
GPIO10	AO2_SD3	GPIO26	XIO_D8	GPIO42	AI1_SD1	GPIO58	XIO_AD25
GPIO11	AO2_SD2	GPIO27	VDI_D23	GPIO43	AI1_SD0	GPIO59	PCI_REQ_B_N
GPIO12	AO2_SD1	GPIO28	VDI_D22	GPIO44	AI1_WS	GPIO60	PCI_GNT_N
GPIO13	AO2_SD0	GPIO29	VDI_D21	GPIO45	AI1_BCK	-	-
GPIO14	VDI_HOR	GPIO30	VDI_D20	GPIO46	AI1_OSCLK	-	-
GPIO15	VDI_VER	GPIO31	VDI_D19	GPIO47	USB_VBUS_FLT	-	-

8.2 Digital video input formats

The PNX9530; PNX9531; PNX9535 accepts several digital video input formats (see Table 22). For restrictions see Table 21.

Table 21. Restrictions on digital video input formats

Restriction on	Digital input formats (mutually exclusive options)[1]				
	2 × 8-bit		2 × 10-bit	8-bit and 8-bit	24-bit
	Dual *ITU656*, embedded sync	Dual *ITU656*, external and embedded sync	Dual *ITU656*, external sync	*ITU656*, embedded sync and TS	RGB
Maximum number of audio I/Os	8 in, 8 out	8 in, 8 out	4 in, 4 out	8 in, 8 out	4 in, 4 out
Host interface	available	available	cannot be used	available	cannot be used
Video output	no restrictions	no restrictions	restricted to 2 × 18-bit	no restrictions	restricted to 2 × 18-bit

[1] For further details on availability or conflicts see Table 19.

Table 22. Digital video input formats[1]

Input pin	Digital input formats (mutually exclusive options)				
	2 × 8-bit		2 × 10-bit	8-bit and 8-bit	24-bit
	Dual *ITU656*, embedded sync	Dual *ITU656*, external and embedded sync	Dual *ITU656*, external sync	*ITU656*, embedded sync and TS	RGB
VDI_CLK0	-	-	ITU2_CLK	-	-
VDI_CLK1	ITU2_CLK	ITU2_CLK	ITU1_CLK	ITU_CLK	-
VDI_CLK2	ITU1_CLK	ITU1_CLK	-	TS_CLK	-
VDI_V0	-	-	-	-	-
VDI_V1	-	-	-	-	-
VDI_V2	-	-	-	TS_VALID	CLK_IN
VDI_HOR	-	ITU1_HOR	ITU2_HOR	TS_START	HSYNC_IN
VDI_VER	-	ITU1_VER	ITU2_VER	TS_STOP	VSYNC_IN
VDI_D0	ITU1_D0	ITU1_D0	ITU1_HOR	TS_D0	R0
VDI_D1	ITU1_D1	ITU1_D1	ITU1_VER	TS_D1	B0
VDI_D2	ITU1_D2	ITU1_D2	-	TS_D2	G0
VDI_D3	ITU1_D3	ITU1_D3	-	TS_D3	R1
VDI_D4	ITU1_D4	ITU1_D4	ITU2_D0	TS_D4	B1
VDI_D5	ITU1_D5	ITU1_D5	ITU2_D1	TS_D5	G1
VDI_D6	ITU1_D6	ITU1_D6	ITU1_D0	TS_D6	R2
VDI_D7	ITU1_D7	ITU1_D7	ITU1_D1	TS_D7	B2
VDI_D8	ITU2_D0	ITU2_D0	ITU1_D2	ITU_D0	G2
VDI_D9	ITU2_D1	ITU2_D1	ITU1_D3	ITU_D1	R3
VDI_D10	ITU2_D2	ITU2_D2	ITU1_D4	ITU_D2	B3
VDI_D11	ITU2_D3	ITU2_D3	ITU1_D5	ITU_D3	G3
VDI_D12	ITU2_D4	ITU2_D4	ITU1_D6	ITU_D4	R4
VDI_D13	ITU2_D5	ITU2_D5	ITU1_D7	ITU_D5	B4
VDI_D14	ITU2_D6	ITU2_D6	ITU1_D8	ITU_D6	G4
VDI_D15	ITU2_D7	ITU2_D7	ITU1_D9	ITU_D7	R5
VDI_D16	-	-	ITU2_D2	-	B5
VDI_D17	-	-	ITU2_D3	-	G5
VDI_D18	-	-	ITU2_D4	-	R6
VDI_D19	-	-	ITU2_D5	-	B6
VDI_D20	-	-	ITU2_D6	-	G6
VDI_D21	-	-	ITU2_D7	-	R7
VDI_D22	-	-	ITU2_D8	-	B7
VDI_D23	-	-	ITU2_D9	-	G7

[1] For pinning see Table 7 and Table 19. For restrictions see Table 21.

9. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Analog supplies						
$V_{DDA(CAB)(1V2)}$	CAB analog supply voltage (1.2 V)			–0.5	+1.5	V
$V_{DDA(CAB)(3V3)}$	CAB analog supply voltage (3.3 V)			–0.5	+3.8	V
$V_{DDA(CAB/DDS)}$	CAB/DDS analog supply voltage			–0.5	+1.5	V
$V_{DDA(CGU/PLL)}$	CGU/PLL analog supply voltage			–0.5	+1.5	V
$V_{DDA(DDR/PLL)}$	DDR/PLL analog supply voltage			–0.5	+1.5	V
$V_{DDA(DLL0)}$	DLL0 analog supply voltage			–0.5	+1.5	V
$V_{DDA(DLL1)}$	DLL1 analog supply voltage			–0.5	+1.5	V
$V_{DDA(DLL2)}$	DLL2 analog supply voltage			–0.5	+1.5	V
$V_{DDA(OSC)}$	oscillator analog supply voltage			–0.5	+1.5	V
$V_{DDA(DRV)(USB)}$	USB driver analog supply voltage			–0.5	+4.0	V
$V_{DDA(FB)(1V2)}$	FB analog supply voltage (1.2 V)			–0.5	+1.5	V
$V_{DDA(USB)}$	USB analog supply voltage			–0.5	+4.0	V
Digital supplies						
$V_{DDD(C)}$	core digital supply voltage			–0.5	+1.5	V
$V_{DDD(IO)}$	I/O digital supply voltage			–0.5	+3.8	V
$V_{DDD(IO)(DDR)}$	DDR input/output digital supply voltage			–0.5	+3.0	V
$V_{DDD(IO)(PCI)}$	PCI input/output digital supply voltage			–0.5	+5.5	V
Temperature						
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
Input voltages						
V_I	input voltage	5 V tolerant inputs		–0.5	5.5	V
		3.3 V tolerant inputs; with $V_{DDD(IO)}$		–0.5	3.8	V
		1.8 V and 2.5 V tolerant inputs; with $V_{DDD(IO)(DDR)}$		–0.5	3.0	V
V_{ESD}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		machine model	[2]	-	±200	V
		charge device model	[3]			
		corner pins		-	±750	V
		all other pins		-	±500	V

[1] Class 2 according to *JEDEC JESD22-A114*.

[2] Class B according to *JEDEC JESD22-A115*.

[3] Class III following *JEDEC JESD22-C101*.

10. Thermal characteristics

Table 24. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1][2]	20	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample amount of copper area directly under the PNX9530; PNX9531; PNX9535 with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Do not use any solder-stop varnish under the chip. In addition the use of soldering glue with a high thermal conductance after curing is recommended.

[2] The customer PCB must be reviewed by NXP experts to check the thermal resistance of the system.

11. Static characteristics

Table 25. Characteristics (supply pins)

Operating conditions for minimum and maximum values in Table 26 to Table 34 hold for conditions given in Table 25 and T_{amb} = −40°C to T_{amb} =+85°C, unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog supplies						
$V_{DDA(CAB)(1V2)}$	CAB analog supply voltage (1.2 V)		1.16	1.20	1.24	V
$V_{DDA(CAB)(3V3)}$	CAB analog supply voltage (3.3 V)		3.15	3.30	3.45	V
$V_{DDA(CAB/DDS)}$	CAB/DDS analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(CGU/PLL)}$	CGU/PLL analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DDR/PLL)}$	DDR/PLL analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DLL0)}$	DLL0 analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DLL1)}$	DLL1 analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DLL2)}$	DLL2 analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(OSC)}$	oscillator analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DRV)(USB)}$	USB driver analog supply voltage		3.15	3.30	3.45	V
$V_{DDA(FB)(1V2)}$	FB analog supply voltage (1.2 V)		1.16	1.20	1.24	V
$V_{DDA(USB)}$	USB analog supply voltage		3.15	3.30	3.60	V
Digital supplies						
$V_{DDD(C)}$	core digital supply voltage		1.16	1.20	1.24	V
$V_{DDD(IO)}$	I/O digital supply voltage		3.15	3.30	3.45	V
$V_{DDD(IO)(DDR)}$	DDR input/output digital supply voltage	normal mode (DDR2)	1.70	1.80	1.90	V
		333 MHz to 400 MHz (DDR1)	2.40	2.55	2.70	V
$V_{DDD(IO)(PCI)}$	PCI input/output digital supply voltage	with 3.3 V supply	3.00	3.30	3.60	V
		with 5 V supply	4.75	5.00	5.25	V
Power dissipation						
P_{tot}	total power dissipation	for all supplies	-	2.07	-	W
		for $V_{DDD(C)}$	-	1.20	-	W
		for $V_{DDD(IO)(DDR)}$	-	0.54	-	W
		for $V_{DDD(IO)}$	-	0.33	-	W

Table 26. Characteristics (type P pins[1][2])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	5 V	$0.7 \times V_{DDD}$	-	5.3	V
		3.3 V	$0.7 \times V_{DDD}$		$V_{DDD} + 0.3$	
V_{IL}	LOW-level input voltage	5 V or 3.3 V	–0.3	-	$+0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD}$	V
t_f	fall time	between $0.2 \times V_{DDD}$ and $0.6 \times V_{DDD}$	1.3	-	-	ns
C_i	input capacitance		-	-	8	pF

[1] See Table 18.

[2] In this context V_{DDD} means $V_{DDD(IO)(PCI)}$.

Table 27. Characteristics (DDR1 (SSTL-2); all DDR SDRAM pins, besides pin MM_VREF)

All DDR1 values are expected, neither tested nor guaranteed..

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input buffers						
$V_{IH(DC)}$	DC HIGH-level input voltage	[1]	$V_{REF} + 0.15$	-	$V_{DD} + 0.30$	V
$V_{IL(DC)}$	DC LOW-level input voltage	[1]	–0.30	-	$V_{REF} - 0.15$	V
$V_{IH(AC)}$	AC HIGH-level input voltage	[1][2]	$V_{REF} + 0.31$	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	[1][2]	-	-	$V_{REF} - 0.31$	V
Output buffers						
V_{OH}	HIGH-level output voltage		$V_{DD} - 0.56$	-	-	V
V_{OL}	LOW-level output voltage		-	0.56	-	V
I_{OH}	HIGH-level output current		14	-	-	mA
I_{OL}	LOW-level output current		14	-	-	mA
Z_o	output impedance		28	-	39	Ω

[1] In this context V_{REF} denotes the reference voltage supplied through pin MM_VREF and V_{DD} denotes the supply voltage $V_{DDD(IO)(DDR)}$.

[2] These values are specified with respect to the supply voltage and not with respect to the input signal levels.

Table 28. Characteristics (DDR2 (SSTL-18); all DDR SDRAM pins, besides pin MM_VREF)

All values are valid within the operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input buffers						
$V_{IH(DC)}$	DC HIGH-level input voltage	[1]	$V_{REF} + 0.125$	-	$V_{DD} + 0.30$	V
$V_{IL(DC)}$	DC LOW-level input voltage	[1]	–0.30	-	$V_{REF} - 0.125$	V
$V_{IH(AC)}$	AC HIGH-level input voltage	[1][2]	$V_{REF} + 0.25$	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	[1][2]	-	-	$V_{REF} - 0.25$	V

Table 28. Characteristics (DDR2 (SSTL-18); all DDR SDRAM pins, besides pin MM_VREF) *...continued*

All values are valid within the operating conditions.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output buffers						
V_{OH}	HIGH-level output voltage		V_{DD} - 0.28	-	-	V
V_{OL}	LOW-level output voltage		-	0.28	-	V
I_{OH}	HIGH-level output current		6	-	-	mA
I_{OL}	LOW-level output current		6	-	-	mA
Z_o	output impedance		31	-	44	Ω

[1] In this context V_{REF} denotes the reference voltage supplied through pin MM_VREF and V_{DD} denotes the supply voltage $V_{DDD(IO)(DDR)}$.

[2] These values are specified with respect to the supply voltage and not with respect to the input signal levels.

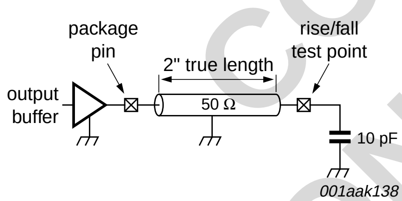


Fig 9. SSTL-2 and SSTL-18 test load conditions

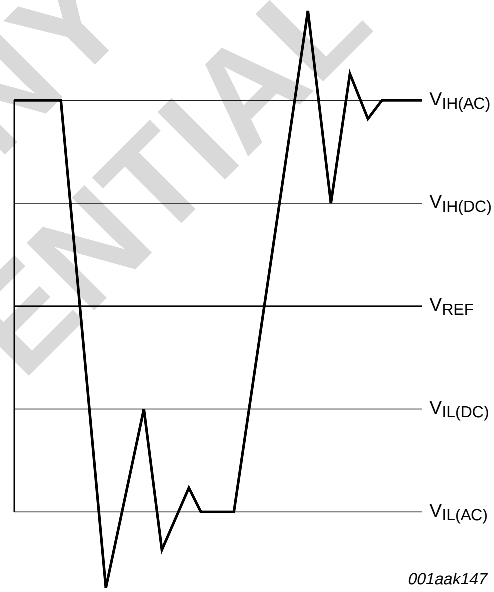


Fig 10. SSTL-2 and SSTL-18 receiver signal conditions

Table 29. Characteristics (type I2 pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.3	-	5.3	V
V_{IL}	LOW-level input voltage		–0.3	-	+1.0	V
V_{OL}	LOW-level output voltage		-	-	0.6	V
V_{hys}	hysteresis voltage		0.25	-	-	V
t_f	fall time	C_L = 10 pF to 400 pF	1.5	-	250	ns
C_i	input capacitance		-	-	6	pF

[1] See Table 18.

Table 30. Characteristics (type H pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD(IO)}$	-	$V_{DDD(IO)} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD(IO)}$	V
I_{OH}	HIGH-level output current	at $V_{OH} = V_{DDD(IO)} - 0.4$ V	16	-	-	mA
I_{OL}	LOW-level output current	at $V_{OL} = 0.4$ V	16	-	-	mA
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		0.5	-	1.0	ns
t_f	fall time		0.5	-	1.5	ns
C_i	input capacitance		-	-	3	pF
Z_o	output impedance		15	20	25	Ω

[1] See Table 18.

Table 31. Characteristics (type L pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD(IO)}$	-	$V_{DDD(IO)} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD(IO)}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD(IO)}$	-	-	V
I_{OH}	HIGH-level output current	at $V_{OH} = V_{DDD(IO)} - 0.4$ V	4.0	-	-	mA
I_{OL}	LOW-level output current	at $V_{OL} = 0.4$ V	4.0	-	-	mA
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		0.5	-	1.5	ns
t_f	fall time		0.5	-	1.8	ns
C_i	input capacitance		-	-	3.5	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 18.

Table 32. Characteristics (type F pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD(IO)}$	-	$V_{DDD(IO)} + 0.3$	V
V_{IL}	LOW-level input voltage		-0.3	-	$+0.3 \times V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD(IO)}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD(IO)}$	-	-	V
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		1	-	2	ns
t_f	fall time		1	-	2	ns
C_i	input capacitance		-	-	4	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 18.

Table 33. Characteristics (type S pins[1][2])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD}$	-	$V_{DDD} + 0.3$	V
V_{IL}	LOW-level input voltage		-0.3	-	$+0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD}$	-	-	V
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		2	-	4	ns
t_f	fall time		2	-	4	ns
C_i	input capacitance		-	-	4.5	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 18.

[2] In this context V_{DDD} means $V_{DDD(IO)(DDR)}$.^

Table 34. Characteristics (type T pins[1][2])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD}$	-	$V_{DDD} + 0.3$	V
V_{IL}	LOW-level input voltage		−0.3	-	$+0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD}$	-	-	V
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		2	-	4	ns
t_f	fall time		2	-	4	ns
C_i	input capacitance		-	-	4.5	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 18.

[2] In this context V_{DDD} means $V_{DDD(IO)(PCI)}$.

Table 35. Characteristics (type U pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog input (pin USB_VBUS)						
$V_{A\_SESS\_VLD}$	A-device session valid voltage		0.8	-	2	V
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	-	V
$V_{B\_SESS\_VLD}$	B-device session valid voltage		2	-	4	V
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V
Analog inputs and outputs (pins USB_DM and USB_DP)						
V_{CM}	differential common mode voltage range		800	-	2500	mV
V_{DI}	differential input sensitivity voltage		100	400	1100	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)		−50	+200	+500	mV

[1] See Table 18.

12. Dynamic characteristics

Table 36. Characteristics (DDR SDRAM memory interface)
Operating conditions for minimum and maximum values in Table 36 to Table 42 hold for conditions given in Table 25 and T_{amb} = +25°C, unless otherwise stated.
All DDR1 values are expected, neither tested nor guaranteed..

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock (pins MM_CLK_N and MM_CLK_P)						
f_{clk}	clock frequency	DDR2 mode	125	-	266	MHz
		DDR1 mode	83	-	200	MHz
t_{sk}	skew time	between MM_CLK_N and MM_CLK_P	–10	0	+10	ps
t_{PD}	propagation delay	on PCB	–240	0	+240	ps
Control and data						
t_{PD}	propagation delay	on PCB				
		pins MM_A[13:0], MM_CAS_N, MM_CKE, MM_CS_N, MM_RAS_N and MM_WE_N	–480	0	+480	ps
		pins MM_DS_N[3:0] and MM_DS_P[3:0]	–120	0	+120	ps
		pins MM_D[31:0] and MM_DM[3:0]	0	-	240	ps
Inputs						
t_r	rise time	DDR2 mode	80	-	120	ps
		DDR1 mode	40	-	120	ps
t_f	fall time	DDR2 mode	60	-	100	ps
		DDR1 mode	40	-	90	ps
Outputs						
t_r	rise time	DDR2 mode	136	217	380	ps
		DDR1 mode	99	131	247	ps
t_f	fall time	DDR2 mode	168	275	554	ps
		DDR1 mode	111	158	308	ps

Table 37. Characteristics (VDI interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency	pins VDI_CLK2 to VDI_CLK0		-	-	157	MHz
		pin VDI_D2, when used as *dv0_clkn*		-	-	108	MHz
		pin VDI_D3, when used as *dv1_clkn*		-	-	108	MHz
Control and data (pins VDI_CLK2 to VDI_CLK0, VDI_D[23:0], VDI_HOR and VDI_VER)							
$t_{su(i)}$	input set-up time		[1]	2	-	-	ns
$t_{h(i)}$	input hold time		[1]	2	-	-	ns

[1] The reference clock depends on the operating mode; see Figure 11.

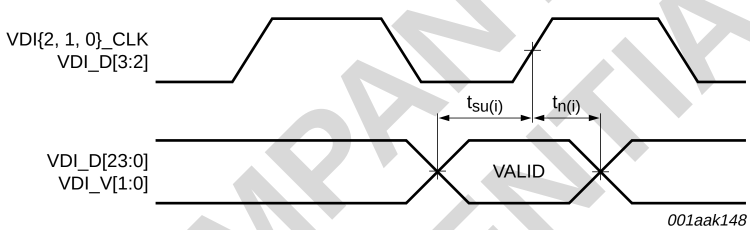


Fig 11. VDI interface timing

Table 38. Characteristics (VDO interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock (pin VDO_CLK)							
f_{clk}	clock frequency	VDO_MODE.QVCP_MODE = logic 1 and VDO_MODE.QVCP_DUAL_EDGE = logic 0	[1][2][3]	-	-	157	MHz
		VDO_MODE.QVCP_MODE = logic 1 and VDO_MODE.QVCP_DUAL_EDGE = logic 1	[1][3]	-	-	81	MHz
		VDO_MODE.VDO_BUFFER_MODE = logic 1	[1][3]	-	-	30	MHz

Table 38. Characteristics (VDO interface) *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Data, see Figure 12							
$t_{d(DV)}$	data valid delay time	QVCP block: VDO_CLK referenced to pins VDO[29:0], VDO_AUX1, VDO_HORand VDO_VER; VDO_MODE.QVCP_MODE = logic 1 ; VDO_CLK as input	[1]	3	-	9	ns
		Buffer: VDO_CLK referenced to pins VDO[47:0], VDO_AUX1, VDO_HOR and VDO_VER; VDO_MODE.VDO_BUFFER _MODE = logic 1	[1][3]	5	-	20	ns
$t_{d(QV)}$	data output valid delay time	QVCP block: VDO_CLK referenced to pins VDO[29:0], VDO_AUX1, VDO_HOR and VDO_VER; VDO_MODE.QVCP_MODE = logic 1 ; VDO_CLK as output	[1]	1.2	-	3.9	ns
$t_{su(i)}$	input set-up time	VDO_VER to VDO_CLK	[1][3]	3	-	-	ns
$t_{h(i)}$	input hold time	VDO_VER to VDO_CLK	[1][3]	2	-	-	ns

[1] VDO_MODE.QVCP_MODE and VDO_MODE.VDO_BUFFER_MODE are mutually exclusive.

[2] When pin VDO_CLK is set as an input, the AC timing of the remaining VDO pins may not allow to run at the maximum operating frequency.

[3] Data are the same for both input or output mode of pin VDO_CLK.

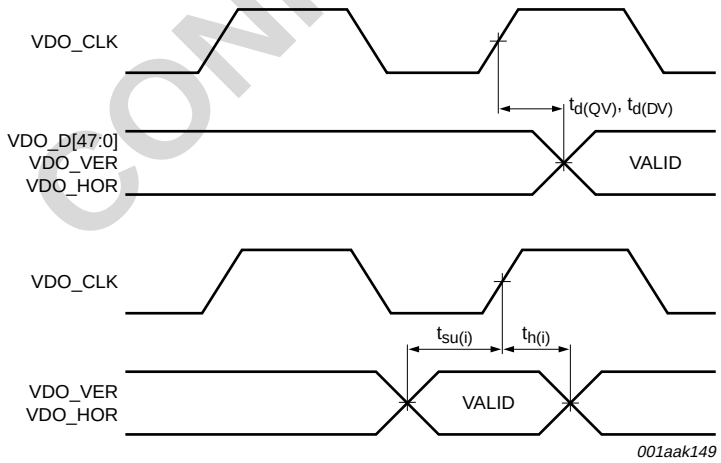


Fig 12. VDO interface timing

Table 39. Characteristics (digital audio input interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency	AI12_OSCLK and AI2_OSCLK		-	-	50	MHz
		AI1_BCK and AI2_BCK		-	-	27	MHz
Data, see Figure 13							
t_{PD}	propagation delay	AI1_BCK to AI1_WS; AI2_BCK to AI2_WS	[1]	4	-	12	ns
$t_{su(i)}$	input set-up time	AI1_SD[3:0], AI1_WS to AI1_BCK; AI2_SD[3:0], AI_WS2 to AI2_BCK	[1]	4	-	-	ns
$t_{h(i)}$	input hold time	AI1_SD[3:0], AI1_WS to AI1_BCK; AI2_SD[3:0], AI_WS2 to AI2_BCK	[1]	0	-	-	ns

[1] Data are the same for both input or output mode of pins AI1_BCK or AI2_BCK (master or slave). They hold for both rising or falling edge. For functional pins see Section 8.1.

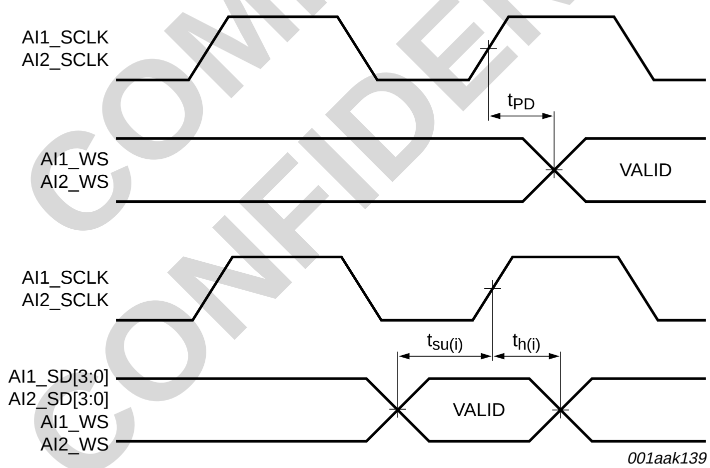


Fig 13. AI interface timing

Table 40. Characteristics (digital audio output interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency	AO12_OSCLK and AO2_OSCLK		-	-	50	MHz
		AO12_BCK and AO2_BCK		-	-	27	MHz
Data, see Figure 14							
t_{PD}	propagation delay	AO12_BCK to AO1_SD[3:0], AO2_SD[3:0], AO12_WS; AO2_BCK to AO2_SD[3:0], AO2_WS	[1]	4	-	12	ns
$t_{su(i)}$	input set-up time	AO12_WS to AO12_BCK; AO2_WS to AO2_BCK	[1]	4	-	-	ns
$t_{h(i)}$	input hold time	AO12_WS to AO12_BCK; AO2_WS to AO2_BCK	[1]	0	-	-	ns

[1] Data are the same for both input or output mode of pins AI1_BCK or AI2_BCK (master or slave). They hold for both rising or falling edge. For functional pins see Section 8.1.

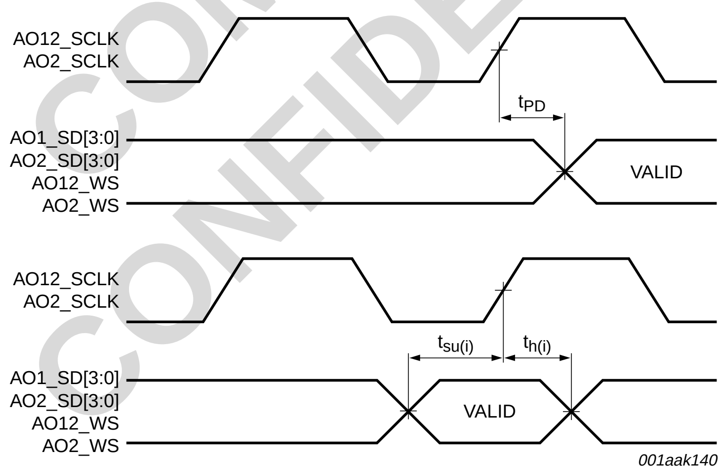


Fig 14. AO interface timing

Table 41. Characteristics (GPIO interface)[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency		[2]	-	-	108	MHz
Data, see Figure 15							
t_{PD}	propagation delay	CLOCK[6:0] to GPIO[7:0]	[3]	2	-	10	ns
		CLOCK[6:0] to GPIO[60:8]]	[3]	4		12	ns
$t_{su(i)}$	input set-up time	GPIO[7:0] to CLOCK[6:0]	[3]	2	-	-	ns
		GPIO[60:8] to CLOCK[6:0]	[3]	5		-	ns
$t_{h(i)}$	input hold time	GPIO[7:0] to CLOCK[6:0]	[3]	2	-	-	ns
		GPIO[60:8] to CLOCK[6:0]	[3]	4	-	-	ns

[1] See Table 19.

[2] The maximum operating frequency may be lower due to the wide variation of t_{PD}.

[3] Data are the same for both input or output mode of these pins. They hold for both rising or falling edge.. See table note in Table 10 for clock and data assignments.

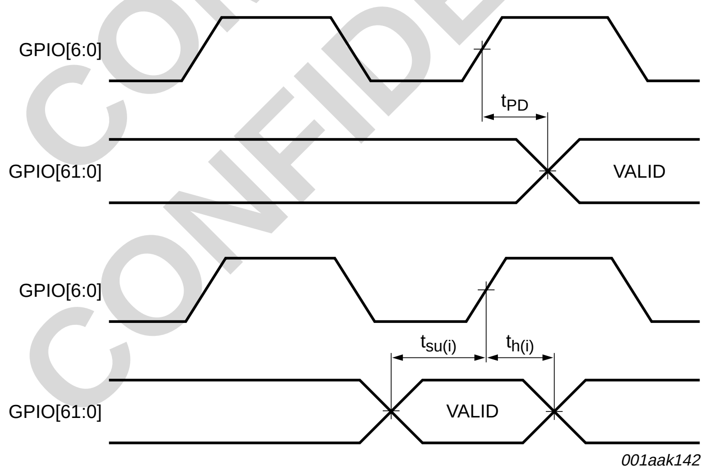


Fig 15. GPIO interface timing

Table 42. Characteristics (PCI-bus and XIO interface)[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock (pins PCI_CLK and PCI_SYS_CLK)							
T_{cy}	cycle time		[2]	15	-	-	ns
t_{high}	CLK high time			6	-	-	ns
t_{low}	CLK low time			6	-	-	ns
t_{val}	CLK to signal valid delay time - bused signals	pin PCI_CLK only	[3][4]	2	-	6	ns
$t_{val(ptp)}$	CLK to signal valid delay time - point-to-point	pin PCI_CLK only	[3][4]	2	-	6	ns
Data pins							
$t_{rst\text{-}off}$	reset active to output float delay time	pins RESET_IN_N and POR_IN_N		-	-	40	ns
t_{su}	input set-up time to CLK - bused signals	clock at pin PCI_CLK	[6][7]				
		PCI-bus		3	-	-	ns
		pins XIO_ACK and XIO_D[15:8]	[5]	9	-	-	ns
$t_{su(ptp)}$	input set-up time to CLK - point-to-point	clock at pin PCI_CLK		5	-	-	ns
t_h	input hold time from CLK	clock at pin PCI_CLK	[6][7]				
		PCI-bus		0	-	-	ns
		signals XIO_ACK and XIO_D[15:8]	[5]	0	-	-	ns
t_{on}	float to active delay time			2	-	-	ns
t_{off}	active to float delay time			-	-	14	ns
t_d	delay time	between pin PCI_CLK and pins XIO_AD[26:25], XIO_SEL[4:0] and XIO_D[15:8]	[5]	2	-	10	ns

[1] See Figure 17.

[2] PCI-bus and XIO interface.

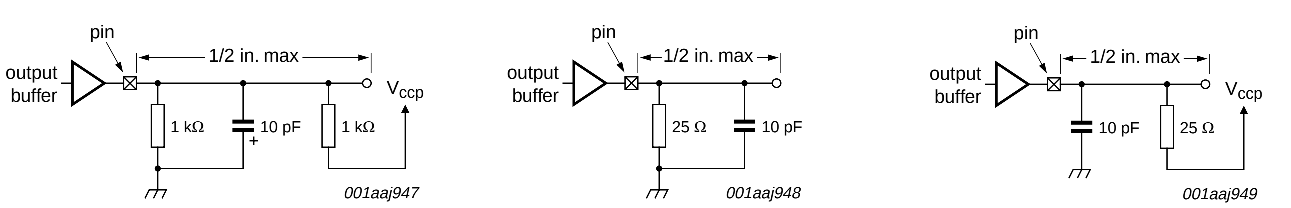
[3] Valid for all XIO signals from Table 19, besides XIO_ACK.

[4] See Figure 16 for measurement conditions of minimum and maximum values.

[5] See Table 19.

[6] 5 V signalling: V_{th} = 2.4 V, V_{tl} = 0.4 V and V_{max} = 2.0 V

[7] 3.3 V signalling: $V_{th} = 0.6 \times V_{DDD(IO)(PCI)}$, $V_{tl} = 0.2 \times V_{DDD(IO)(PCI)}$ and $V_{max} = 0.4 \times V_{DDD(IO)(PCI)}$



a. Slew rate b. Rising edge c. Falling edge

Fig 16. Type P cell test load conditions; see Table 18

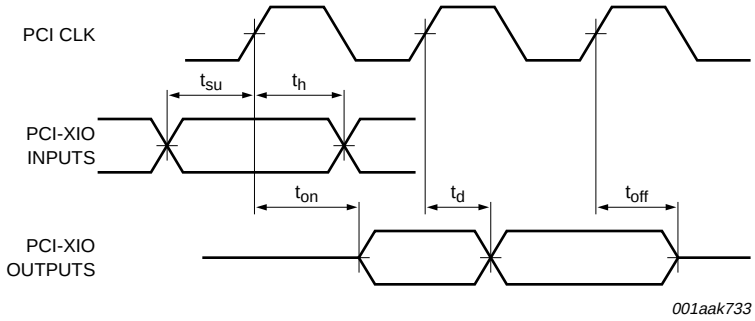


Fig 17. PCI-bus and XIO interface timing

Table 43. Characteristics (host interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T	period	access time, i.e. delay between two consecutive HOSTIF_CS_N falling edges	[1]	40	-	-	ns
$t_{su(W)}$	write set-up time	HOSTIF_D[15:0] and HOSTIF_CLE rising edge to rising edge of HOSTIF_WR_N and rising edge of HOSTIF_CS_N	[1]	10	-	-	ns
$t_{h(W)}$	write hold time	HOSTIF_D[15:0] and falling edge of HOSTIF_CLE to rising edge of HOSTIF_WR_N or rising edge of HOSTIF_CS_N	[1]	5	-	-	ns
$t_{d(WV)}$	write valid delay time	between a rising edge on HOSTIF_WR_N and a falling edge on HOSTIF_CS_N, i.e. delay between end of write and next access	[1]	10	-	-	ns
$t_{d(o)}$	output delay time	falling edge of HOSTIF_RD_OE_N and falling edge of HOSTIF_CS_N to HOSTIF_D[15:0	[2]	2.5	-	13	ns
$t_{h(o)}$	output hold time	rising edge of HOSTIF_RD_OE_N and rising edge of HOSTIF_CS_N to HOSTIF_D[15:0]	[2]	2.5	-	13	ns

[1] HOSTIF_RD_OE_N is constant logic 1 during a write command; see Figure 18.

[2] HOSTIF_WR_N is a constant logic 1 and HOSTIF_CLE is a constant logic 0 during read command.

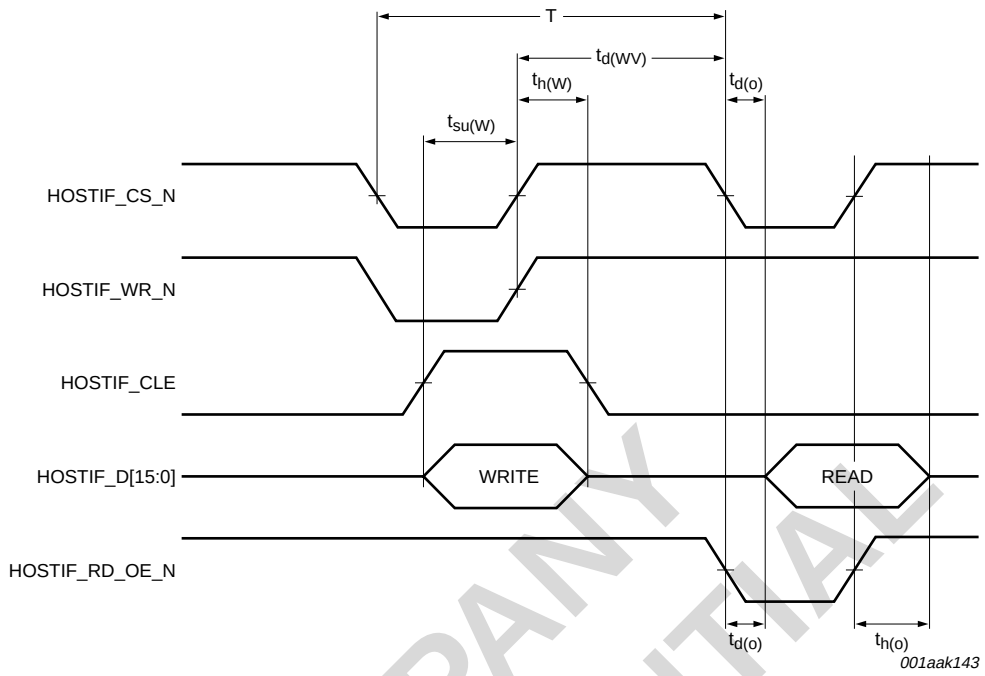


Fig 18. Host interface timing

Table 44. Characteristics (reset interface[1][2], see Figure 19)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{por}	reset active time after power stable	pin POR_IN_N	1	-	-	ms
t_{rst}	reset time	pin RESET_IN_N	100	-	-	µs

[1] POR_IN_N and RESET_IN_N are asynchronous signals.

[2] At power-up only POR_IN_N is required to be asserted. RESET_IN_N can be used as warm reset and left unconnected if not used as warm reset. Note that the JTAG state machines do not get reset when only RESET_IN_N is being asserted low.

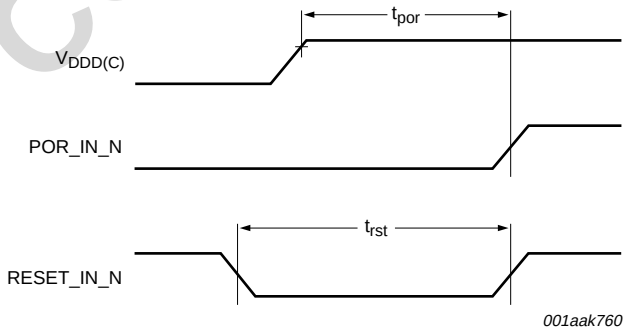


Fig 19. Reset interface timing

Table 45. Characteristics (I^2C-bus interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
f_{clk}	clock frequency		-	-	400	kHz
Data						
t_{BUF}	bus free time between a STOP and START condition		1	-	-	µs
t_{LOW}	LOW period of the SCL clock		1	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		1	-	-	µs
t_f	fall time of both SCL and SDA signals	C_b = 10 pF to 400 pF, from V_{IH} to V_{IL}	$20 + 0.1 \times C_b$	-	250	ns
$t_{SU; STA}$	set-up time for a repeated START condition		1	-	-	µs
$t_{HD; STA}$	hold time (repeated) START condition		1	-	-	µs
$t_{SU; DAT}$	data set-up time		100	-	-	ns
$t_{HD; DAT}$	data hold time		0	-	-	ns
$t_{VD; DAT}$	data valid time	LOW to data out valid	-	-	0.5	µs
		HIGH to data out	1	-	-	ns

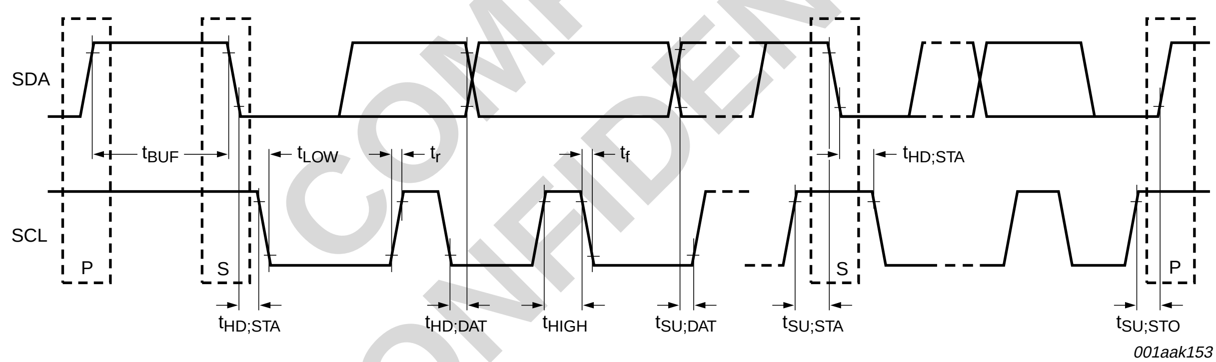


Fig 20. I^2C-bus interface timing

Table 46. Characteristics (JTAG interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
f_{clk}	clock frequency	boundary scan	-	-	25	MHz
		operating frequency	-	-	50	MHz
Data, see Figure 21						
t_{PD}	propagation delay		0	-	5	ns
$t_{su(i)}$	input set-up time		5	-	-	ns
$t_{h(i)}$	input hold time		3	-	-	ns

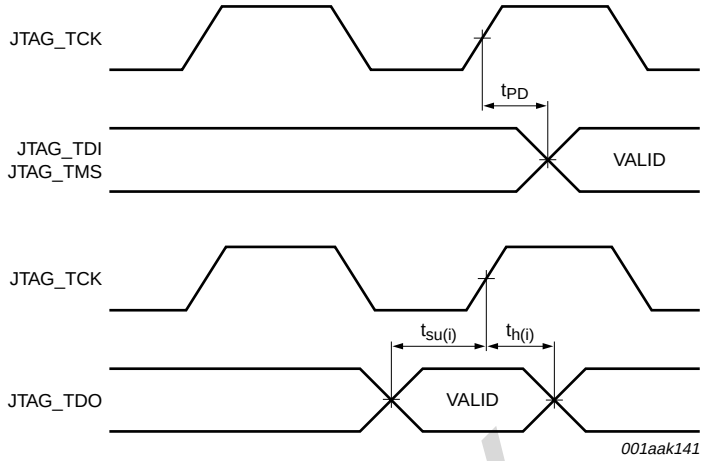


Fig 21. JTAG interface timing

13. External crystal

13.1 With external crystal HC-49U

Table 47. Characteristics (external crystal HC-49U, pin XTAL_I)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	fundamental mode	-	27.000	-	MHz
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	with temperature	-	±30	-	10^{-6}
T_{amb}	ambient temperature		–40	-	+85	°C
C_{ext}	external capacitance		-	-	18	pF
C_L	load capacitance		-	18	-	pF
C_{shunt}	shunt capacitance		-	-	7	pF
R_{ESR}	equivalent series resistance		-	-	130	Ω
P_{drive}	drive power		-	-	1	mW

13.2 In oscillator mode

Table 48. Characteristics (in oscillator mode, pin XTAL_I)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta f_{xtal}/f_{xtal}$	relative crystal frequency variation	with temperature	-	±30	-	10^{-6}
δ	duty cycle		45	-	55	%
T_{amb}	ambient temperature		–40	-	+85	°C
C_{shunt}	shunt capacitance		-	-	7	pF

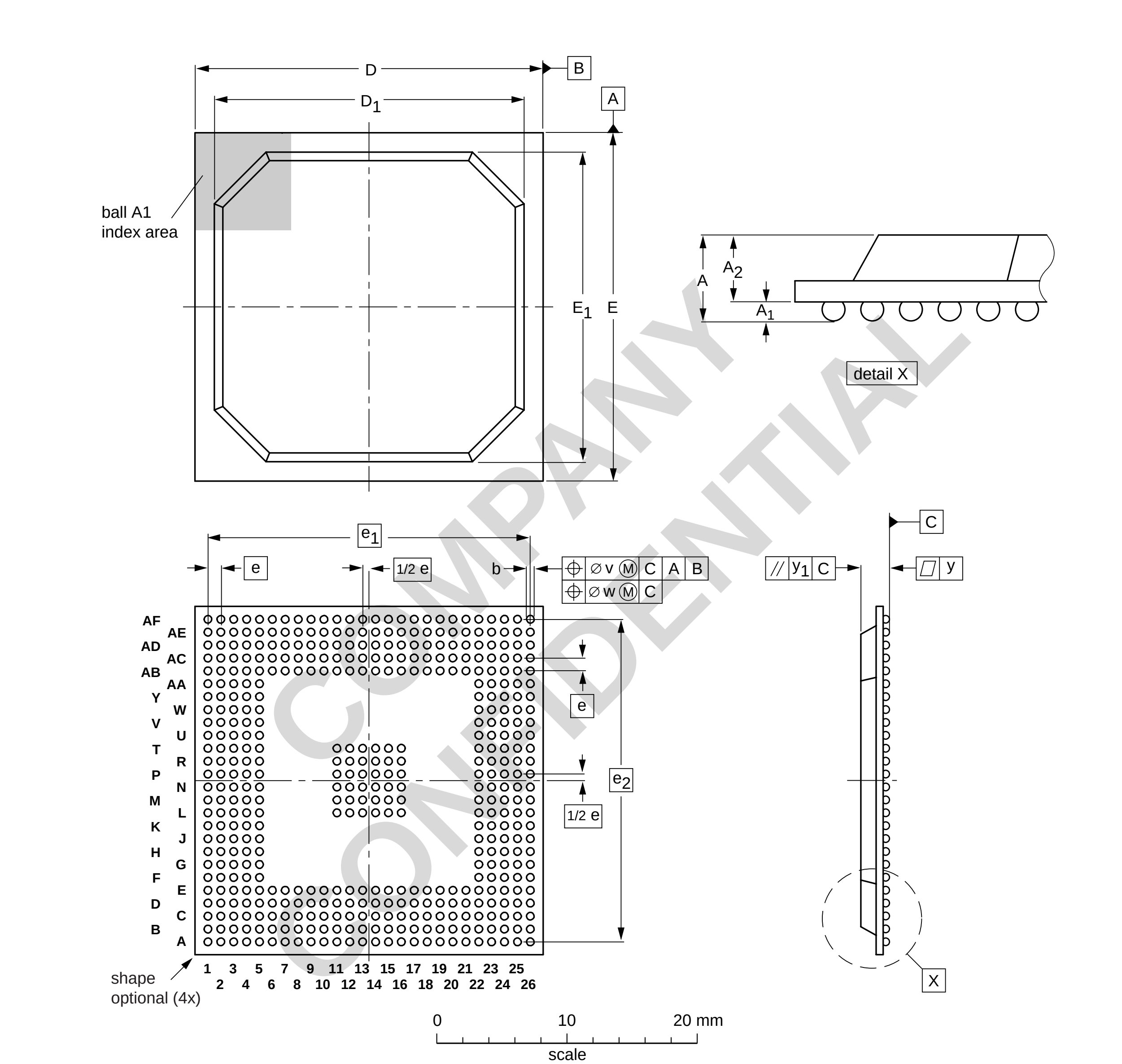
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

BGA456: plastic ball grid array package; 456 balls; body 27 x 27 x 1.75 mm **SOT795-1**



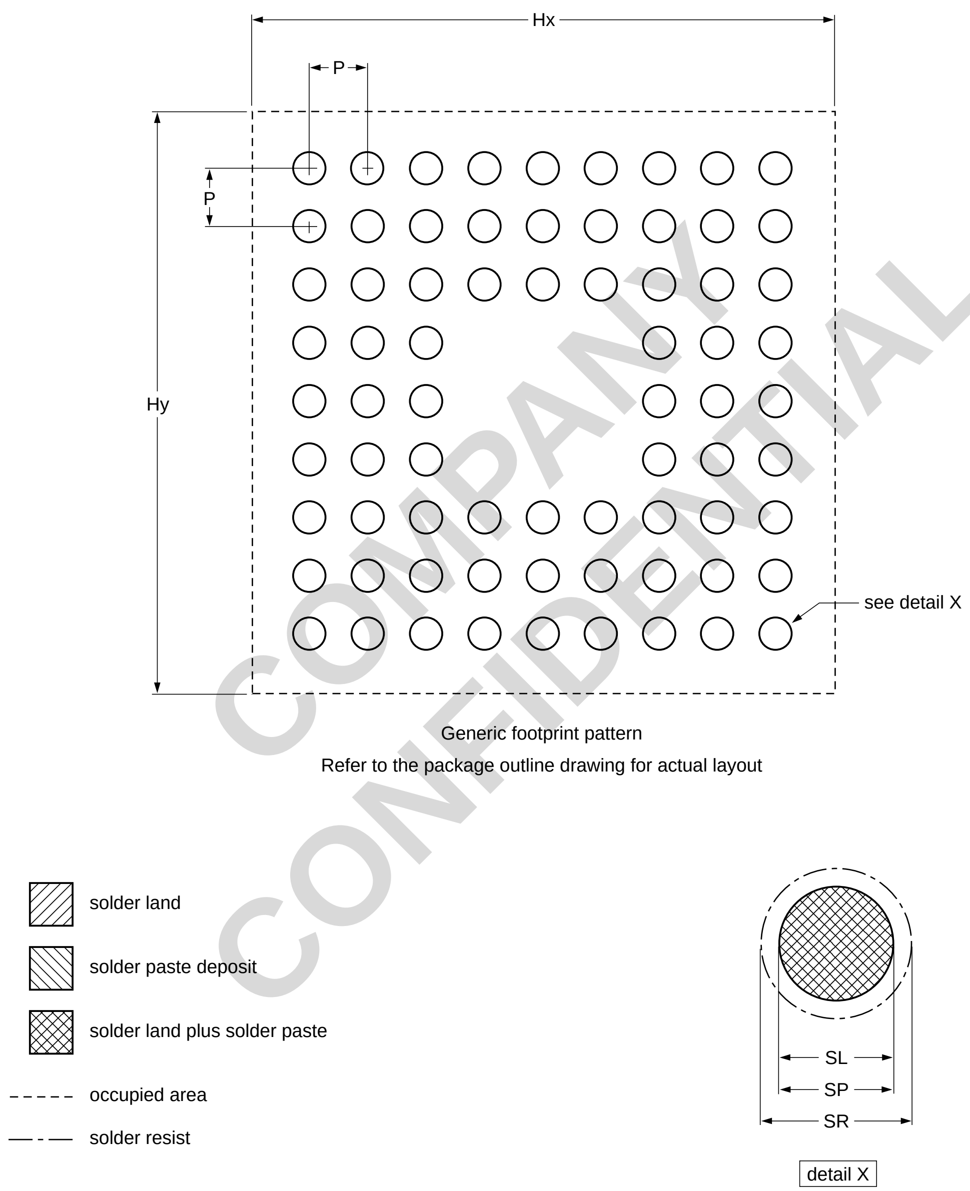
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	D_1	E	E_1	e	e_1	e_2	v	w	y	y_1
mm	2.45	0.6 0.4	1.85 1.60	0.7 0.5	27.2 26.8	24.75 23.75	27.2 26.8	24.75 23.75	1	25	25	0.3	0.15	0.2	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT795-1	144E	MS-034	- - -			~~02-11-18~~ 05-04-26

Fig 22. Package outline SOT795-1 (BGA456)

Footprint information for reflow soldering of BGA456 package SOT795-1



DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	27.575	27.575

Fig 23. Soldering footprint SOT795-1 (BGA456)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 49 and 50

Table 49. SnPb eutectic process (from J-STD-020C)

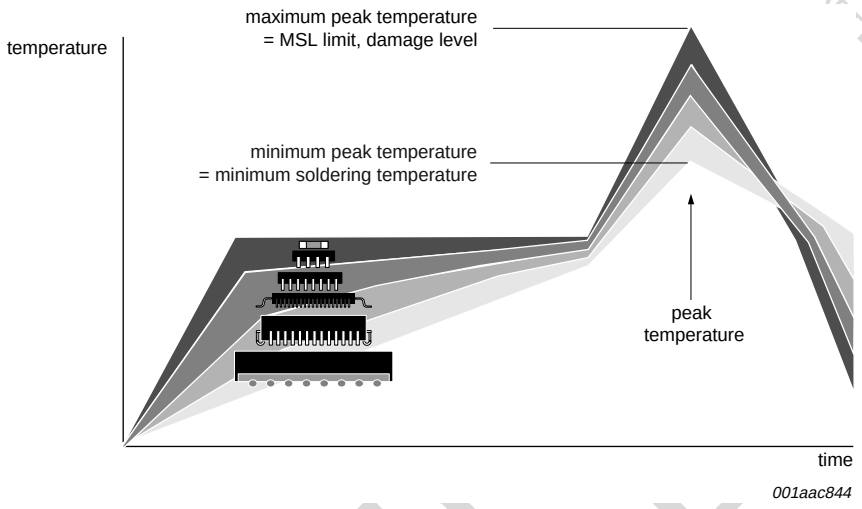
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 50. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 51. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AI	Audio Input
AI2	Audio Input 2 interface
AO	Audio Output
AO2	Audio Output 2 interface
BOM	Bill Of Materials
CAB	Custom Analog Block
CD	Compact Disc
CGU	Clock Generation Unit
CPU	Central Processing Unit
DAB	Digital Audio Broadcast
DAC	Digital-to-Analog Converter
DCS	Device Status and Control
DDR	Double Data Rate
DDS	Direct Digital Synthesis
DLL	Delay-Locked Loop
DLNA	Digital Living Network Alliance[1]
DMA	Direct Memory Access
DTL	Device Transaction Level

Table 51. Abbreviations *…continued*

Acronym	Description
DV	Digital Video
DVD	Digital Versatile Disc
DVD-D	DVD-Descrambler
EDDI	Edge-Dependent De-Interlacing
EJTAG	Enhanced JTAG
FB	Fuse Box
FGPI	Fast General Purpose Interface
FIFO	First-In First-Out
FIR	Finite Impulse Response
FSE	Front Seat Entertainment
GPIO	General Purpose Input and Output
GUI	Graphical User Interface
HD	High-Definition
HDD	Hard Disc Drive
HDTV	High-Definition TV
HS	High-Speed
IC	Integrated Circuit
IDE	Integrated Drive Electronics
I^2C-bus	Inter-IC bus
I^2S	Inter-IC Sound
I/O	Input/Output
ITU	International Telecommunication Union
JEDEC	Joint Electron Device Engineering Council[2]
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LUT	Look-Up Table
MBS	Memory Based Scaler
MMIO	Memory Mapped I/O
MPEG	Moving Picture Expert Group
MSB	Most Significant Bit
NTSC	National Television Standards Committee
OSD	On-Screen Display
OTG	On-The-Go
PAL	Phase Alternating Line
PCI-bus	Peripheral Component Interconnect-bus
PI	Programming Interface
PIO	Programming I/O
PLL	Phase-Locked Loop

Table 51. Abbreviations *…continued*

Acronym	Description
QVCP	Quality Video Composition Processor
RAM	Random Access Memory
RGB	Red Green Blue
RSE	Rear Seat Entertainment
R/W	Read/Write
SD card	Secure Digital card
SDRAM	Synchronous Dynamic RAM
SDTV	Standard-Definition TV
SSTL[3]	Stub Series Terminated Logic
SW	SoftWare
TM	TriMedia
TS	Transport Stream
TSU	Time Stamp Unit
TV	TeleVision
UI	User Interface
USB	Universal Serial Bus
VBI	Vertical Blanking Interval
VDI	ViDeo Input
VDO	ViDeo Output
VDOB	ViDeo Out Buffer
VESA	Video Electronics Standards Association
VGA	Video Graphics Array
VIP	Video Input Processor
XIO	eXtended I/O

[1] An international, cross-industry collaboration of consumer electronics, computing industry and mobile device companies.

[2] Nowadays called JEDEC Solid State Technology Association, or simply JEDEC.

[3] *EIA/JESD8-9b 2002* defines this standard for DDR SDRAM interfaces.

18. Glossary

Bluetooth — A standard for wireless radio communications.

Co-sited video — The video pixel are more regularly distributed across the video memory.

DDR1 — Same as DDR, see Table 51.

DDR2 — DDR memory with 4-fold, instead of 2-fold, prefetch for high bandwidth storage.

FLASH memory — Non-volatile memory that can be electrically erased and programmed.

Interspersed video — The video pixel are interspersed in memory; the VDO module makes them accessible again.

UV — The U- and V-components of a YUV signal.

WiFi — Wireless technology used to connect portable devices to the car.

YUV — The color space used in the PAL analog television standard.

19. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[4] UTMI+ Specification Rev. 1.0

[5] USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[6] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[7] Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) (JESD22-A115-A)

[8] Field-Induced Charged-Device Model Test Method for Electrostatic Discharge-Withstand Thresholds of Microelectronic Components (JESD22-C101C)

[9] Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test (IEC 61000-4-2)

20. Revision history

Table 52. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PNX9530_PNX9531_PNX9535_1	<yyyymmdd>	Preliminary data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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