HARRIS SEMICONDUCTOR

CA3130

BiMOS Operational Amplifier with MOSFET Input/CMOS Output

April 1993

Features

- MOSFET Input Stage Provides:
  - Very High Z_i = 1.5 TΩ (1.5 x 10^{12}Ω) Typ.
  - Very Low I_I = 5pA Typ. at 15V Operation
    = 2pA Typ. at 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input-Voltage Range Includes Negative Supply Rail; Input Terminals can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or both) Supply Rails

Applications

- Ground-Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long-Duration Timers/Monostables
- High-Input-Impedance Comparators (Ideal Interface with Digital CMOS)
- High-Input-Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Peak Detectors
- Single-Supply Full-Wave Precision Rectifiers
- Photo-Diode Sensor Amplifiers

Description

CA3130A and CA3130 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

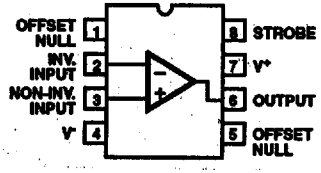
A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions can also made to permit strobing of the output stage.

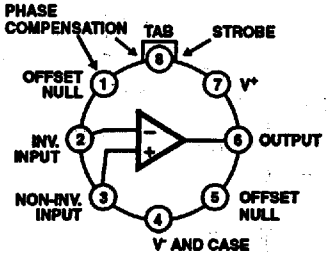
The CA3130A offers superior input characteristics over those of the CA3130.

Pinouts

CA3130, CA3130A
(PDIP, SOIC)
TOP VIEW



CA3130, CA3130A
(CAN)
TOP VIEW



Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
CA3130AE	-55°C to +125°C	8 Lead PDIP
CA3130AM	-55°C to +125°C	8 Lead SOIC
CA3130AM96	-55°C to +125°C	8 Lead SOIC*
CA3130AT	-55°C to +125°C	8 Pin CAN
CA3130BT	-55°C to +125°C	8 Pin CAN
CA3130E	-55°C to +125°C	8 Lead PDIP
CA3130M	-55°C to +125°C	8 Lead SOIC
CA3130M96	-55°C to +125°C	8 Lead SOIC*
CA3130T	-55°C to +125°C	8 Pin CAN

* Denotes Tape and Reel

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 817.2

Specifications CA3130, CA3130A

Absolute Maximum Ratings

DC Supply Voltage (Between V^+ And V^- Terminals) 16V
Differential-Mode Input Voltage 8V
DC Input Voltage ..... (V^+ +8 V) to (V^- -0.5V)
Input-Terminal Current 1mA
Device Dissipation:
  Without Heat Sink-
    Up To 55°C ..... 630 mW
    Above 55°C ..... Derate Linearly 6.67 mW/°C
  With Heat Sink-
    Up To 90°C 1W
    Above 90°C ..... Derate Linearly 16.7 mW/°C.
Output Short-Circuit Duration (Note 1) ..... Indefinite
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
Lead Temperature (Soldering 10 Sec.) ..... +300°C

Operating Conditions

Operating Temperature Range (All Types) ..... -55°C to +125°C
Storage Temperature Range(All Types) ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 15V, V- = 0V (Unless Otherwise Specified)

PARAMETERS	SYMBOLS	TEST CONDITIONS	LIMITS						UNITS
			CA3130A			CA3130			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\|V_{IO}\|$	V± = ±7.5V	-	2	5	-	8	15	mV
Input Offset Current	$\|I_{IO}\|$	V± = ±7.5V	-	0.5	20	-	0.5	30	pA
Input Current	I_I	V± = ±7.5V	-	5	30	-	5	50	pA
Large-Signal Voltage Gain	A_{OL}	V_O = 10 Vp-p, R_L = 2kΩ	50	320	-	50	320	-	kV/V
			94	110	-	94	110	-	dB
Common-Mode Rejection Ratio	CMRR		80	90	-	70	90	-	dB
Common-Mode Input Voltage Range	V_{ICR}		0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V\pm$	V± = ±7.5V	-	32	150	-	32	320	µV/V
Maximum Output Voltage	$V_{OM}+$	At R_L = 2kΩ	12	13.3	-	12	13.3	-	V
	$V_{OM}-$	At R_L = 2kΩ	-	0.002	0.01	-	0.002	0.01	V
	$V_{OM}+$	At R_L = 2kΩ	14.99	15	-	14.99	15	-	V
	$V_{OM}-$	At R_L = 2kΩ	-	0	0.01	-	0	0.01	V
Maximum Output Current	$I_{OM}+$ (Source) at V_O = 0V		12	22	45	12	22	45	mA
	$I_{OM}-$ (Sink) at V_O = 15V		12	20	45	12	20	45	mA
Supply Current	I+	V_O = 7.5V, R_L = ∞	-	10	15	-	10	15	mA
	I+	V_O = 0V, R_L = ∞	-	2	3	-	2	3	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$		-	10	-	-	10	-	µV/°C

NOTE:
1. Short circuit may be applied to ground or to either supply.

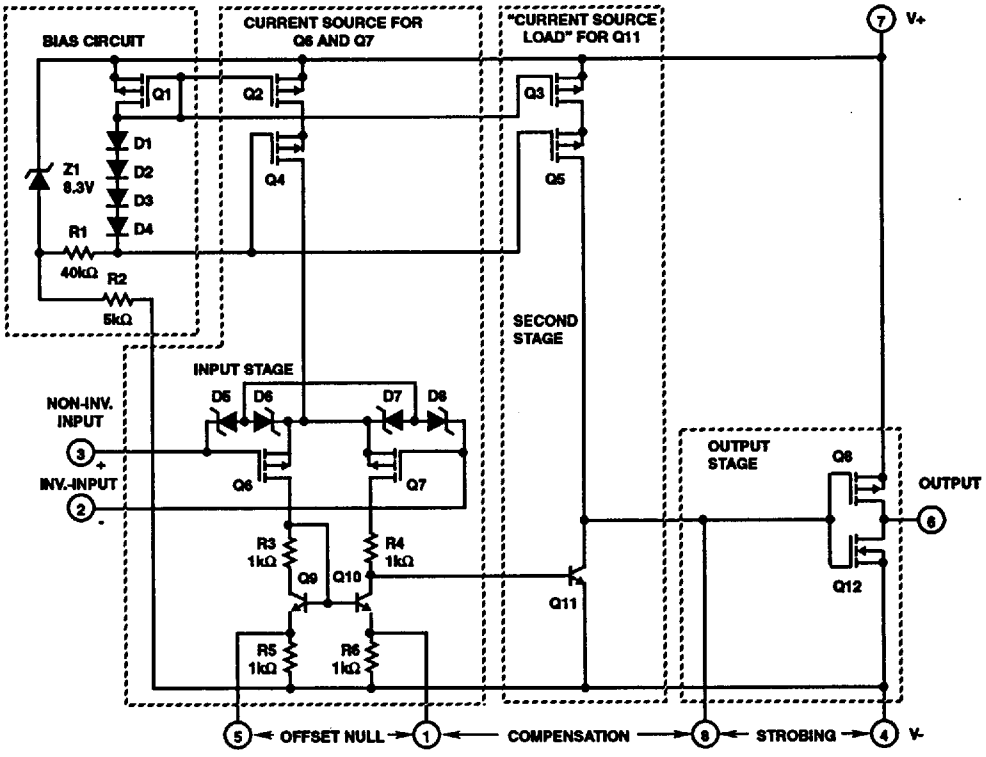
Electrical Specifications Typical Values Intended Only for Design Guidance, V+ = +7.5V, V- = -7.5V, T_A = +25°C (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3130A, CA3130	UNITS
Input Offset Voltage Adjustment Range		10kΩ Across Terms. 4 and 5 or 4 and 1	±22	mV
Input Resistance	R_I		1.5	TΩ
Input Capacitance	C_I	f = 1MHz	4.3	pF
Equivalent Input Noise Voltage	e_N	BW = 0.2MHz, R_S = 1MΩ*	23	μV
Unity Gain Crossover Frequency	f_T	C_C = 0	15	MHz
		C_C = 47pF	4	MHz
Slew Rate:	SR			
Open Loop		C_C = 0	30	V/μs
Closed Loop		C_C = 56pF	10	V/μs
Transient Response:		C_C = 56pF, C_L = 25pF, R_L = 2kW (Voltage Follower)		
Rise Time	t_R		0.09	μs
Overshoot	OS		10	%
Settling Time (To <0.1%, V_{IN} = 4V_{P-P})	t_S		1.2	μs

* Although a 1MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10MΩ.

Electrical Specifications Typical Values Intended Only for Design Guidance, V+ = 5V, V- = 0V, T_A = +25°C (Unless Otherwise Specified)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3130A	CA3130	UNITS
Input Offset Voltage	V_{IO}		2	8	mV
Input Offset Current	I_{IO}		0.1	0.1	pA
Input Current	I_I		2	2	pA
Common-Mode Rejection Ratio	CMRR		90	80	dB
Large-Signal Voltage Gain	A_{OL}	V_O = 4V_{P-P}, R_L = 5kW	100	100	kV/V
			100	100	dB
Common-Mode Input Voltage Range	V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current	I+	V_O = 5V, R_L = ∞	300	300	μA
		V_O = 2.5V, R_L = ∞	500	500	μA
Power Supply Rejection Ratio	$\Delta V_{IO}/\Delta V+$		200	200	μV/V



NOTE: DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOSFET INPUT STAGE

FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3130 SERIES

Circuit Description

Figure 2 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Figure 2, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g.,when the amplifier output is used to drive CMOS digital circuits in Comparator applications).

Input Stages

The circuit of the CA3130 is shown in Figure 1. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000Ω potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascade-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, including static electricity during handling for Q6 and Q7.

Second-Stage

Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascade-connected load resistance provided by

PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit

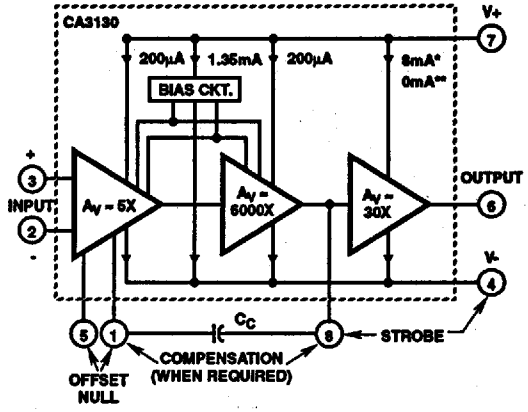
At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"* to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Figure 5. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

* For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File Number 619, data bulletin on CA3600E "CMOS Transistor Array".

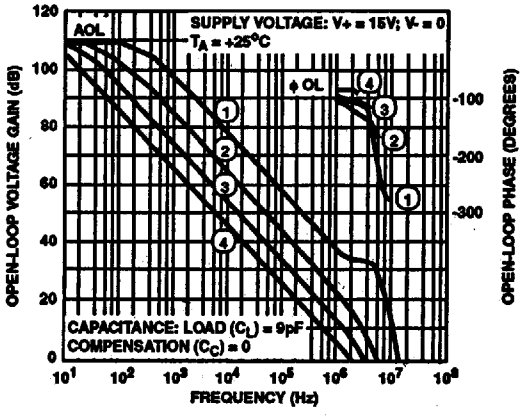


TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15V

*WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5V ABOVE TERM. 4.

**WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

FIGURE 2. BLOCK DIAGRAM OF THE CA3130 SERIES



1 = LOAD RESISTANCE (R_L) = ∞
2 = C_L = 30pF, C_C = 15pF, R_L = 2kΩ
3 = C_L = 30pF, C_C = 47pF, R_L = 2kΩ
4 = C_L = 30pF, C_C = 150pF, R_L = 2kΩ

FIGURE 3. OPEN-LOOP VOLTAGE GAIN AND PHASE SHIFT vs FREQUENCY

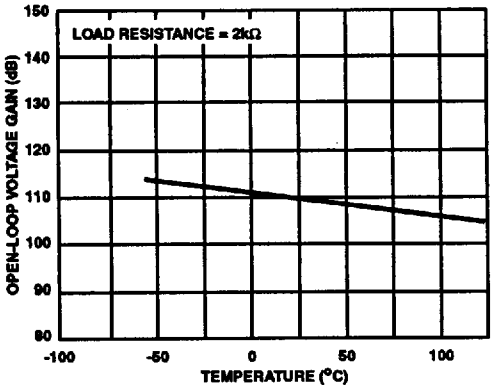


FIGURE 4. OPEN-LOOP GAIN vs TEMPERATURE

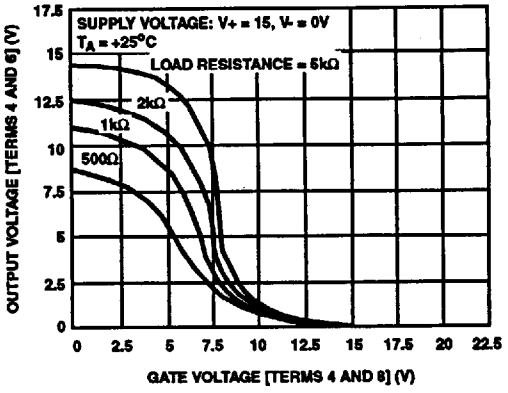


FIGURE 5. VOLTAGE TRANSFER CHARACTERISTICS OF CMOS OUTPUT STAGE

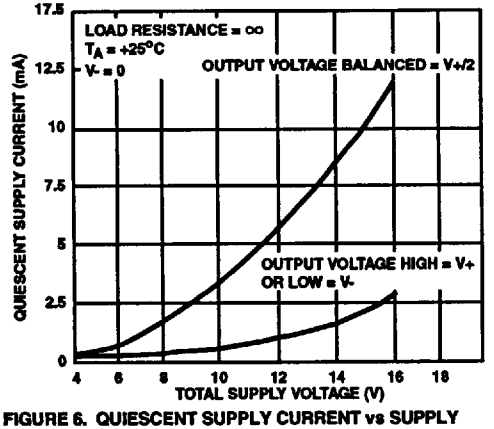


FIGURE 6. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

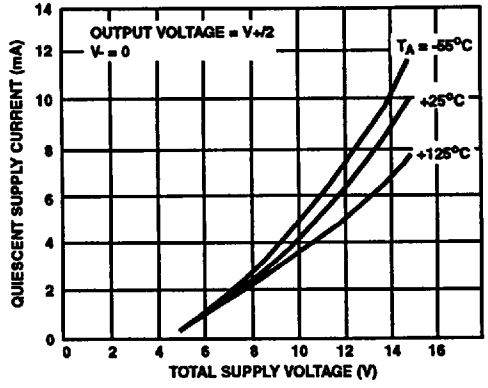


FIGURE 7. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE

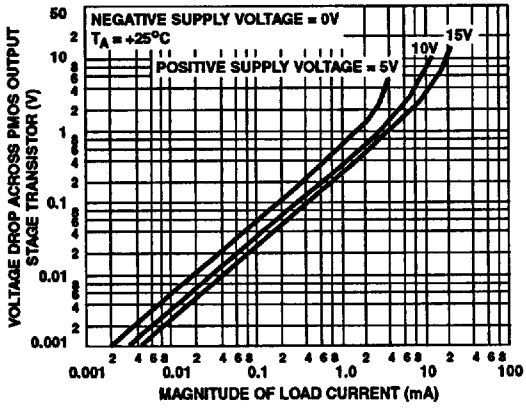


FIGURE 8. VOLTAGE ACROSS PMOS OUTPUT TRANSISTOR (Q8) vs LOAD CURRENT

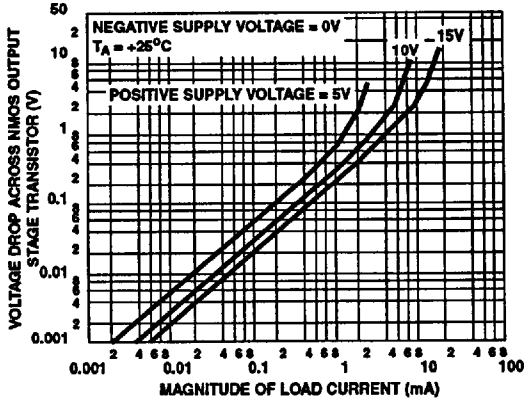


FIGURE 9. VOLTAGE ACROSS NMOS OUTPUT TRANSISTOR (Q12) vs LOAD CURRENT

Input Current Variation with Common Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5pA at T_A = +25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Figure 10 contains data showing the variation of input current as a function of common-mode input voltage at T_A = +25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

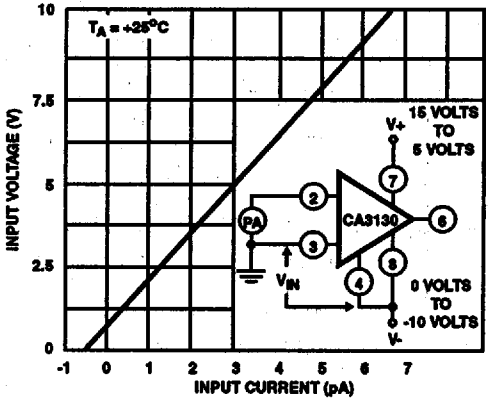


FIGURE 10. INPUT CURRENT vs COMMON-MODE VOLTAGE

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5pA at +25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op-amps with a junction-FET input stage, the leakage current approximately doubles for every +10°C increase in temperature. Figure 11 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

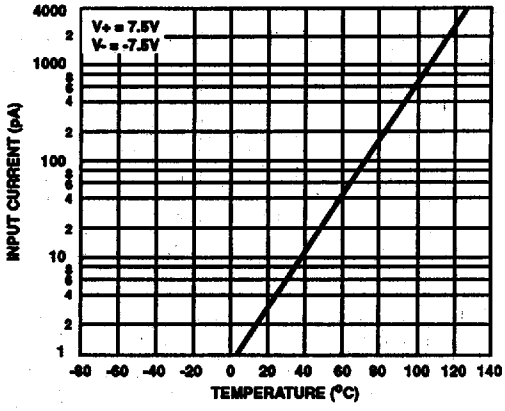


FIGURE 11. INPUT CURRENT vs AMBIENT TEMPERATURE

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs Device Operating Life

It is well known that the characteristics of a MOSFET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Figure 12 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at +85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

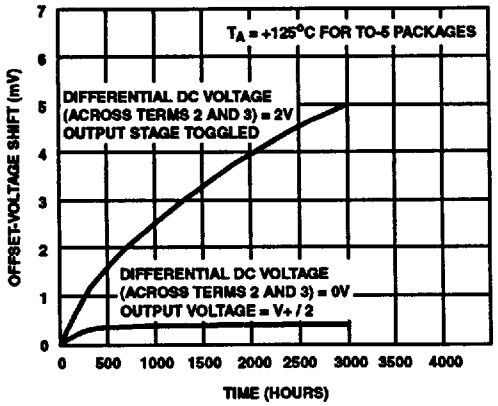
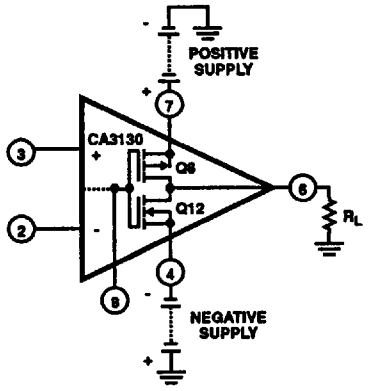
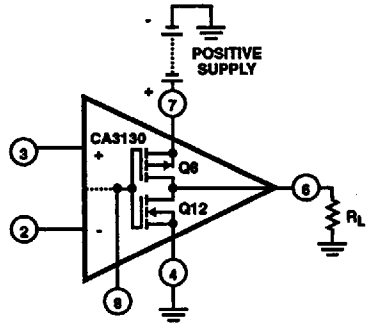


FIGURE 12. TYPICAL INCREMENTAL OFFSET-VOLTAGE SHIFT vs OPERATING LIFE



(A) DUAL POWER-SUPPLY OPERATION



(B) SINGLE POWER-SUPPLY OPERATION

FIGURE 13. CA3130 OUTPUT STAGE IN DUAL AND SINGLE POWER-SUPPLY OPERATION

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figures 13A and 13B show the CA3130 connected for both dual-and single-supply operation.

Dual-supply Operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply Operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Figure 6 shows typical quiescent supply-current vs supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Figure 5). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Figure 6) even though the output stage is strobed off. Figure 13A shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$ by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Figure 13B. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Figure 8 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Figure 5 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is on the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23μV when the

test-circuit amplifier of Figure 14 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

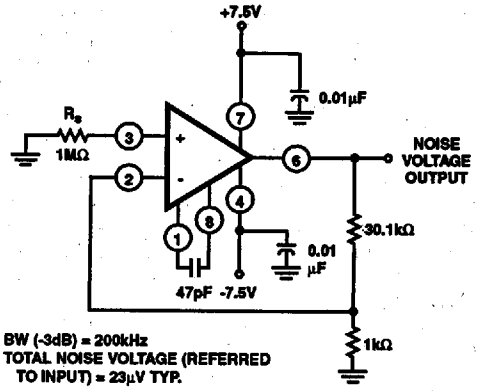


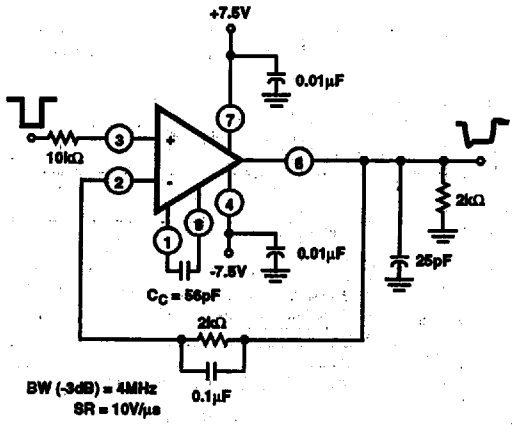
FIGURE 14. TEST-CIRCUIT AMPLIFIER (30-dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENTS

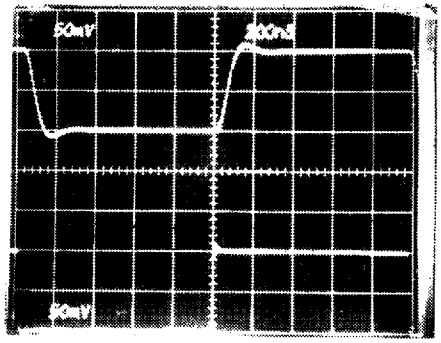
Typical Applications

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Figure 15 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

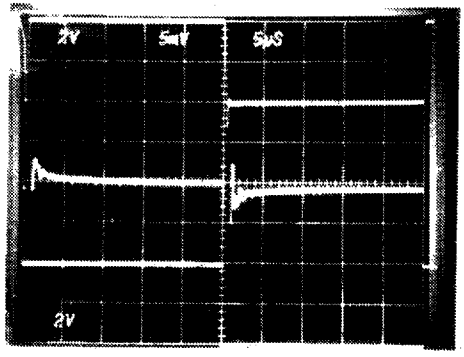
A voltage follower, operated from a single supply, is shown in Figure 16, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Figure 16A with input-signal ramping. The waveforms in Figure 16B show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Figure 16B also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.





Top Trace: Output
Bottom Trace: Input

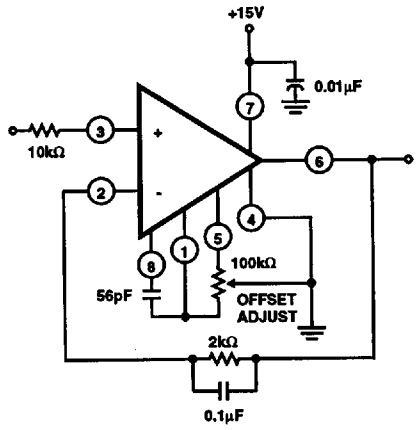
(A) SMALL-SIGNAL RESPONSE (50mV/DIV. AND 200ns/DIV.)

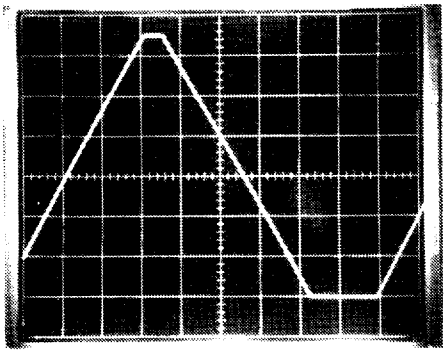


Top Trace: Output Signal (2V/DIV. and 5μs/DIV.)
Center Trace: Difference Signal (5mV/DIV. and 5μs/DIV.)
Bottom Trace: Input Signal (2V/DIV. and 5μs/DIV.)

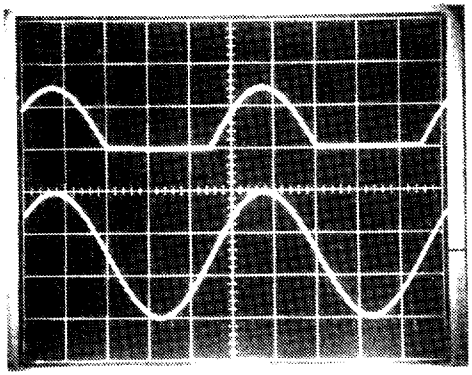
(B) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)

FIGURE 15. SPLIT-SUPPLY VOLTAGE FOLLOWER WITH ASSOCIATED WAVEFORMS





(A) OUTPUT-WAVEFORM WITH INPUT-SIGNAL RAMPING (2V/DIV. AND 500μs/DIV.)



Top Trace: Output (5V/DIV. and 200μs/DIV.)
Bottom Trace: Input Signal (5V/DIV. and 200μs/DIV.)

(B) OUTPUT WAVEFORM WITH GROUND-REFERENCE SINE-WAVE INPUT

FIGURE 16. SINGLE-SUPPLY VOLTAGE-FOLLOWER WITH ASSOCIATED WAVEFORMS. (e.g., FOR USE IN SINGLE-SUPPLY D/A CONVERTER; SEE FIGURE 9 IN AN6080)

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Figure 17 This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op-amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Figure 17.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one percent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

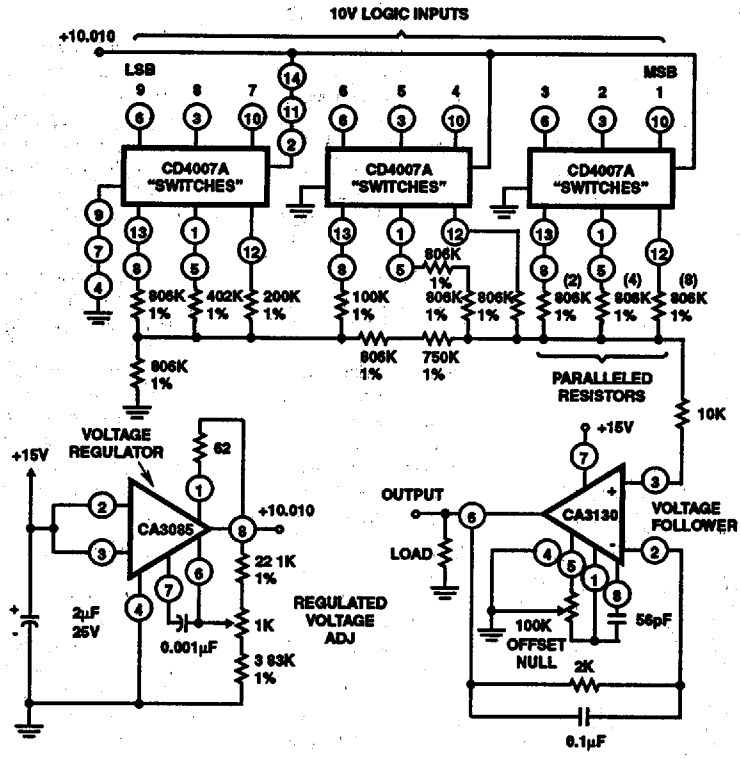
A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Figure 18. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Figure 18 is satisfied, the full-wave output is symmetrical.

Peak Detectors

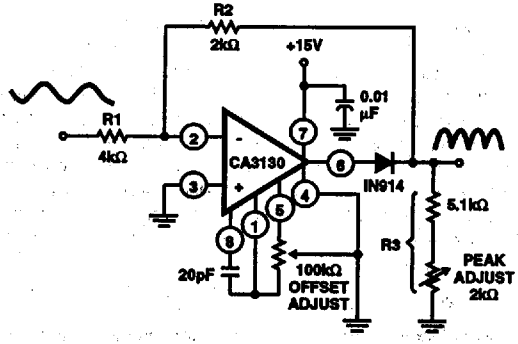
Peak-detector circuits are easily implemented with the CA3130, as illustrated in Figure 19 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6 - 9	±1% ABS

ALL RESISTANCES IN OHMS

FIGURE 17. 18-9-BIT DAC USING CMOS DIGITAL SWITCHES AND CA3130

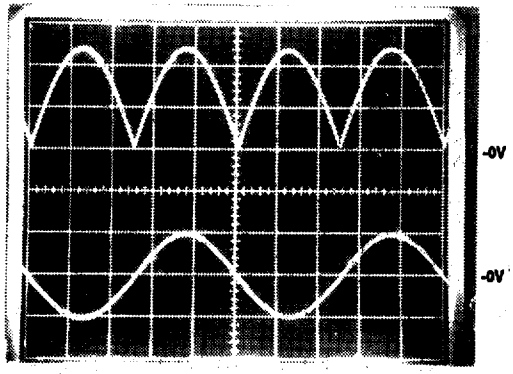


$$\text{Gain} = \frac{R_2}{R_1} = X = \frac{R_3}{R_1 + R_2 + R_3}$$

$$R_3 = R_1\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{For } X = 0.5: \frac{2k\Omega}{4k\Omega} = \frac{R_2}{R_1}$$

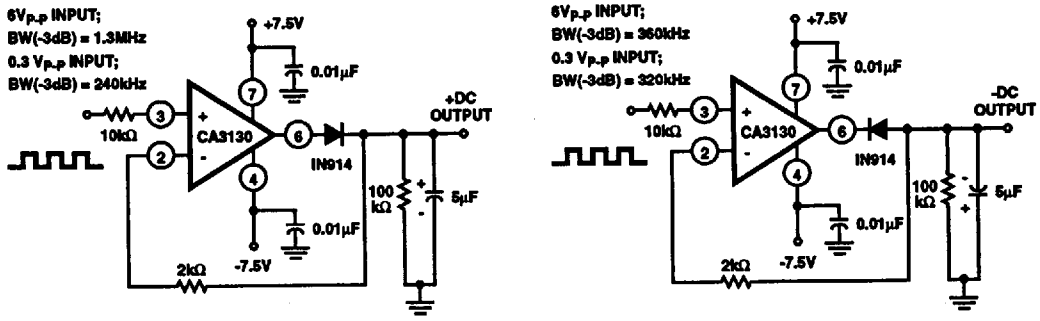
$$R_3 = 4k\Omega\left(\frac{0.75}{0.5}\right) = 6k\Omega$$



Top Trace: Output Signal (2V/div.)
Bottom Trace: Input Signal (10V/div.)
Time base on both traces: 0.2ms/div.

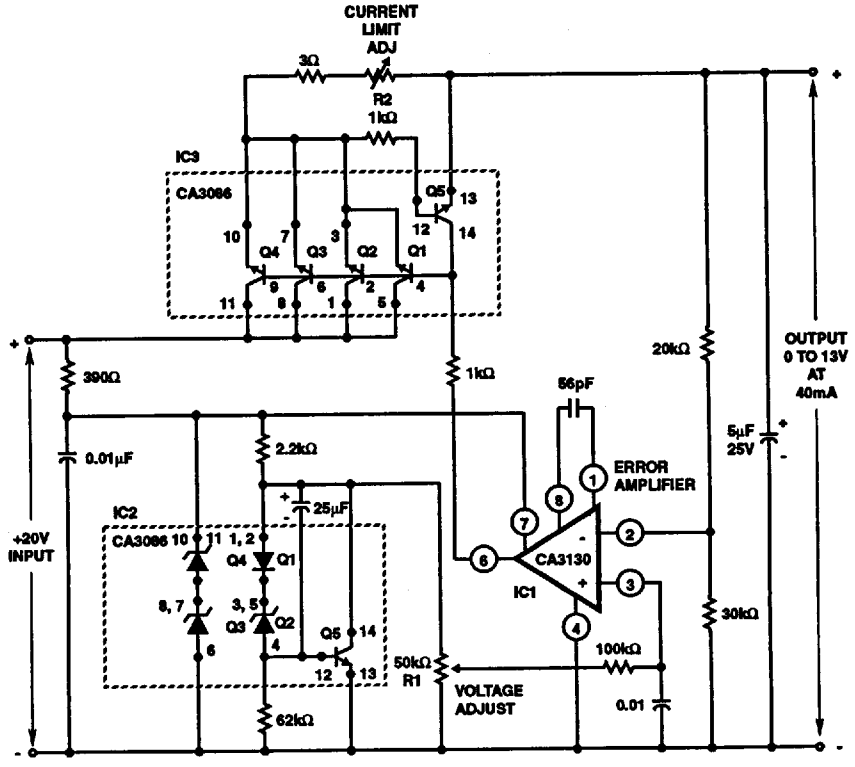
20Vp-p Input: BW(-3dB) = 230kHz, DC Output (Avg.) = 3.2V
1Vp-p Input: BW(-3dB) = 130kHz, DC Output (Avg.) = 160mV

FIGURE 18. SINGLE-SUPPLY, ABSOLUTE-VALUE, IDEAL FULL-WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS



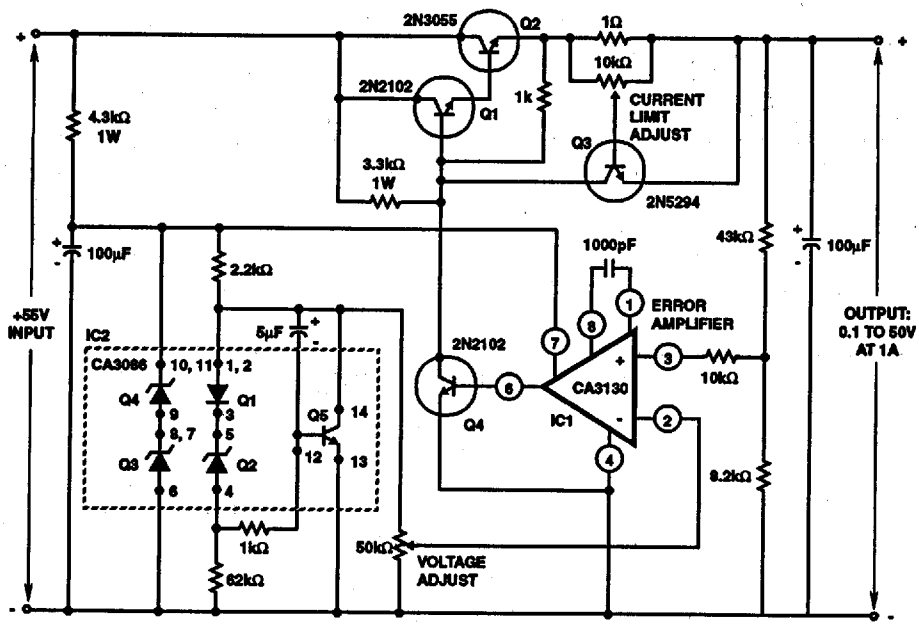
(A) PEAK POSITIVE DETECTOR CIRCUIT (B) PEAK NEGATIVE DETECTOR CIRCUIT

FIGURE 19. PEAK-DETECTOR CIRCUITS



REGULATION (NO LOAD TO FULL LOAD): < 0.01%
INPUT REGULATION: 0.02%/V
HUM AND NOISE OUTPUT: < 25µV UP TO 100kHz

FIGURE 20. VOLTAGE REGULATOR CIRCUIT (0 TO 13V AT 40mA)



REGULATION (NO LOAD TO FULL LOAD): < 0.005%
INPUT REGULATION: 0.01%/V
HUM AND NOISE OUTPUT: < 250µV RMS UP TO 100kHz

FIGURE 21. VOLTAGE REGULATOR CIRCUIT (0.1 TO 50V AT 1A)

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Figure 20 shows the schematic diagram of a 40mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Figure 21 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Figure 22. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Figure 23 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

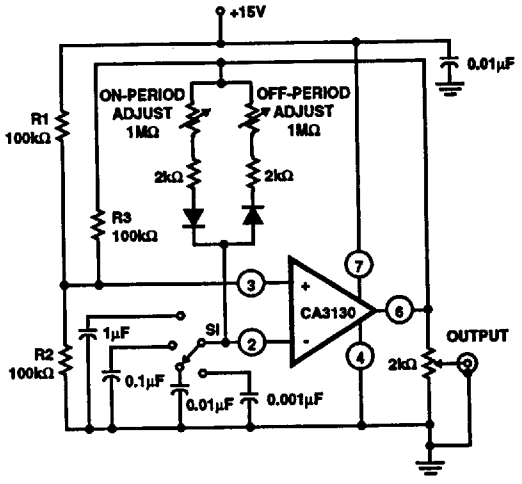
Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

Operation with Output-Stage Power-Booster

The current-sourcing and-sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Figure 24, three CMOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Figure 24 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (-3dB) is 50 kHz.

* See File Number 619 for technical information.



FREQUENCY RANGE:

POSITION OF S1	PULSE PERIOD
0.001μF	4μs to 1ms
0.01μF	40μs to 10ms
0.1μF	0.4μs to 100ms
1μF	4μs to 1s

FIGURE 22. PULSE GENERATOR (ASTABLE MULTIVIBRATOR) WITH PROVISIONS FOR INDEPENDENT CONTROL OF "ON" AND "OFF" PERIODS.

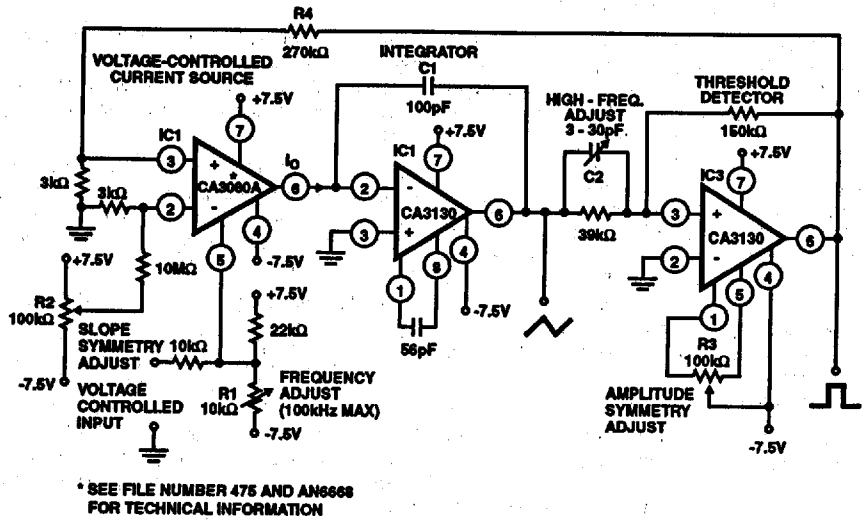


FIGURE 23. FUNCTION GENERATOR (FREQUENCY CAN BE VARIED 1,000,000/1 WITH A SINGLE CONTROL).

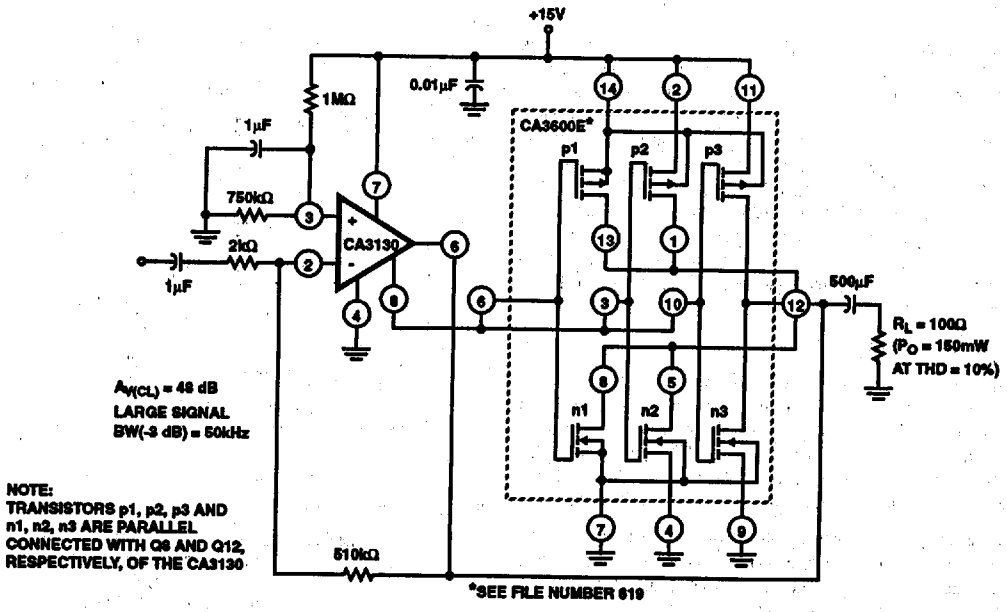


FIGURE 24. CMOS TRANSISTOR ARRAY (CA3600E) CONNECTED AS POWER BOOSTER IN THE OUTPUT STAGE OF THE CA3130.