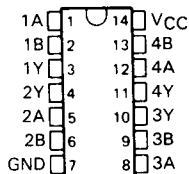


SN54HC386, SN74HC386 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

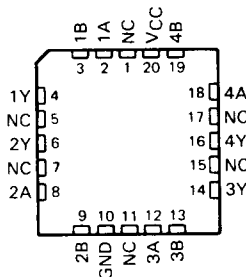
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC386 . . . J PACKAGE
SN74HC386 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC386 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

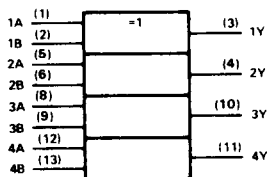
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54HC386 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC386 is characterized for operation from -40°C to 85°C .

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	$-0.5\text{ V to }7\text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	$\pm 20\text{ mA}$
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	$\pm 20\text{ mA}$
Continuous output current, I_O ($V_O = 0$ to V_{CC})	$\pm 25\text{ mA}$
Continuous current through V_{CC} or GND pins	$\pm 50\text{ mA}$
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	$-65^{\circ}\text{C to }150^{\circ}\text{C}$

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2

HCMOS Devices

SN54HC386, SN74HC386
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

2
HCMOS Devices

recommended operating conditions

		SN54HC386			SN74HC386			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V		1.5 3.15 4.2	1.5 3.15 4.2			V
V _{IL}	Low-level input voltage	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V		0 0 0	0.3 0.9 1.2		0 0.3 1.2	V
V _I	Input voltage			0	V _{CC}		V _{CC}	V
V _O	Output voltage			0	V _{CC}		V _{CC}	V
t _t	Input transition (rise and fall) times	V _{CC} = 2 V V _{CC} = 4.5 V V _{CC} = 6 V		0 0 0	1000 500 400		0 500 400	ns
T _A	Operating free-air temperature			-55	125		-40 85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC386		SN74HC386		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
	V _I = V _{IH} or V _{IL} , I _{OH} = -5.2 mA	6 V	5.48	5.80		5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	4.5 V		0.17	0.26		0.4		0.33		
	6 V		0.15	0.26		0.4		0.33		
	V _I = V _{IH} or V _{IL} , I _{OL} = 5.2 mA	6 V								
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			2		40		20	μA
C _i		2 to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC386		SN74HC386		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t _t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C _{pd}	Power dissipation capacitance per gate	No load, T _A = 25°C	35 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.