

MAX44241/MAX44243/MAX44246

36V, Low-Noise, Precision, Single/Quad/Dual Op Amps

General Description

The MAX44241/MAX44243/MAX44246 are 36V, ultra-precision, low-noise, low-drift, single/quad/dual operational amplifiers that offer near-zero DC offset and drift through the use of patented chopper stabilized and auto-zeroing techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of $1/f$ noise. These single/quad/dual devices feature rail-to-rail outputs, operate from a single 2.7V to 36V supply or dual $\pm 1.35V$ to $\pm 18V$ supplies, and consume only 0.42mA per channel, with only $9nV/\sqrt{Hz}$ input-referred voltage noise.

The ICs are available in 8-pin μ MAX® or SO packages and are rated over the $-40^{\circ}C$ to $+125^{\circ}C$ temperature range.

Applications

Transducer Amplifiers	Battery-Powered Equipment
Load Cell Amplifiers	PLC Analog I/O Modules
Precision Instrumentation	

Benefits and Features

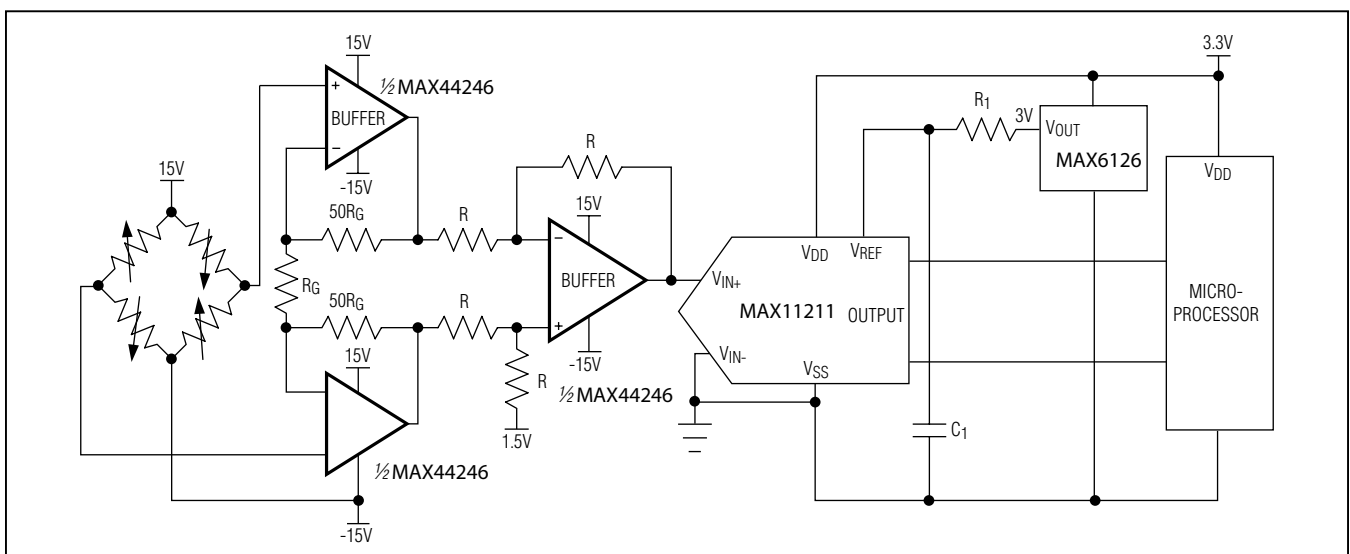
- ◆ **Reduces Noise-Sensitive Precision Applications**
 - Low $9nV/\sqrt{Hz}$ Noise at 1kHz
 - Integrated EMI Filter
- ◆ **Eliminates Cost of Calibration with Increased Accuracy and Patented Auto-Zero Circuitry**
 - Ultra-Low Input V_{OS} : $5\mu V$ (max)
 - Low $20nV/^{\circ}C$ (max) of Offset Drift
- ◆ **Suitable for High-Bandwidth Applications**
 - $1\mu s$ Fast Settling Time
 - 5MHz Gain-Bandwidth Product
- ◆ **Low 0.55mA Per Channel (max) Quiescent Current**
- ◆ **Wide Supply for High-Voltage Front-Ends**
 - 2.7V to 36V Supply Range
- ◆ **Rail-to-Rail Output**

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX44241.related.

μ MAX is a registered trademark of Maxim Integrated Products, Inc.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to GND)	-0.3V to +40V	8-Pin SO (derate 7.60mW/°C above +70°C).....	606.1mW
All Other Pins.....	(GND - 0.3V) to (V_{DD} + 0.3V)	14-Pin SO (derate 12.30mW/°C above +70°C).....	987.7mW
Short-Circuit Duration, OUTA, OUTB to Either Supply Rail.....	1s	14-Pin TSSOP (derate 10mW/°C above +70°C).....	796.8mW
Continuous Input Current (Any Pin)	20mA	Operating Temperature Range	-40°C to +125°C
Differential Input Current.....	±20mA	Junction Temperature	+150°C
Differential Input Voltage (Note 1).....	±6V	Storage Temperature Range.....	-65°C to +150°C
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)		Lead Temperature (soldering, 10s)	+300°C
5-Pin SOT23 (derate 3.9mW/°C above +70°C).....	312.6mW	Soldering Temperature (reflow)	+260°C
8-Pin μ MAX (derate 4.8mW/°C above +70°C).....	387.8mW		

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding $\pm 1\text{V}$ are applied, limit input current to 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

μ MAX	SOT23		
Junction-to-Ambient Thermal Resistance (θ_{JA})	206.3°C/W	Junction-to-Ambient Thermal Resistance (θ_{JA})	255.9°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	42°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	81°C/W
SO-8	TSSOP		
Junction-to-Ambient Thermal Resistance (θ_{JA})	132°C/W	Junction-to-Ambient Thermal Resistance (θ_{JA})	100.4°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	38°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	30°C/W
SO-14			
Junction-to-Ambient Thermal Resistance (θ_{JA})	81°C/W		
Junction-to-Case Thermal Resistance (θ_{JC})	32°C/W		

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 30\text{V}$, $V_{GND} = 0\text{V}$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5\text{k}\Omega$ to $V_{DD}/2$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. Typical values at $T_A = +25^\circ\text{C}$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Voltage Range	V_{DD}	Guaranteed by PSRR	2.7		36	V	
Power-Supply Rejection Ratio (Note 4)	PSRR	$V_{DD} = 2.7\text{V}$ to 36V , $T_A = +25^\circ\text{C}$	148	166		dB	
		$V_{DD} = 2.7\text{V}$ to 36V , $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	146				
Quiescent Current per Amplifier	I_{DD}	$R_L = \infty$		$T_A = +25^\circ\text{C}$	0.42	0.55	mA
				$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.60	
Power-Up Time	t_{ON}			20		μs	
DC SPECIFICATIONS							
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	$(V_{GND} - 0.05)$		$(V_{DD} - 1.5)$	V	
Common-Mode Rejection Ratio (Note 4)	CMRR	$V_{CM} = (V_{GND} - 0.05\text{V})$ to $(V_{DD} - 1.5\text{V})$	146	166		dB	
Input Offset Voltage (Note 4)	V_{OS}			1	5	μV	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 30V$, $V_{GND} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values at $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage Drift (Note 4)	$TC V_{OS}$			1	20	nV/°C
Input Bias Current (Note 4)	I_B	$T_A = +25^\circ C$		300	600	pA
		$-40^\circ C < T_A < +125^\circ C$			1250	
Input Offset Current (Note 4)	I_{OS}	$T_A = +25^\circ C$		600	1200	pA
		$-40^\circ C < T_A < +125^\circ C$			2500	
Open-Loop Gain (Note 4)	A_{VOL}	$(V_{GND} + 0.5V) \leq V_{OUT} \leq (V_{DD} - 0.5V)$	154	168		dB
Output Short-Circuit Current		Noncontinuous	Sinking	40		mA
			Sourcing	30		
Output Voltage Low	V_{OL}	$T_A = +25^\circ C$		90	115	mV
		$-40^\circ C < T_A < +125^\circ C$			180	
Output Voltage High	V_{OH}	$T_A = +25^\circ C$	$(V_{DD} - 0.17)$	$(V_{DD} - 0.13)$		V
		$-40^\circ C < T_A < +125^\circ C$	$(V_{DD} - 0.25)$			

AC SPECIFICATIONS

Input Voltage-Noise Density	e_N	$f = 1kHz$		9		nV/√Hz
Input Voltage Noise		$0.1Hz < f < 10Hz$		117		nV _{P-P}
Input Capacitance	C_{IN}			2		pF
Gain-Bandwidth Product	GBW			5		MHz
Phase Margin	PM	$C_L = 20pF$		60		Degrees
Slew Rate	SR	$A_V = 1V/V$, $V_{OUT} = 4V_{P-P}$		3.8		V/μs
Capacitive Loading	C_L	No sustained oscillation, $A_V = 1V/V$		300		pF
Total Harmonic Distortion	THD	$V_{OUT} = 4V_{P-P}$, $A_V = +1V/V$	$f = 1kHz$	-96		dB
			$f = 20kHz$	-77		
		$V_{OUT} = 2V_{P-P}$, $A_V = +1V/V$	$f = 1kHz$	-91		dB
			$f = 20kHz$	-76		

ELECTRICAL CHARACTERISTICS

($V_{DD} = 10V$, $V_{GND} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values at $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Quiescent Current per Amplifier	I_{DD}	$R_L = \infty$	$T_A = +25^\circ C$	0.42	0.55	mA
			$-40^\circ C < T_A < +125^\circ C$		0.60	
Power-Up Time	t_{ON}			20		μs

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 10V$, $V_{GND} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values at $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC SPECIFICATIONS						
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	$(V_{GND} - 0.05)$		$(V_{DD} - 1.5)$	V
Common-Mode Rejection Ratio (Note 4)	CMRR	$V_{CM} = (V_{GND} - 0.05V)$ to $(V_{DD} - 1.5V)$	140	158		dB
Input Offset Voltage (Note 4)	V_{OS}			1	5	μV
Input Offset Voltage Drift (Note 4)	TC V_{OS}			2.4	20	nV/ $^\circ C$
Input Bias Current (Note 4)	I_B	$T_A = +25^\circ C$		300	600	pA
		$-40^\circ C < T_A < +125^\circ C$			1100	
Input Offset Current (Note 4)	I_{OS}	$T_A = +25^\circ C$		600	1200	pA
		$-40^\circ C < T_A < +125^\circ C$			2200	
Open-Loop Gain (Note 4)	A_{VOL}	$(V_{GND} + 0.5V) \leq V_{OUT} \leq (V_{DD} - 0.5V)$	144	164		dB
Output Short-Circuit Current		Noncontinuous	Sinking	40		mA
			Sourcing	30		
Output Voltage Low	V_{OL}	$T_A = +25^\circ C$		30	40	mV
		$-40^\circ C < T_A < +125^\circ C$			60	
Output Voltage High	V_{OH}	$T_A = +25^\circ C$	$(V_{DD} - 0.06)$	$(V_{DD} - 0.05)$		V
		$-40^\circ C < T_A < +125^\circ C$	$(V_{DD} - 0.09)$			
AC SPECIFICATIONS						
Input Voltage-Noise Density	e_N	$f = 1kHz$		9		nV/ \sqrt{Hz}
Input Voltage Noise		$0.1Hz < f < 10Hz$		117		nV _{P-P}
Input Capacitance	C_{IN}			2		pF
Gain-Bandwidth Product	GBW			5		MHz
Phase Margin	PM	$C_L = 20pF$		60		Degrees
Slew Rate	SR	$A_V = +1V/V$, $V_{OUT} = 2V_{P-P}$, 10% to 90%		3.8		V/ μs
Capacitive Loading	C_L	No sustained oscillation, $A_V = 1V/V$		300		pF
Total Harmonic Distortion	THD	$V_{OUT} = 2V_{P-P}$, $A_V = 1V/V$	$f = 1kHz$	-92		dB
			$f = 20kHz$	-76		
Settling Time		To 0.01%, $V_{OUT} = 2V$ step, $A_V = 1V/V$		1		μs

Note 3: All devices are 100% production tested at $T_A = +25^\circ C$. Temperature limits are guaranteed by design.

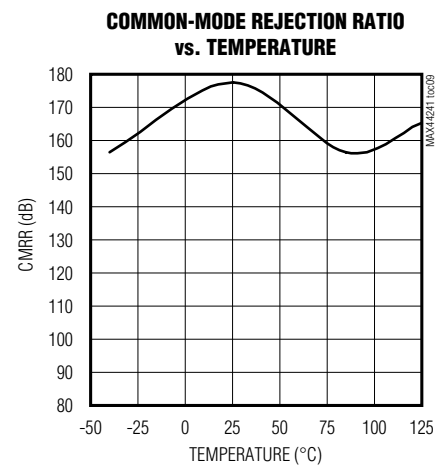
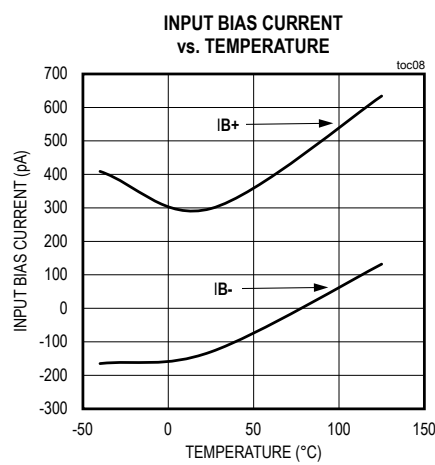
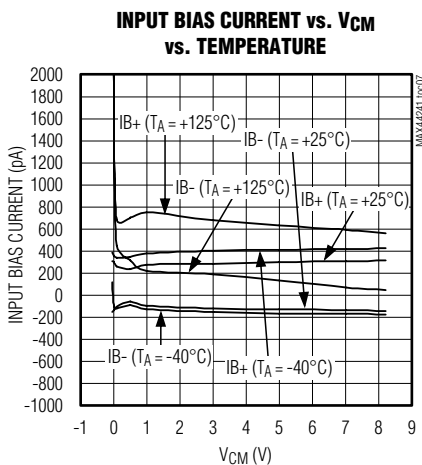
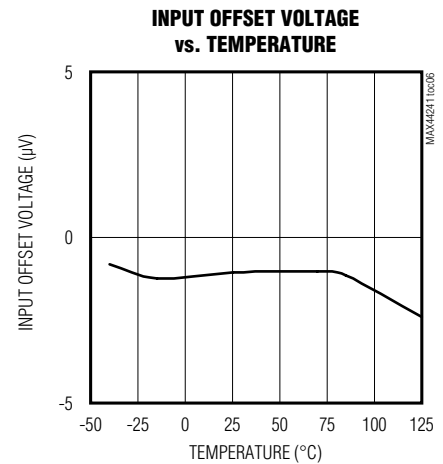
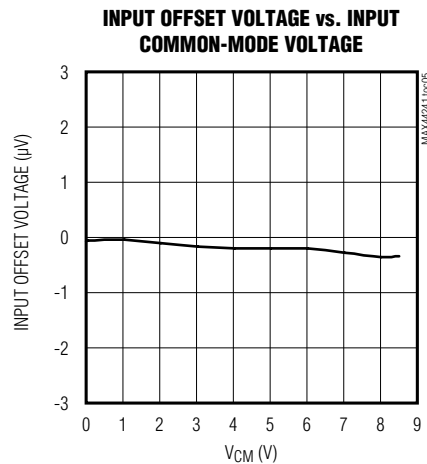
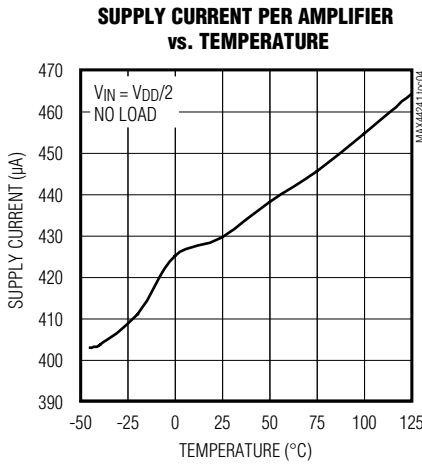
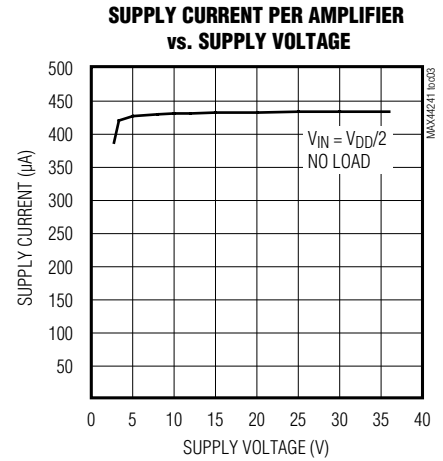
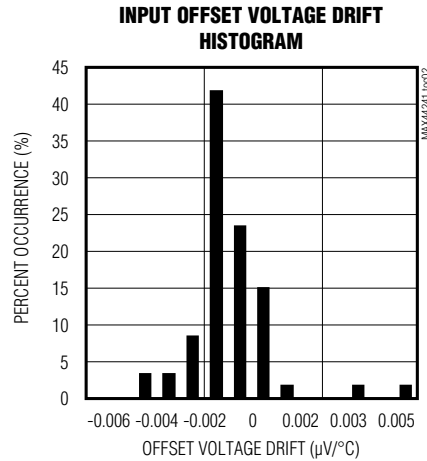
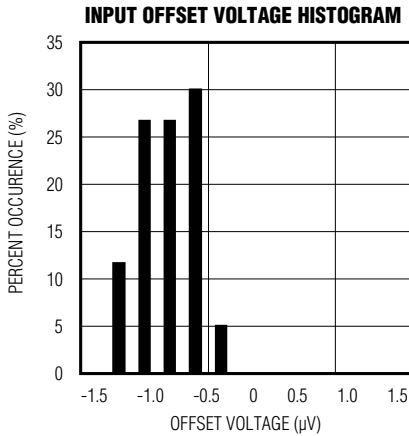
Note 4: Guaranteed by design.

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Typical Operating Characteristics

($V_{DD} = 10V$, $V_{GND} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 3)



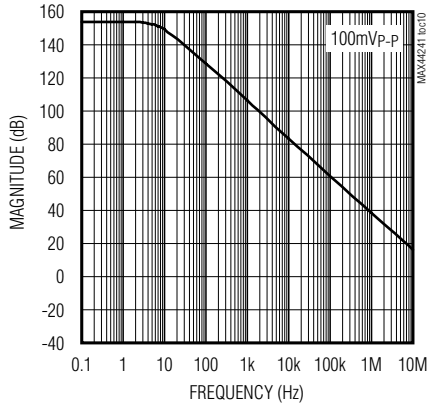
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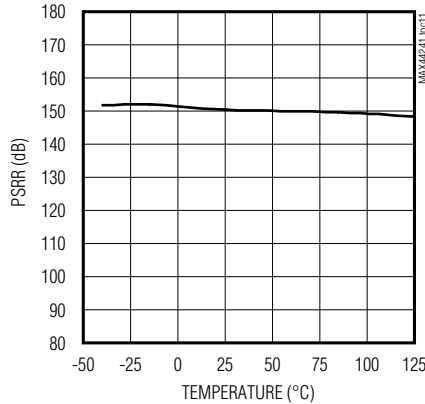
Typical Operating Characteristics (continued)

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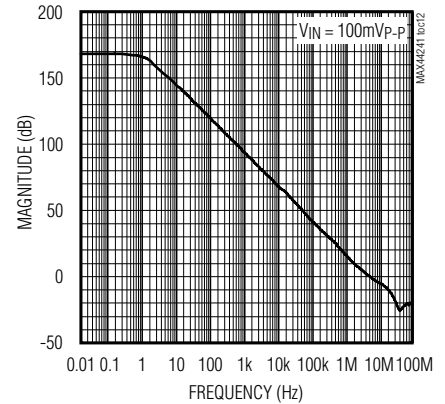
COMMON-MODE REJECTION RATIO vs. FREQUENCY



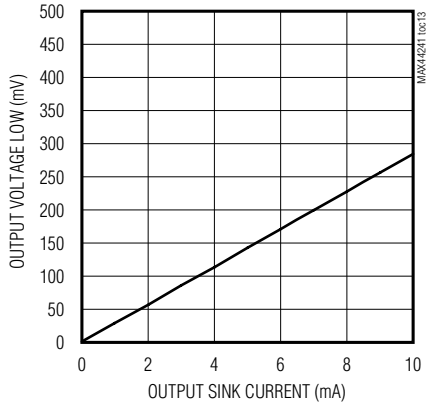
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



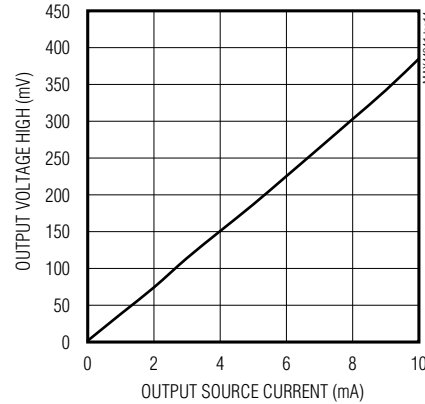
OPEN-LOOP GAIN vs. FREQUENCY



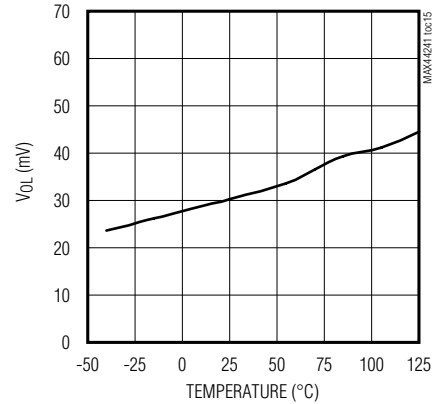
OUTPUT VOLTAGE LOW vs. OUTPUT SINK CURRENT



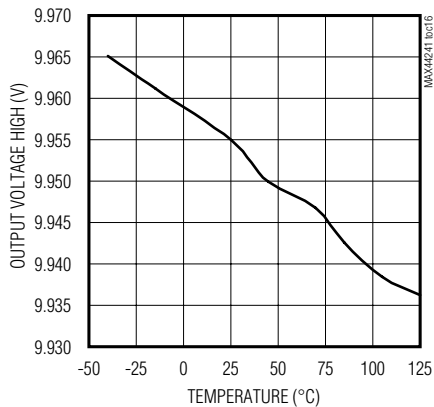
OUTPUT VOLTAGE HIGH vs. OUTPUT SOURCE CURRENT



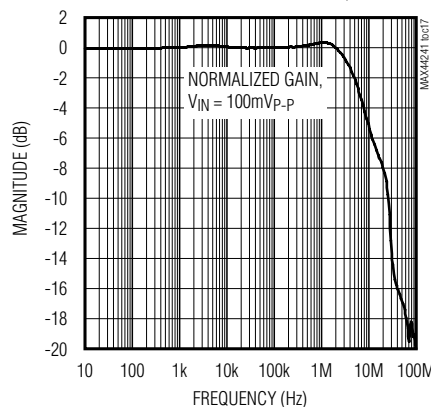
OUTPUT VOLTAGE LOW vs. TEMPERATURE



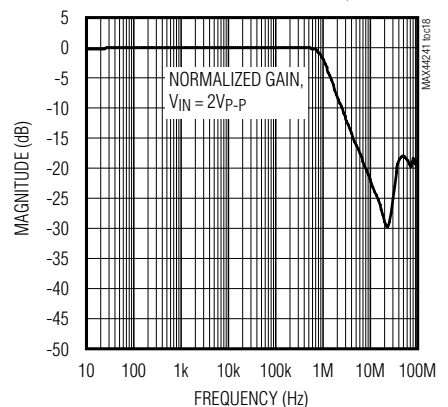
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



SMALL-SIGNAL GAIN vs. FREQUENCY



LARGE-SIGNAL GAIN vs. FREQUENCY

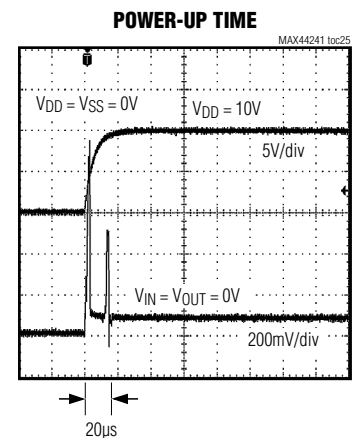
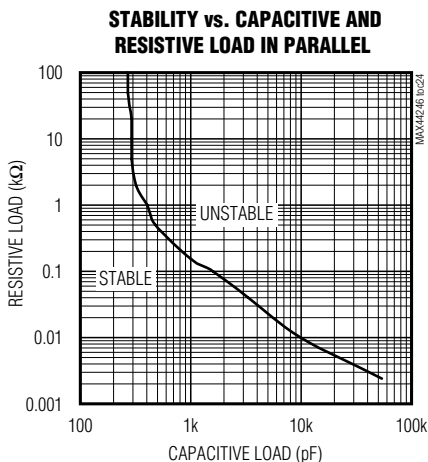
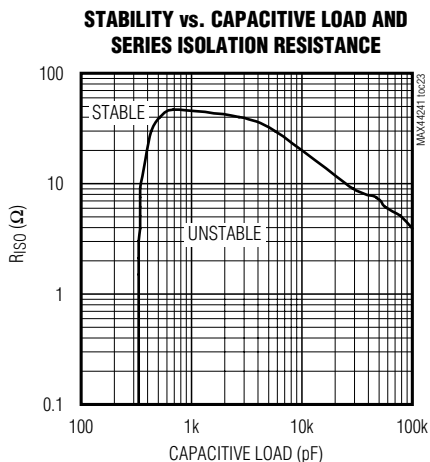
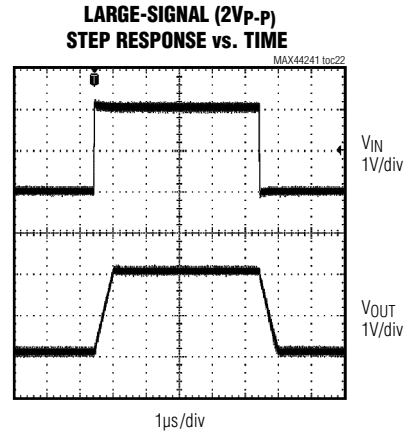
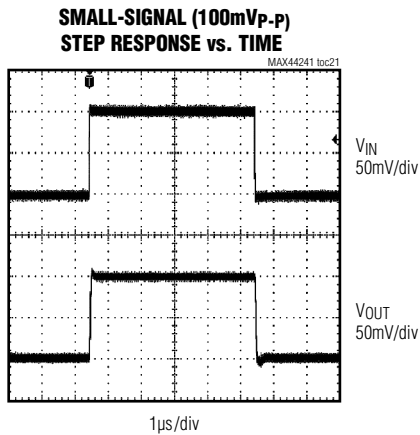
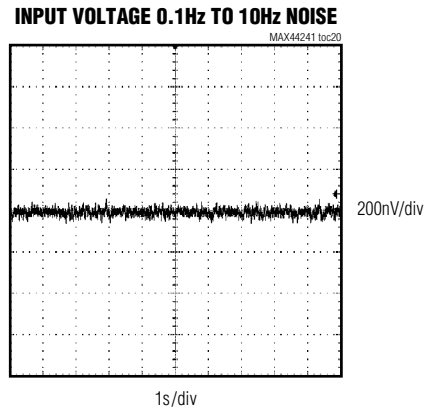
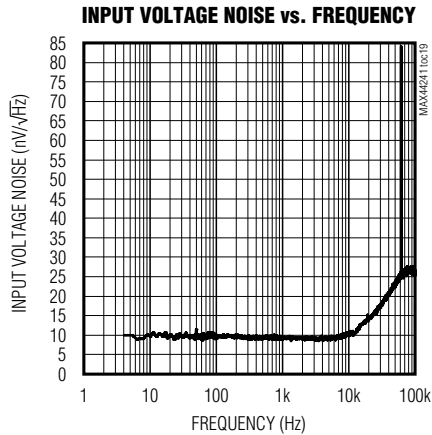


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Typical Operating Characteristics (continued)

($V_{DD} = 10V$, $V_{GND} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 3)

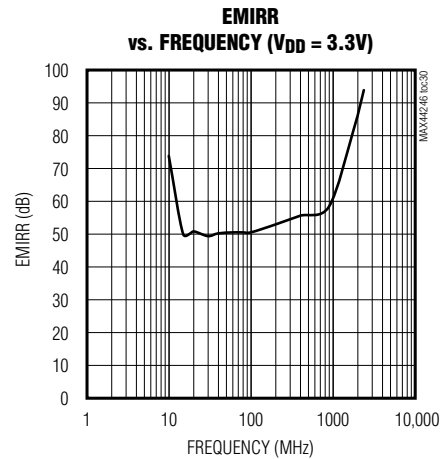
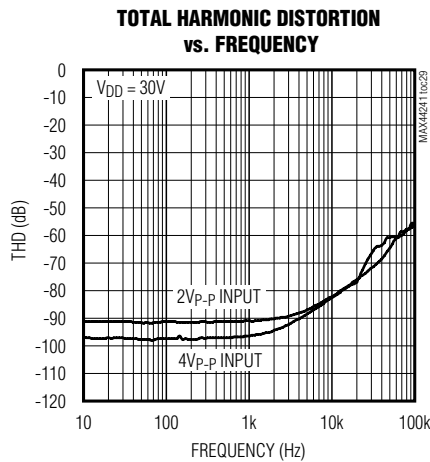
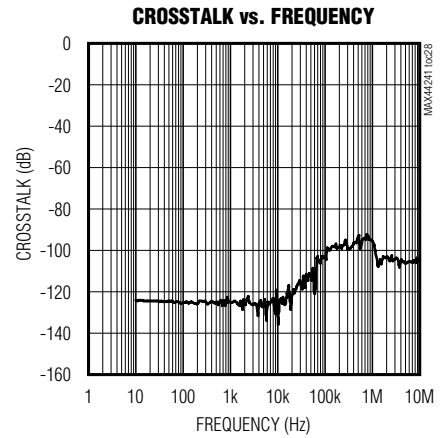
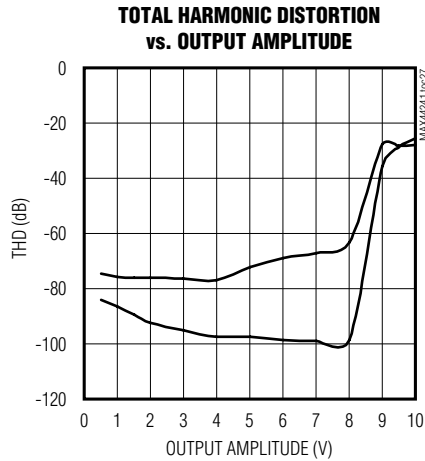
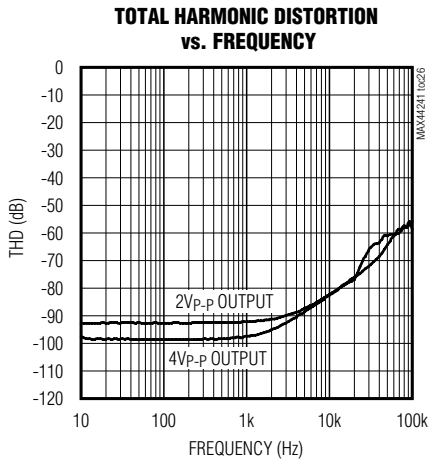


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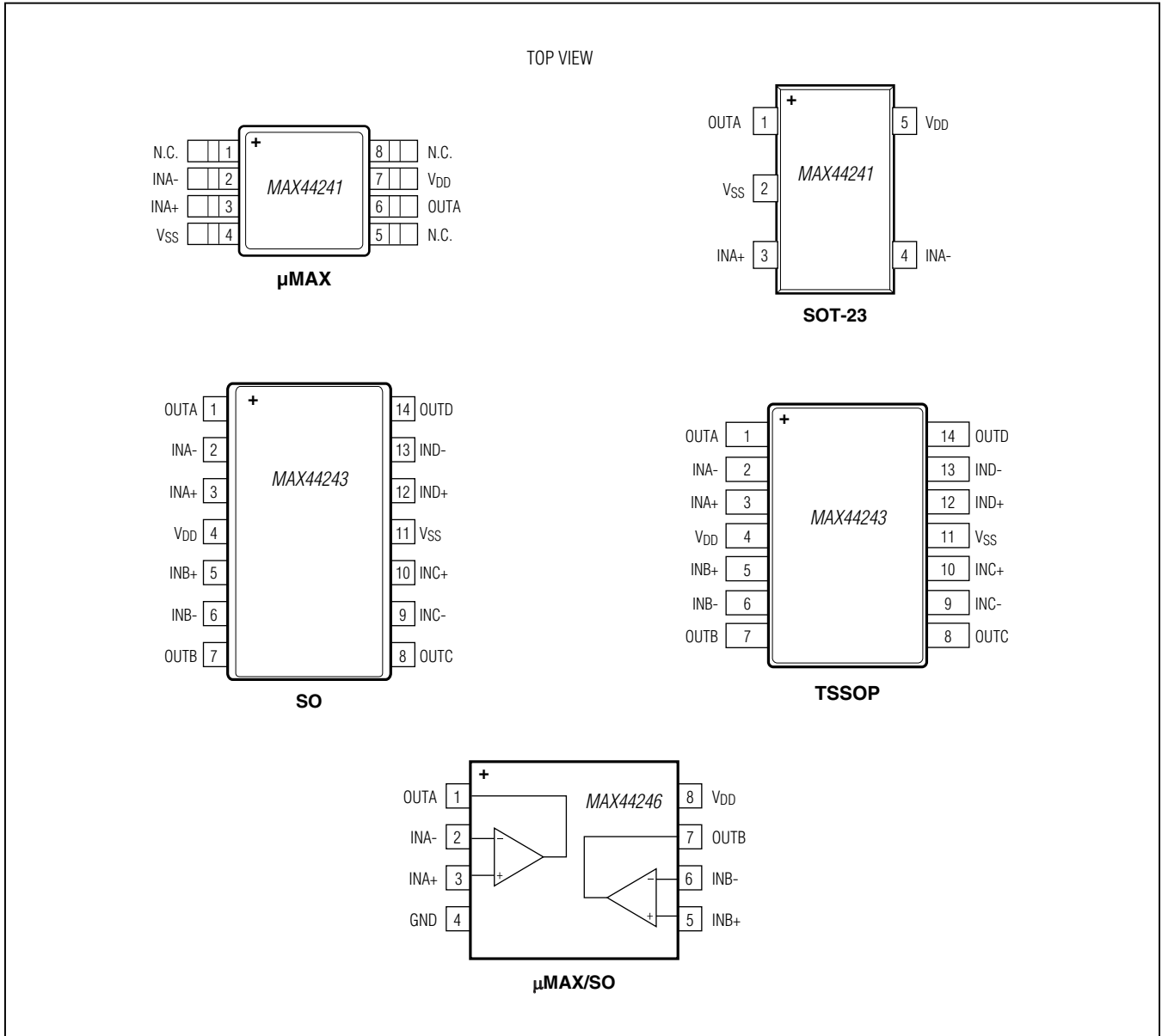
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Pin Configurations



MAX44241/MAX44243/MAX44246

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Pin Descriptions

PIN						NAME	FUNCTION
MAX44241		MAX44243		MAX44246			
SOT23-5	μMAX-8	SO-14	TSSOP-14	SO-8	μMAX-8		
1	6	1	1	1	1	OUTA	Channel A Output
2	4	11	11	4	4	V _{SS}	Negative Supply Voltage
3	3	3	3	3	3	INA+	Channel A Positive Input
4	2	2	2	2	2	INA-	Channel A Negative Input
5	7	4	4	8	8	V _{DD}	Positive Supply Voltage
—	—	5	5	5	5	INB+	Channel B Positive Input
—	—	6	6	6	6	INB-	Channel B Negative Input
—	—	7	7	7	7	OUTB	Channel B Output
—	—	8	8	—	—	OUTC	Channel C Output
—	—	9	9	—	—	INC-	Channel C Negative Input
—	—	10	10	—	—	INC+	Channel C Positive Input
—	—	12	12	—	—	IND+	Channel D Positive Input
—	—	13	13	—	—	IND-	Channel D Negative Input
—	—	14	14	—	—	OUTD	Channel D Output
—	1, 5, 8	—	—	—	—	N.C.	No Connection. Not internally connected.

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36V, Low-Noise, Precision, Single/Quad/Dual Op Amps

Detailed Description

The MAX44241/MAX44243/MAX44246 are high-precision amplifiers that provide below 5 μ V of maximum input-referred offset and low flicker noise. These characteristics are achieved by using a combination of proprietary auto-zeroing and chopper stabilized techniques. This combination of auto-zeroing and chopping ensures that these amplifiers give all the benefits of zero-drift amplifiers, while still ensuring low noise, minimizing chopper spikes, and providing wide bandwidth. Offset voltages due to power ripple/spikes as well as common-mode variation, are corrected resulting in excellent PSRR and CMRR specifications.

Noise Suppression

Flicker noise, inherent in all active devices, is inversely proportional to frequency present. Charges at the oxide-silicon interface that are trapped-and-released by MOSFET oxide occurs at low frequency more often. For this reason, flicker noise is also called 1/f noise. The MAX44241/MAX44243/MAX44246 eliminate the 1/f noise internally, thus making them ideal choices for DC or sub-Hz precision applications. The 1/f noise appears as a slow varying offset voltage and is eliminated by the chopping technique used.

Electromagnetic interference (EMI) noise occurs at higher frequency, resulting in malfunction or degradation of electrical equipment. The ICs have an input EMI filter to avoid the output being affected by radio frequency interference. The EMI filter composed of passive devices, presents significant higher impedance to higher frequency.

Applications Information

ADC Buffer Amplifier

The MAX44241/MAX44243/MAX44246 have low input offset voltage, low noise, and fast settling time that make these amplifiers ideal for ADC buffers. Weight scales are one application that often requires a low-noise, high-voltage amplifier in front of an ADC. The *Typical Operating*

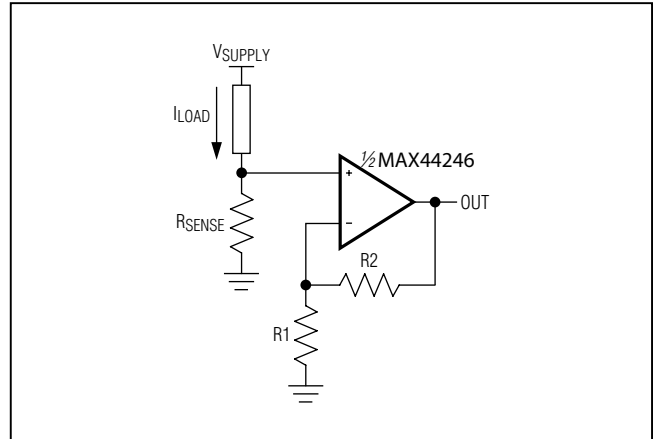


Figure 1. Low-Side Current Sensing

Circuit details an example of a load cell and amplifier driven from the same ± 10 V supplies, along with the MAX11211 18-bit delta sigma ADC. Load cells produce a very small voltage change at their outputs; therefore driving the excitation source with a higher voltage produces a wider dynamic range that can be measured at the ADC inputs.

The MAX11211 ADC operates from a single 2.7V to 3.6V analog supply, offers 18-bit noise-free resolution and 0.86mW power dissipation. The MAX11211 also offers > 100dB rejection at 50Hz and 60Hz. This ADC is part of a family of 16-, 18-, 20-, and 24-bit delta sigma ADCs with high precision and < 1mW power dissipation.

The low input offset voltage and low noise of MAX44241/MAX44243/MAX44246 allow a gain circuit to precede the MAX11211 without losing any dynamic range at the ADC. See the *Typical Operating Circuit*.

Precision Low-Side Current Sensing

The ICs' ultra-low offset voltage and drift make them ideal for precision current-sensing applications. Figure 1 shows the ICs in a low-side current-sense configuration. This circuit produces an accurate output voltage, V_{OUT} equal to $I_{LOAD} \times R_{SENSE} \times (1 + R_2/R_1)$.

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Layout Guidelines

The MAX44241/MAX44243/MAX44246 feature ultra-low offset voltage and noise. Therefore, to get optimum performance follow the following layout guidelines.

Avoid temperature gradients at the junction of two dissimilar metals. The most common dissimilar metals used on a PCB are solder-to-component lead and solder-to-board trace. Dissimilar metals create a local thermocouple. A variation in temperature across the board can cause an additional offset due to Seebeck effect at the solder junctions. To minimize the Seebeck effect, place the amplifier away from potential heat sources on the board, if possible. Orient the resistors such that both the ends are heated equally. It is a good practice to match the input signal path to ensure that the type and number of thermoelectric junctions remain the same. For example, consider using dummy 0Ω resistors oriented in such a way that the thermoelectric sources, due to the real resistors in the signal path, are cancelled. It is recommended to flood the PCB with ground plane. The ground plane ensures that heat is distributed uniformly reducing the potential offset voltage degradation due to Seebeck effect.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44241 AUA+	-40°C to +125°C	8 μ MAX	—
MAX44241AUK+	-40°C to +125°C	5 SOT23	AFMQ
MAX44243 ASD+	-40°C to +125°C	14 SO	—
MAX44243AUD+	-40°C to +125°C	14 TSSOP	—
MAX44246 ASA+	-40°C to +125°C	8 SO	—
MAX44246AUA+	-40°C to +125°C	8 μ MAX	—

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5+1	21-0057	90-0174
8 SO	S8+4	21-0041	90-0096
8 μ MAX	U8+1	21-0036	90-0092
14 SO	S14M+4	21-0041	90-0112
14 TSSOP	U14M+1	21-0066	90-0113

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	9/12	Revised the <i>Electrical Characteristics</i> and the <i>Typical Operating Characteristics</i> .	1, 2, 3, 5
2	2/13	Revised the <i>Typical Operating Characteristics</i> .	8
3	5/13	Updated <i>General Description</i> , <i>Typical Application Circuit</i> , and <i>Pin Description</i> .	1, 9
4	9/13	Added the MAX44241/MAX44243 to the data sheet. Revised the <i>Typical Operating Circuit</i> .	1–13
5	1/14	Revised <i>Electrical Characteristics</i> and the <i>Typical Operating Characteristics</i> .	2, 5
6	12/14	Revised <i>Benefits and Features</i> section.	1
7	4/15	Revised <i>Ordering Information</i>	13



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