

## FEATURES/BENEFITS

- 20 output, low skew clock signal buffer
- High drive FCT-type outputs
- Reduced swing TTL outputs for low noise
- Input hysteresis for better noise margin
- Monitor output
- Guaranteed low skew
  - 0.35ns output skew
  - 0.7ns pulse skew
  - 1.0ns part-to-part skew
- Available in 40-pin QVSOP (Q2)

## DESCRIPTION

The QS5820T clock driver/buffer circuits can be used for clock distribution schemes where low skew, high speed, and small footprint are primary concerns. The QS5820T offers four banks of five non-inverting outputs. Designed in QSI's proprietary QCMOS process, this device provides low propagation delay buffering with on-chip skew of 0.35ns for same-transition, same-bank signals. The QS5820T provides major skew advantages over octal type devices where total part-to-part skew ( $t_{SK(t)}$ ) of  $>1$  ns is unacceptable. Furthermore, board area consumed by the QVSOP package is almost one-third that of the typical SOIC package offered for octal devices. This clock buffer product is designed for use in high performance workstation, multi-board computing and telecommunications systems. The QS5820T is available in the 40-pin QVSOP package which offers the world's smallest logic footprint.

**Figure 1. Functional Block Diagram and Pinout**

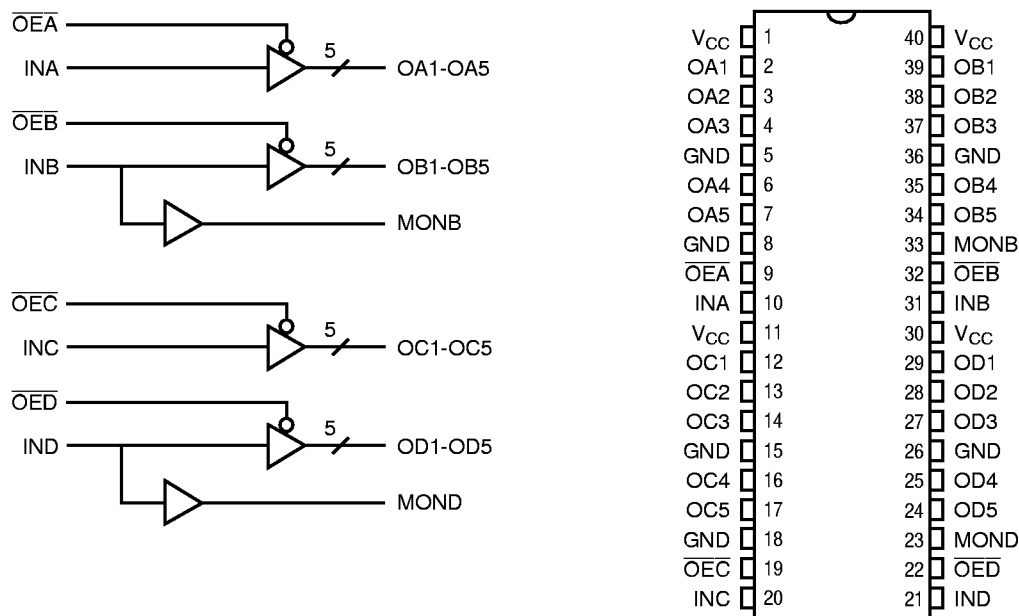


Table 1. Pin Descriptions

Pin Name	I/O	Description
$\overline{OEA}$ , $\overline{OEB}$ , $\overline{OEC}$ , $\overline{OED}$	I	Output Enable Inputs
INA, INB, INC, IND	I	Clock Inputs
OAn, OBn, OCn, ODn	O	Clock Outputs
MONB, MOND	O	Non-disable Monitor Outputs

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Table 2. Absolute Maximum Ratings

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Switch Voltage $V_S$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation .....	1.2 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	QVSOP		Unit
	Typ	Max	
All Pins	5	8	pF

**Note:** Capacitance is characterized but not tested.

Table 4. Recommended Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Power Supply Voltage	4.75	5.25	V
$V_{IN}$	Input Voltage	0	5.5	V
$V_{OUT}$	Voltage Applied to Outputs	0	5.5	V
$T_A$	Ambient Operating Temperature	0	70	°C

**Table 5. DC Electrical Characteristics Over Operating Range**

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH for Inputs	2.0	—	—	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW for Inputs	—	—	0.8	V
V <sub>IC</sub>	Clamp Diode Voltage <sup>(3)</sup>	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -24mA	2.4	—	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 64mA	—	—	0.55	V
I <sub>IN</sub>	Input Leakage Current	V <sub>CC</sub> = Max., 0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	—	—	1	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>CC</sub> = Max., Outputs High-Z	—	—	1	μA
I <sub>OS</sub>	Short Circuit Current <sup>(2,3)</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND	-60	—	—	mA

**Notes:**

1. Typical values indicate V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.
2. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
3. Guaranteed by design but not tested.

**Table 6. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ <sup>(3)</sup>	Max	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND or V <sub>CC</sub>	0.4	3.0	mA
ΔI <sub>CC</sub>	Supply Current per Input HIGH	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V, f <sub>I</sub> = 0MHz	0.5	2.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current per Output <sup>(2)</sup>	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub> or V <sub>IN</sub> = GND Outputs enabled, 50% duty cycle	0.1	0.2	mA/ MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Guaranteed but not tested.
3. Typical values are for reference only. Conditions are V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.
4. I<sub>C</sub> = I<sub>CC</sub> + (ΔI<sub>CC</sub>)(D<sub>H</sub>)(N<sub>T</sub>) + I<sub>CCD</sub> (f<sub>O</sub>)(N<sub>O</sub>)

where:

D<sub>H</sub> = Input duty cycle

N<sub>T</sub> = Number of TTL HIGH inputs at D<sub>H</sub>

f<sub>O</sub> = Output frequency

N<sub>O</sub> = Number of outputs at f<sub>O</sub>

Table 7. Skew Characteristics Over Operating Range

Symbol	Description <sup>(1,2)</sup>	A		B		Unit
		Min	Max	Min	Max	
$t_{SK(O1)}$	Skew between two outputs same transition, same bank	—	0.5	—	0.35	ns
$t_{SK(O2)}$	Skew between two outputs same transition, different banks	—	0.7	—	0.5	ns
$t_{SK(p)}$	Duty cycle distortion (pulse skew) on a single output opposite transitions ( $t_{PHL}-t_{PLH}$ )	—	1.0	—	0.7	ns
$t_{SK(t)}$	Part-to-part skew same transition <sup>(3)</sup>	—	1.5	—	1.0	ns

**Notes:**

1. Skew parameters are guaranteed across temperature range, but not production tested. Skew parameters apply to propagation delays only.
2. See Test Circuit and Waveforms.
3.  $t_{SK(t)}$  only applies to Quality Semiconductor devices of the same transition, same  $V_{CC}$ , same temperature, same speed grade, and same loading.

Table 8. Switching Characteristics Over Operating Range

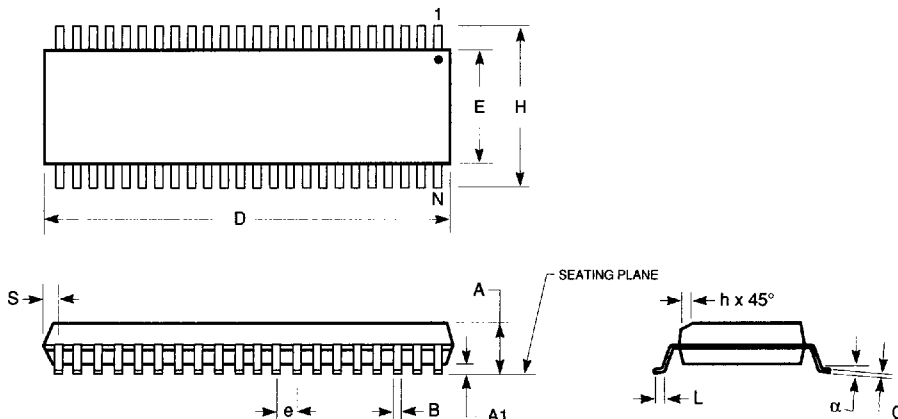
$C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$ .

Symbol	Description <sup>(1)</sup>	A		B		Unit
		Min	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Propagation Delay <sup>(1, 2)</sup>	1.5	5.8	1.5	5.0	ns
$t_R$	Output Rise Time, 0.8V to 2.0V	—	1.5	—	1.5	ns
$t_F$	Output Fall Time, 2.0V to 0.8V	—	1.5	—	1.5	ns
$t_{PZL}$ , $t_{PZH}$	Output Enable Time	1.5	8.0	1.5	7.0	ns
$t_{PLZ}$ , $t_{PZH}$	Output Disable Time <sup>(3)</sup>	1.5	7.0	1.5	6.0	ns

**Notes:**

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.
3. Guaranteed by design but not tested.

**150-MIL QVSOP™ - Package Code Q1/Q2**  
**150-Mil Wide Plastic Small Outline Gull-Wing**



JEDEC#	MO-154BB			MO-154AB		
DWG#	PSS-40A (Q2)			PSS-48A (Q1)		
Symbol	Min	Nom	Max	Min	Nom	Max
A	0.059	0.065	0.069	0.059	0.065	0.069
A1	0.004	0.006	0.008	0.004	0.006	0.008
B	0.0067	0.008	0.009	0.0051	0.0063	0.008
C	0.0075	0.008	0.0098	0.0075	0.008	0.0098
D	0.386	0.390	0.394	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157
e	0.0197 BSC, 0.5mm			0.0157 BSC, 0.4mm		
H	0.228	0.236	0.244	0.228	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016
L	0.020	0.024	0.030	0.020	0.024	0.030
N	40			48		
$\alpha$	0°	5°	8°	0°	5°	8°
S	0.006	0.008	0.010	0.012	0.014	0.016

**Notes:**

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.003in. maximum.

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