

N-Channel 8-V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a) ^a Q _g (Typ.)						
8	0.011 at V _{GS} = 4.5 V	12							
	0.013 at V _{GS} = 2.5 V	12							
	0.016 at V _{GS} = 1.8 V	12	19 nC						
	0.022 at V _{GS} = 1.5 V	12							
	0.041 at V _{GS} = 1.2 V	12							

FEATURES

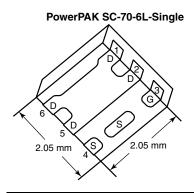
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

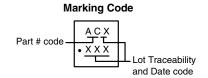


HALOGEN FREE

APPLICATIONS

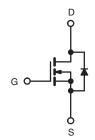
Load Switch for Portable Applications





Ordering Information:

SiA414DJ-T4-GE3 (Lead (Pb)-free and Halogen-free) SiA414DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

Parameter		Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	8	V			
Gate-Source Voltage	V_{GS}	± 5	v			
	T _C = 25 °C		12 ^a			
Continuous Drain Current (T _{.I} = 150 °C)	$T_C = 70 ^{\circ}C$	I _D	12 ^a			
Continuous Brain Current (1) = 100 °C)	T _A = 25 °C	טי	12 ^{a, b, c}			
	T _A = 70 °C		11.6 ^{b, c}	A		
Pulsed Drain Current	I _{DM}	40				
Continuous Source-Drain Diode Current	T _C = 25 °C		12 ^a			
Continuous Source-Diam Diode Current	T _A = 25 °C	Is	2.9 ^{b, c}			
	T _C = 25 °C		19			
Maximum Power Dissipation	T _C = 70 °C	P _D	12	w		
Maximum Fower Dissipation	T _A = 25 °C	ט' ד	3.5 ^{b, c}	VV		
	T _A = 70 °C		2.2 ^{b, c}			
Operating Junction and Storage Temperatur	T _J , T _{stg}	- 55 to 150	°C			
Soldering Recommendations (Peak Tempera	ature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5	O/ VV				

Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishav.com/ppg273257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
 e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

SiA414DJ

Vishay Siliconix



SPECIFICATIONS ($T_J = 25 ^{\circ}\text{C}$,		•			T				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static	T		I	1	1	I			
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	8			V			
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		9		mV/°(
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 3		,			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	0.35		0.8	V			
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 100	nA			
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 8 V, V _{GS} = 0 V			1	μΑ			
Zoro dato voltago Brain Garrent	.055	$V_{DS} = 8 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10				
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			Α			
		$V_{GS} = 4.5 \text{ V}, I_D = 9.7 \text{ A}$		0.009	0.011	1			
		$V_{GS} = 2.5 \text{ V}, I_D = 9 \text{ A}$		0.011	0.013				
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 1.8 V, I _D = 8.1 A		0.013	0.016	Ω			
		$V_{GS} = 1.5 \text{ V}, I_D = 4.5 \text{ A}$		0.016	0.022				
		V _{GS} = 1.2 V, I _D = 2.4 A		0.027	0.041	1			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 4 V, I _D = 9.7 A		50		S			
Dynamic ^b	l		L	L	<u> </u>				
Input Capacitance	C _{iss}			1800		pF			
Output Capacitance	C _{oss}	$V_{DS} = 4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		650					
Reverse Transfer Capacitance	C _{rss}			450					
Tatal Cata Chausa	0	$V_{DS} = 4 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 10 \text{ A}$		21	32	nC			
Total Gate Charge	Qg	V _{DS} = 4 V, V _{GS} = 4.5 V, I _D = 10 A		19	29				
Gate-Source Charge	Q_{gs}			2.5					
Gate-Drain Charge	Q_{gd}			6.5					
Gate Resistance	R_g	f = 1 MHz		2.5		Ω			
Turn-on Delay Time	t _{d(on)}			12	20				
Rise Time	t _r	, , , , , , , , , , , , , , , , , , ,		10	15				
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 4 \text{ V}, R_L = 0.4 \Omega$ $I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_q = 1 \Omega$		65	100				
Fall Time	t _f	$ID = 10 \text{ A}, VGEN = 4.5 \text{ V}, H_g = 1.52$		20	30				
Turn-on Delay Time	t _{d(on)}			10	15	ns			
Rise Time	t _r	<u>-</u>		10	15				
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 4 \text{ V}, R_L = 0.4 \Omega$ $I_D \cong 10 \text{ A}, V_{GEN} = 5 \text{ V}, R_g = 1 \Omega$		35	55	1			
Fall Time				10	15	1			
Drain-Source Body Diode Characteristic				<u> </u>	<u> </u>	1			
Continuous Source-Drain Diode Current	Continuous Source-Drain Diode Current I _S				12				
Pulse Diode Forward Current					40	A .			
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V		0.8	1.2	٧			
Body Diode Reverse Recovery Time	t _{rr}			40	80	ns			
Body Diode Reverse Recovery Charge	Q _{rr}	·		20	40	nC			
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		12					
Reverse Recovery Rise Time	t _b	1		28	1	ns			

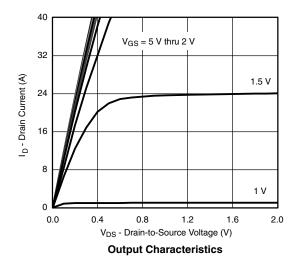
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

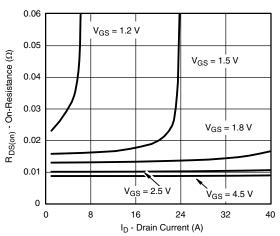
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing.

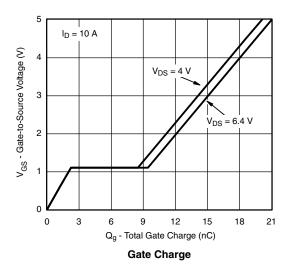


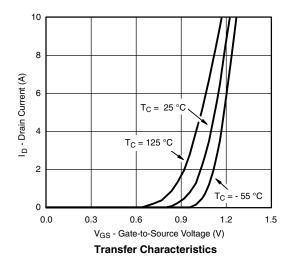
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

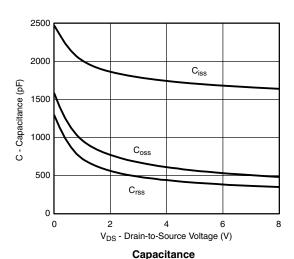


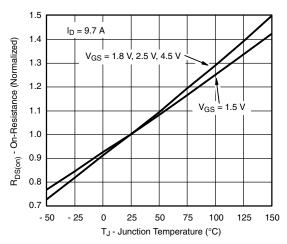


On-Resistance vs. Drain Current and Gate Voltage



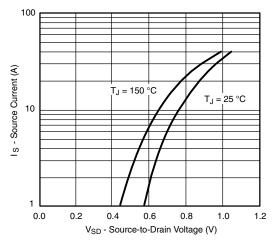




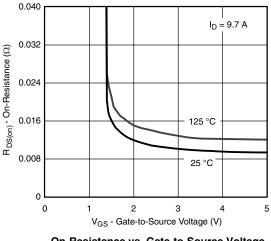


On-Resistance vs. Junction Temperature

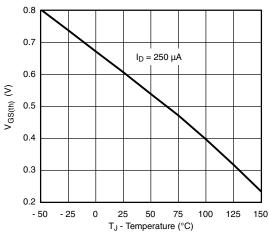
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



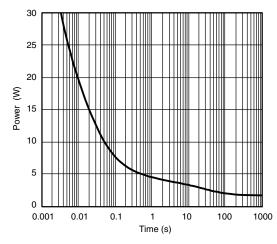
Source-Drain Diode Forward Voltage



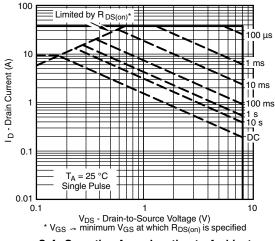
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



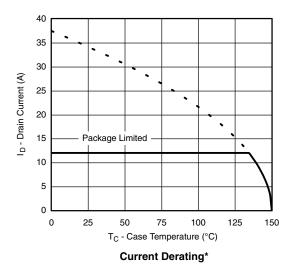
Safe Operating Area, Junction-to-Ambient

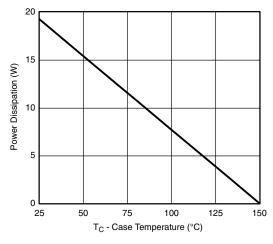






TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



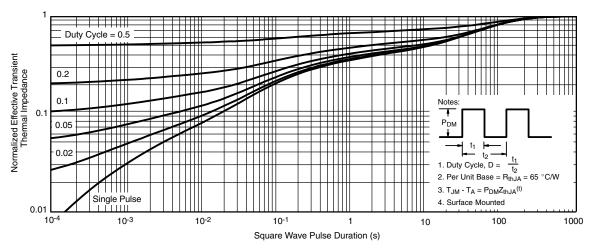


Power Derating

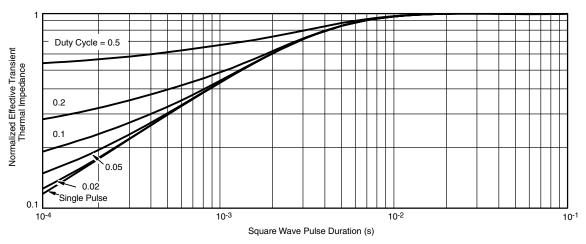
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73954.





PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

	SINGLE PAD						DUAL PAD					
DIM	M	ILLIMETER	RS	INCHES MILLIMETERS		RS	INCHES					
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP			0.011 TYP		0.275 TYP		0.011 TYP			
K1		0.400 TYP			0.016 TYP		0.320 TYP		0.013 TYP			
K2		0.240 TYP		0.009 TYP		0.252 TYP		0.010 TYP				
К3		0.225 TYP		0.009 TYP					•	•		
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

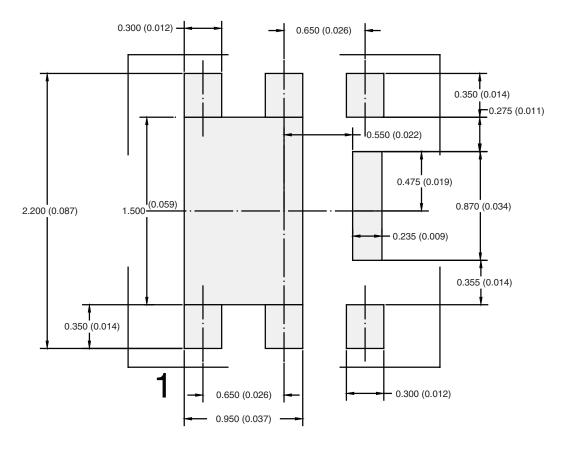
ECN: C-07431 - Rev. C, 06-Aug-07

DWG: 5934

06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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