

# 2SJ652 — P-Channel Silicon MOSFET

## General-Purpose Switching Device

### Applications

#### Features

- ON-resistance  $R_{DS(on)1}=28.5m\Omega$ (typ.)
- Input capacitance  $C_{iss}=4360pF$  (typ.)
- 4V drive

#### Specifications

##### Absolute Maximum Ratings at $T_a=25^\circ C$

| Parameter                          | Symbol    | Conditions                                | Ratings     | Unit       |
|------------------------------------|-----------|---|-------------|------------|
| Drain-to-Source Voltage            | $V_{DSS}$ |   | -60         | V          |
| Gate-to-Source Voltage             | $V_{GSS}$ |   | $\pm 20$    | V          |
| Drain Current (DC)                 | $I_D$     |   | -28         | A          |
| Drain Current (Pulse)              | $I_{DP}$  | $PW \leq 10\mu s$ , duty cycle $\leq 1\%$ | -112        | A          |
| Allowable Power Dissipation        | PD        |   | 2.0         | W          |
|                                    |           | $T_c=25^\circ C$                          | 30          | W          |
| Channel Temperature                | $T_{ch}$  |   | 150         | $^\circ C$ |
| Storage Temperature                | $T_{stg}$ |   | -55 to +150 | $^\circ C$ |
| Avalanche Energy (Single Pulse) *1 | $E_{AS}$  |   | 343         | mJ         |
| Avalanche Current *2               | $I_{AV}$  |   | -28         | A          |

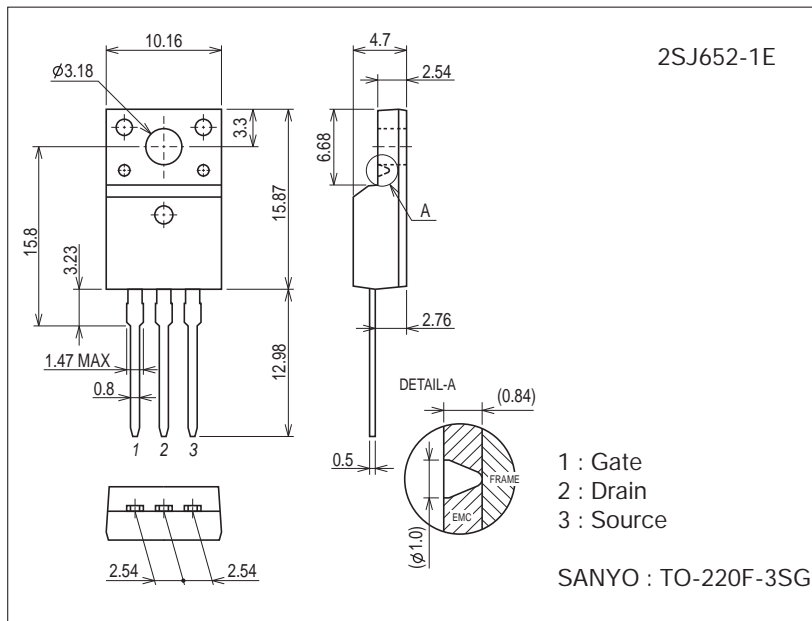
Note : \*1  $V_{DD}=-30V$ ,  $L=500\mu H$ ,  $I_{AV}=-28A$  (Fig.1)

\*2  $L \leq 500\mu H$ , single pulse

#### Package Dimensions

unit : mm (typ)

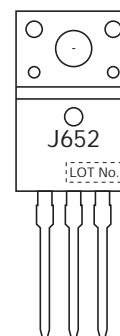
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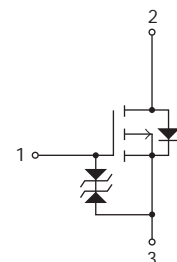
#### Product & Package Information

- Package : TO-220F-3SG
- JEITA, JEDEC : SC-67
- Minimum Packing Quantity : 50 pcs./magazine

#### Marking



#### Electrical Connection



# 2SJ652

## Electrical Characteristics at Ta=25°C

| Parameter                                  | Symbol               | Conditions   | Ratings                                   |      |       | Unit |
|--|----------------------|--|---|------|-------|------|
|  |                      |  | min                                       | typ  | max   |      |
| Drain-to-Source Breakdown Voltage          | V(BR)DSS             | I <sub>D</sub> =-1mA, V <sub>GS</sub> =0V                          | -60                                       |      |       | V    |
| Zero-Gate Voltage Drain Current            | I <sub>DSS</sub>     | V <sub>DS</sub> =-60V, V <sub>GS</sub> =0V                         |   |      | -1    | μA   |
| Gate-to-Source Leakage Current             | I <sub>GSS</sub>     | V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V                         |   |      | ±10   | μA   |
| Cutoff Voltage                             | V <sub>GS(off)</sub> | V <sub>DS</sub> =-10V, I <sub>D</sub> =-1mA                        | -1.2                                      |      | -2.6  | V    |
| Forward Transfer Admittance                | y <sub>fs</sub>      | V <sub>DS</sub> =-10V, I <sub>D</sub> =-14A                        | 18  | 26   |       | S    |
| Static Drain-to-Source On-State Resistance | R <sub>DS(on)1</sub> | I <sub>D</sub> =-14A, V <sub>GS</sub> =-10V                        |   | 28.5 | 38    | mΩ   |
|  | R <sub>DS(on)2</sub> | I <sub>D</sub> =-14A, V <sub>GS</sub> =-4V                         |   | 39   | 55.5  | mΩ   |
| Input Capacitance                          | C <sub>iss</sub>     | V <sub>DS</sub> =-20V, f=1MHz                                      |   | 4360 |       | pF   |
| Output Capacitance                         | C <sub>oss</sub>     |  |   | 470  |       | pF   |
| Reverse Transfer Capacitance               | C <sub>rss</sub>     |  |   | 335  |       | pF   |
| Turn-ON Delay Time                         | t <sub>d(on)</sub>   |  | See Fig.2                                 |      | 33    |      |
| Rise Time                                  | t <sub>r</sub>       |  |   | 210  |       | ns   |
| Turn-OFF Delay Time                        | t <sub>d(off)</sub>  |  |   | 310  |       | ns   |
| Fall Time                                  | t <sub>f</sub>       |  |   | 180  |       | ns   |
| Total Gate Charge                          | Q <sub>g</sub>       | V <sub>DS</sub> =-30V, V <sub>GS</sub> =-10V, I <sub>D</sub> =-28A |   |      | 80    |      |
| Gate-to-Source Charge                      | Q <sub>gs</sub>      |  |   | 15   |       | nC   |
| Gate-to-Drain "Miller" Charge              | Q <sub>gd</sub>      |  |   | 12   |       | nC   |
| Diode Forward Voltage                      | V <sub>SD</sub>      |  | I <sub>S</sub> =-28A, V <sub>GS</sub> =0V |      | -0.96 | -1.2 |

Fig.1 Avalanche Resistance Test Circuit

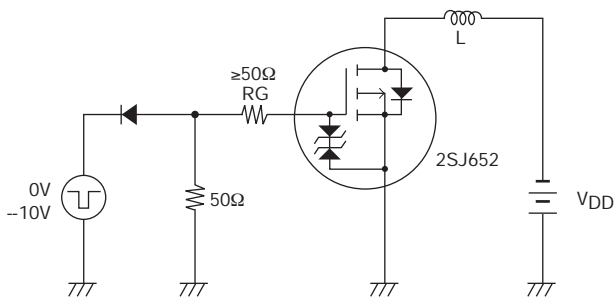
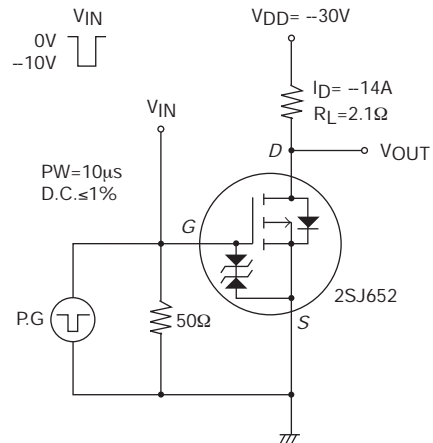
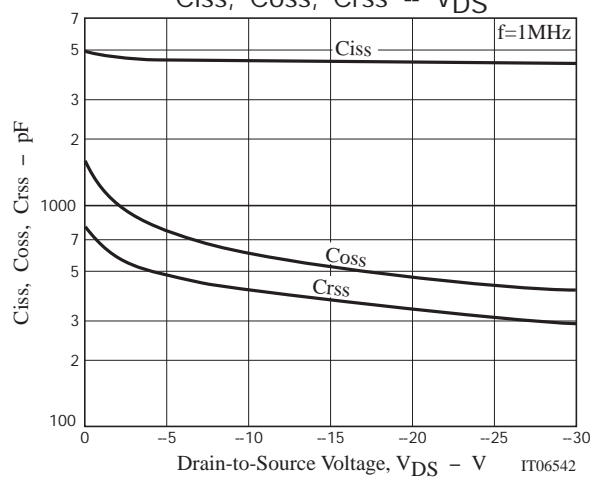
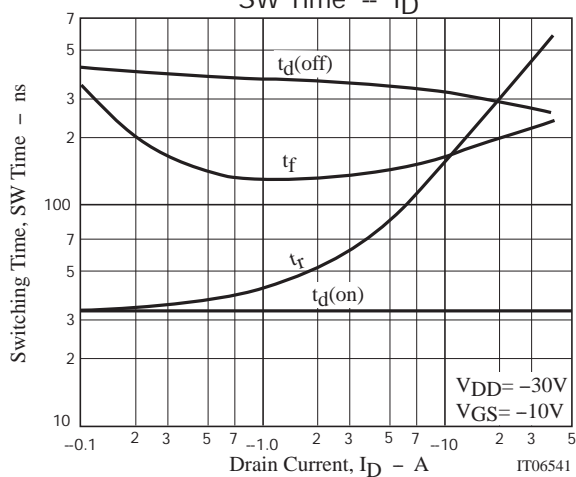
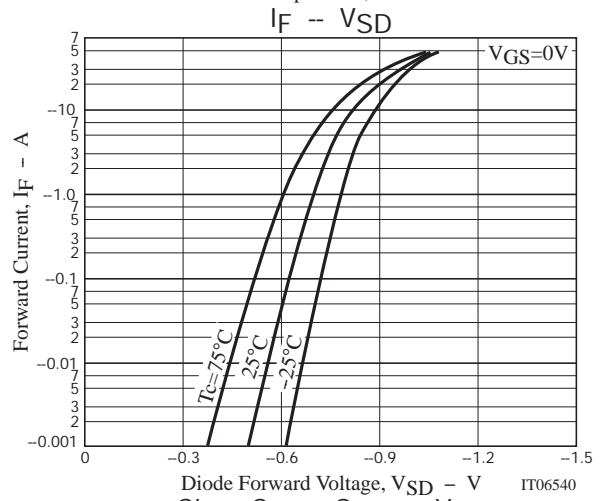
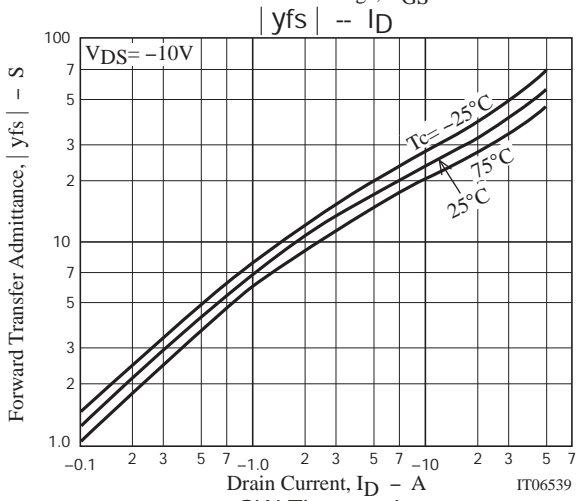
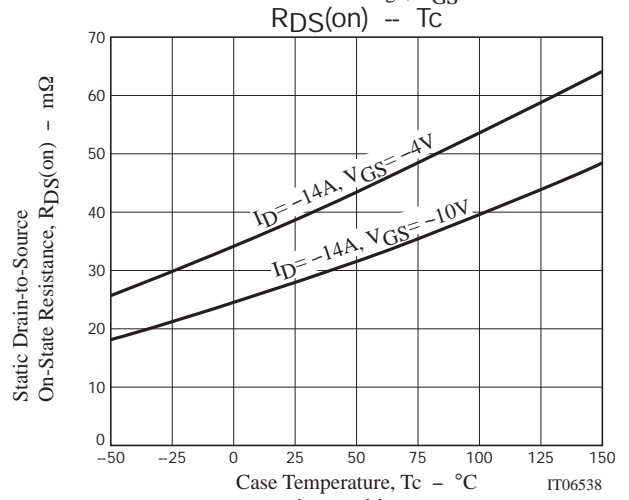
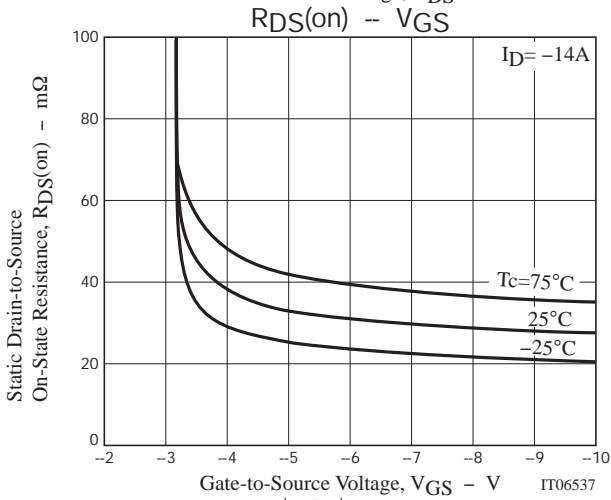
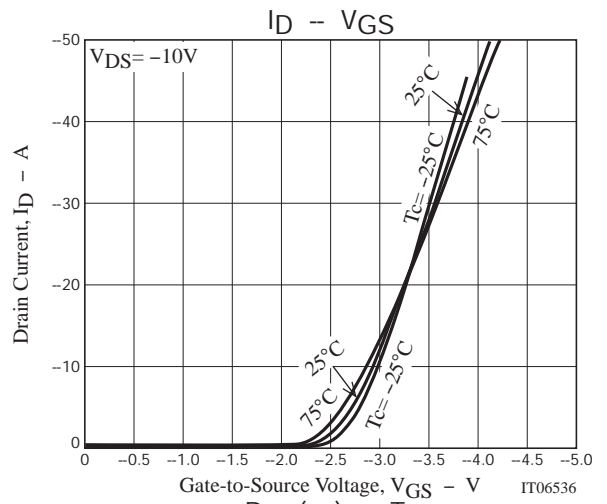
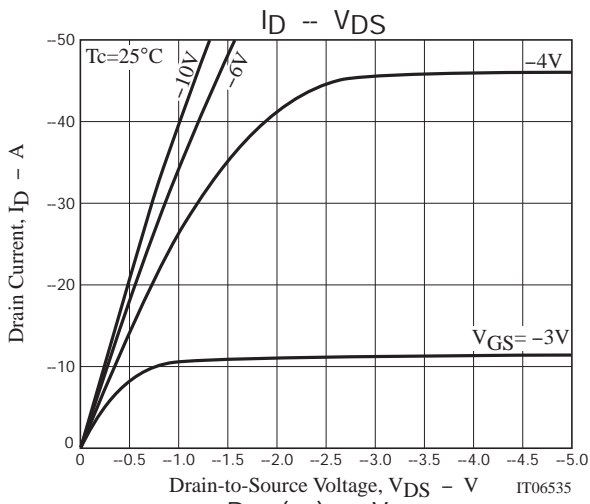


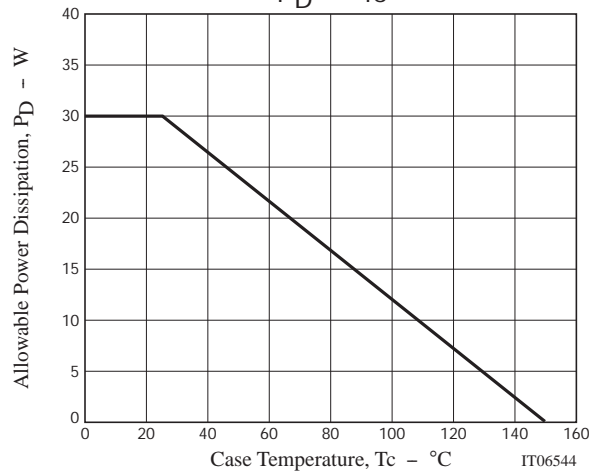
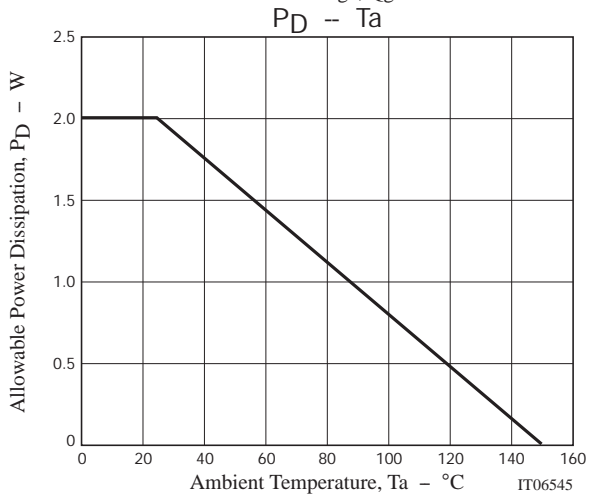
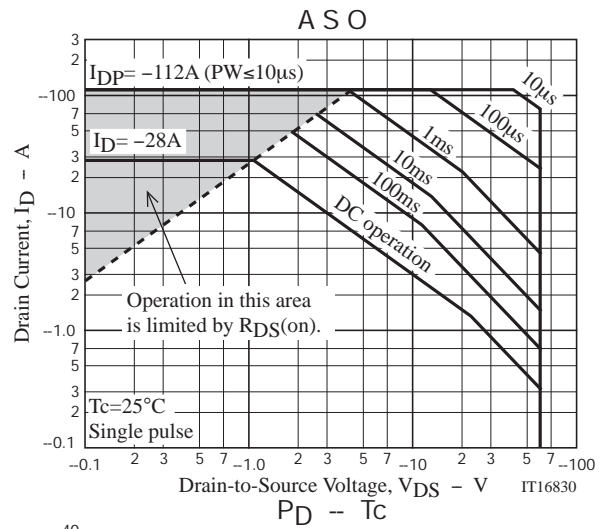
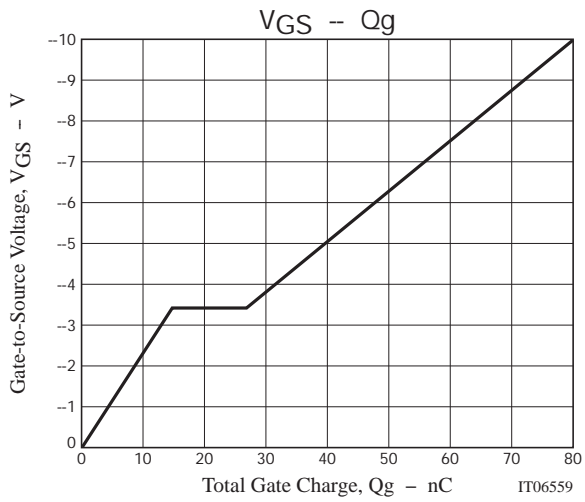
Fig.2 Switching Time Test Circuit



## Ordering Information

| Device    | Package     | Shipping        | memo    |
|-----------|-------------|-----------------|---------|
| 2SJ652-1E | TO-220F-3SG | 50pcs./magazine | Pb Free |





Magazine Specification

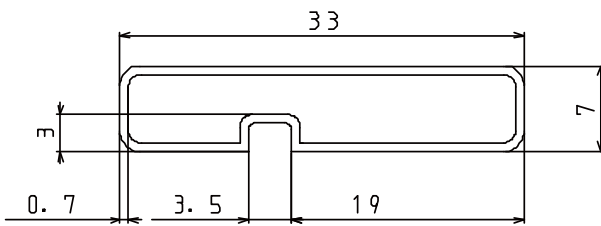
2SJ652-1E

1. Packing Format

| Package Name | Magazine Name | Maximum Number of devices contained (pcs) |           |           | Packing format   |  |
|--------------|---------------|---|-----------|-----------|--|--|
|              |               | Magazine                                  | Inner box | Outer box | Inner BOX  | Outer BOX  |
| TO-220F-3SG  | TO-220F       | 50  | 1,000     | 4,000     | SPD-0V0001<br>20 magazines contained<br>Dimensions:mm (external)<br>568×150×55 | SPT-081029<br>4 inner boxes contained<br>Dimensions:mm (external)<br>590×225×178 |

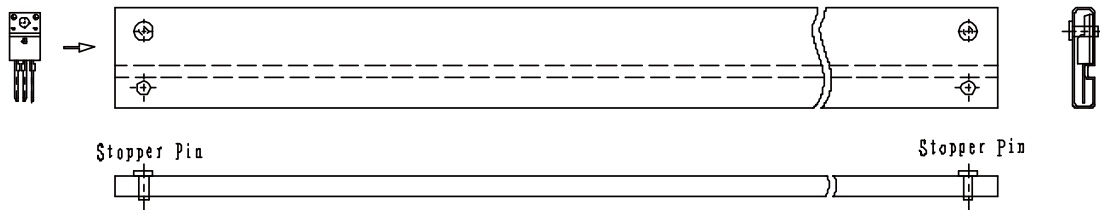
2. Magazine dimensions

(unit:mm)

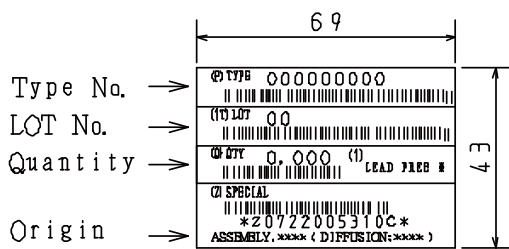


Tolerance=±0.3mm  
 Thickness=0.7±0.2mm  
 Length =532.5±2mm  
 Material =PVC (Antistatic treatment)

3. Storage method to magazine

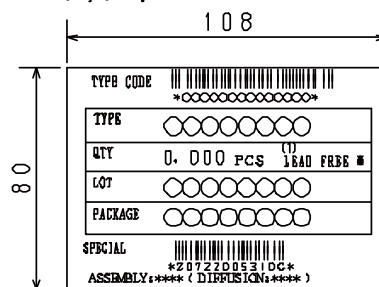


4. Inner box label (unit:mm)



5. Outer box label (unit:mm)

It is a label at the time of factory shipments.  
 The form of a label may change in physical  
 distribution process.



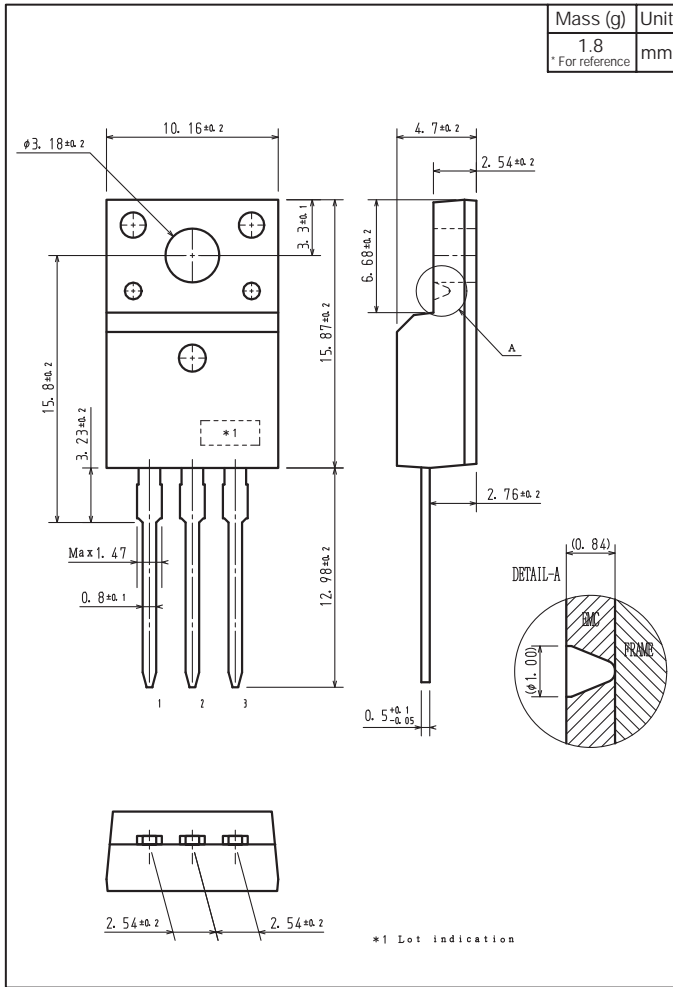
NOTE (1)

The LEAD FREE \* description shows that the surface treatment of the terminal is lead free.

| Label       | JEITA Phase    |
|-------------|----------------|
| LEAD FREE 3 | JEITA Phase 3A |

Outline Drawing

2SJ652-1E



Note on usage : Since the 2SJ652 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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