

# IRFP450, IRFP451, IRFP452, IRFP453

12A and 14A, 450V and 500V, 0.4 and 0.5 Ohm,  
N-Channel Power MOSFETs

January 1998

## Features

- 12A and 14A, 450V and 500V
- $r_{DS(ON)} = 0.4\Omega$  and  $0.5\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

## Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFP450	TO-247	IRFP450
IRFP451	TO-247	IRFP451
IRFP452	TO-247	IRFP452
IRFP453	TO-247	IRFP453

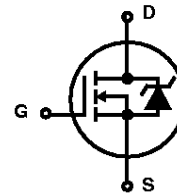
NOTE: When ordering, use the entire part number.

## Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

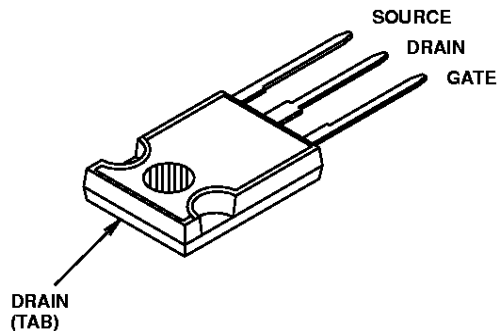
Formerly developmental type TA17435.

## Symbol



## Packaging

JEDEC STYLE TO-247



## IRFP450, IRFP451, IRFP452, IRFP453

### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	IRFP450	IRFP451	IRFP452	IRFP453	UNITS
Drain to Source Voltage (Note 1) . . . . . $V_{DS}$	500	450	500	450	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . . $V_{DGR}$	500	450	500	450	V
Continuous Drain Current . . . . . $I_D$	14	14	12	12	A
$T_C = 100^\circ\text{C}$ . . . . . $I_D$	8.8	8.8	7.9	7.9	A
Pulsed Drain Current (Note 3) . . . . . $I_{DM}$	56	56	48	48	A
Gate to Source Voltage . . . . . $V_{GS}$	$\pm 20$	$\pm 20$	$\pm 20$	$\pm 20$	V
Maximum Power Dissipation . . . . . $P_D$	180	180	180	180	W
Linear Derating Factor . . . . .	1.44	1.44	1.44	1.44	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4) . . . . . $E_{AS}$	860	860	860	860	mJ
Operating and Storage Temperature . . . . . $T_J, T_{STG}$	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . $T_L$	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . . $T_{pkg}$	260	260	260	260	$^\circ\text{C}$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**

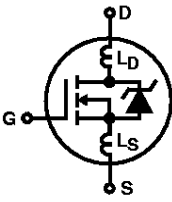
- $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

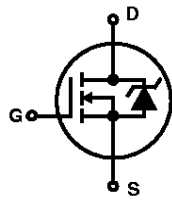
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRFP450, IRFP452	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 10)	500	-	-	V
			IRFP451, IRFP453	450	-	-
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2.0	-	4.0	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^\circ\text{C}$	-	-	250	$\mu\text{A}$
On-State Drain Current (Note 2) IRFP450, IRFP451	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$ , $V_{GS} = 10\text{V}$	14	-	-	A
			IRFP452, IRFP453	12	-	-
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
On Resistance (Note 2) IRFP450, IRFP451	$r_{DS(ON)}$	$I_D = 7.9\text{A}$ , $V_{GS} = 10\text{V}$ (Figures 8, 9)	-	0.3	0.4	$\Omega$
			IRFP452, IRFP453	-	0.4	0.5
Forward Transconductance (Note 2)	$g_{fs}$	$V_{DS} \geq 50\text{V}$ , $I_D = 7.9\text{A}$ (Figure 12)	9.3	13.8	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 250\text{V}$ , $I_D \approx 14\text{A}$ , $V_{GS} = 10\text{V}$ , $R_G = 6.1\Omega$ , $R_L = 17.4\Omega$ (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	27	ns
Rise Time	$t_r$		-	45	66	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	68	100	ns
Fall Time	$t_f$		-	41	60	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_g(\text{TOT})$	$V_{GS} = 10\text{V}$ , $I_D \approx 14\text{A}$ , $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{G(REF)} = 1.5\text{mA}$ (Figures 14, 19, 20) Gate Charge is Essentially Independent of Oper- ating Temperature	-	82	130	nC
Gate to Source Charge	$Q_{gs}$		-	12	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$		-	42	-	nC

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### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 11)		-	2000	-	pF
Output Capacitance	$C_{OSS}$			-	400	-	pF
Reverse Transfer Capacitance	$C_{RSS}$			-	100	-	pF
Internal Drain Inductance	$L_D$	Measured From the Contact Screw on Header Closer to Source and Gate Pins to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	$L_S$	Measured From the Source Lead, 6.0mm (0.25in) From Header to Source Bonding Pad		-	12.5	-	nH
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	0.70	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^\circ\text{C/W}$

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	$I_{SD}$	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 	-	-	14	A	
Pulse Source to Drain Current (Note 3)	$I_{SDM}$		-	-	56	A	
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_{SD} = 14\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 13)		-	-	1.4	V
Reverse Recovery Time	$t_{rr}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = 13\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	1300	-	ns
Reverse Recovery Charge	$Q_{RR}$	$T_J = 150^\circ\text{C}$ , $I_{SD} = 13\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	7.4	-	$\mu\text{C}$

#### NOTES:

2. Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4.  $V_{DD} = 50\text{V}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 7.9\text{mH}$ ,  $R_G = 25\Omega$ , peak  $I_{AS} = 14\text{A}$ . (Figures 15, 16)

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## Typical Performance Curves Unless Otherwise Specified

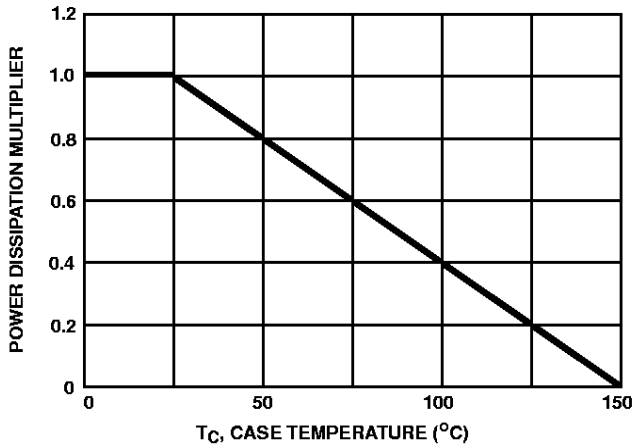


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

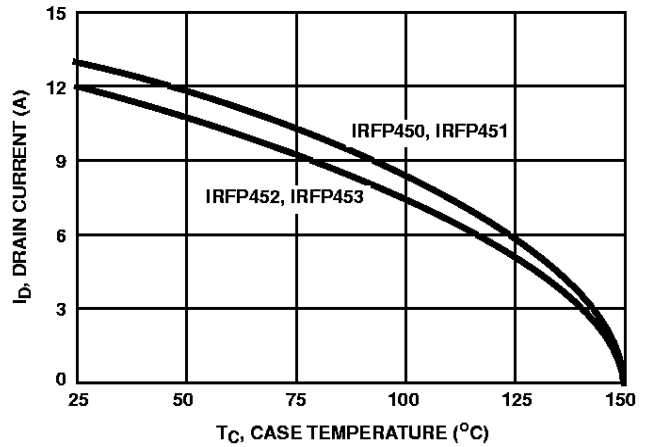


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

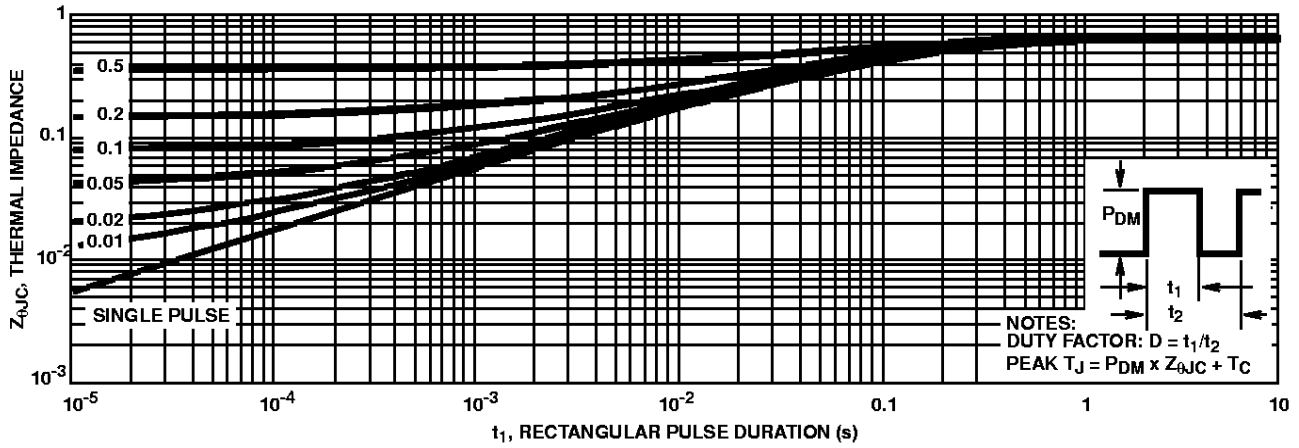


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

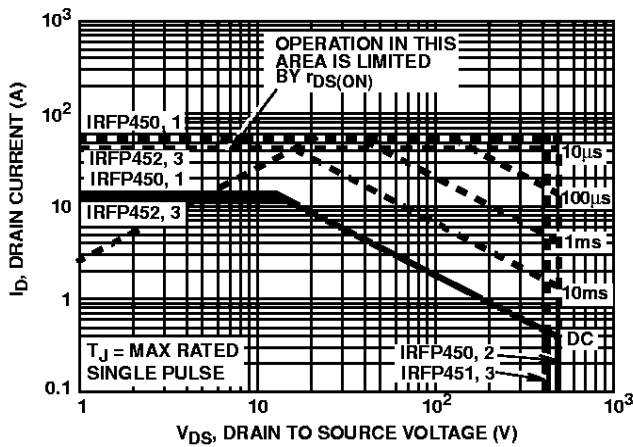


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

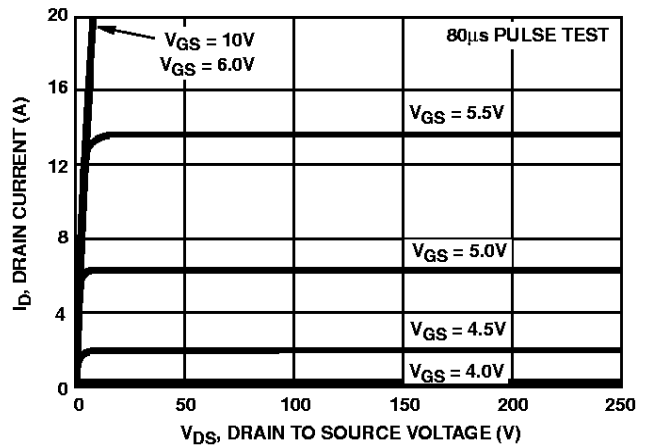


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

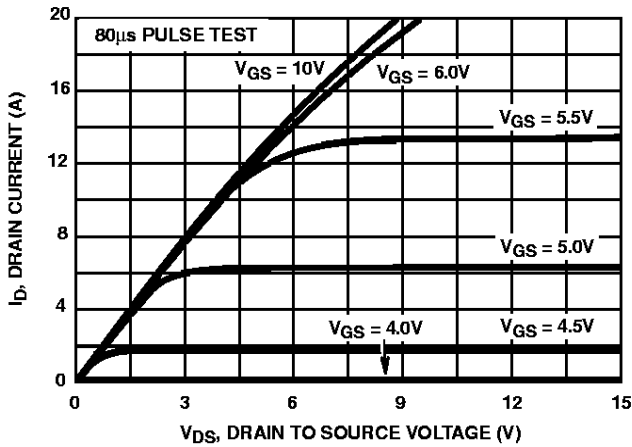


FIGURE 6. SATURATION CHARACTERISTICS

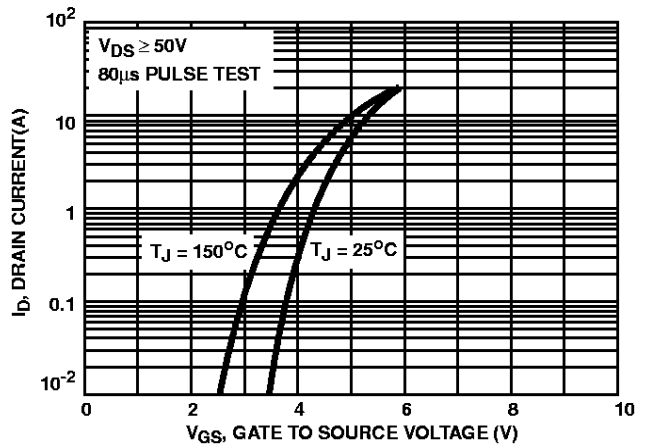
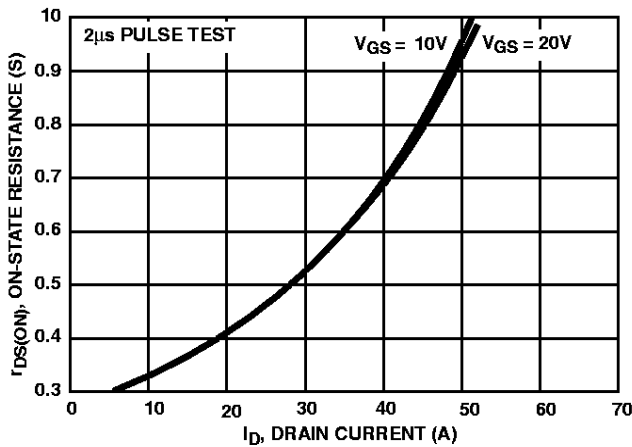


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2µs is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

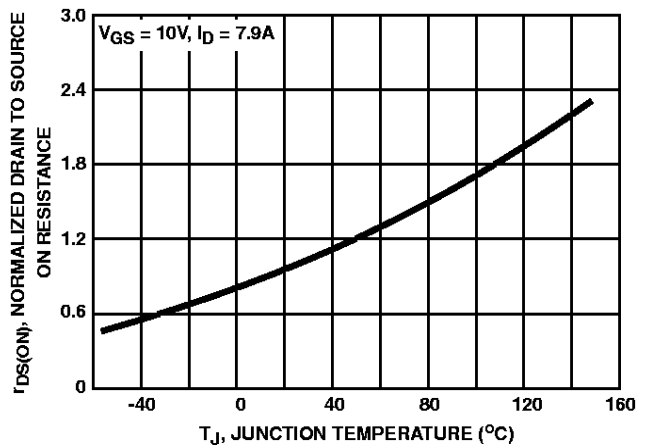


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

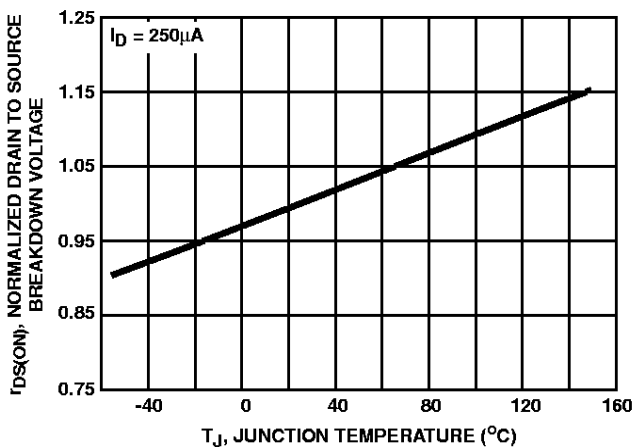


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

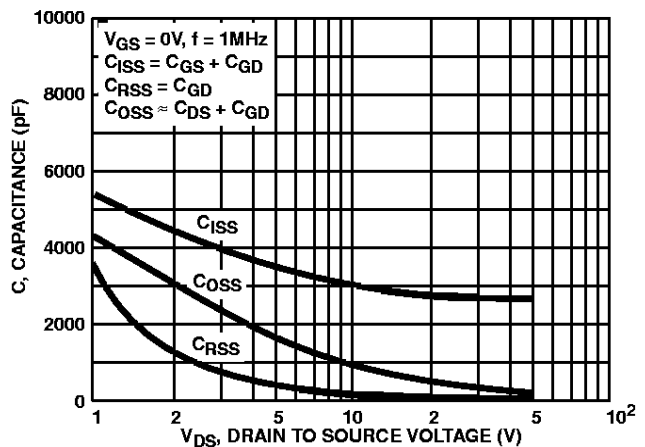


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

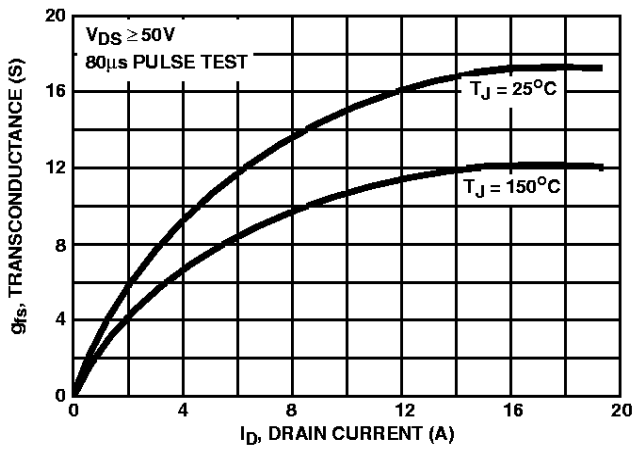


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

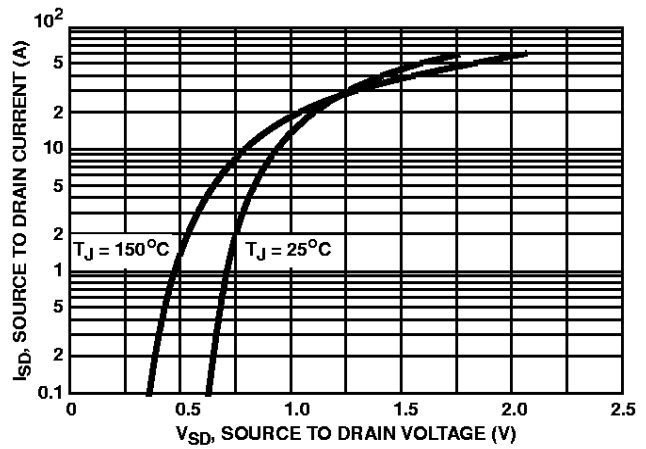


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

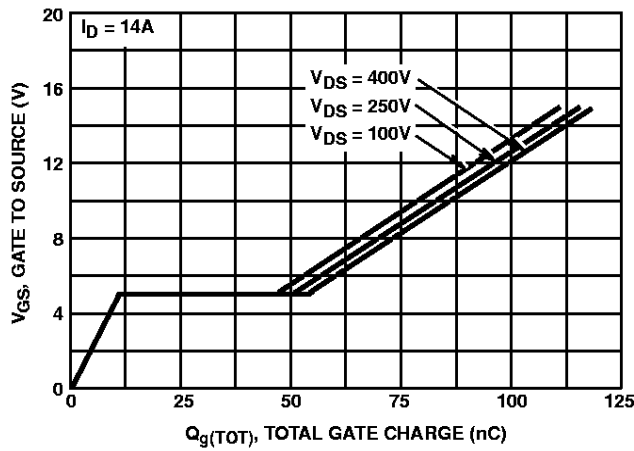


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

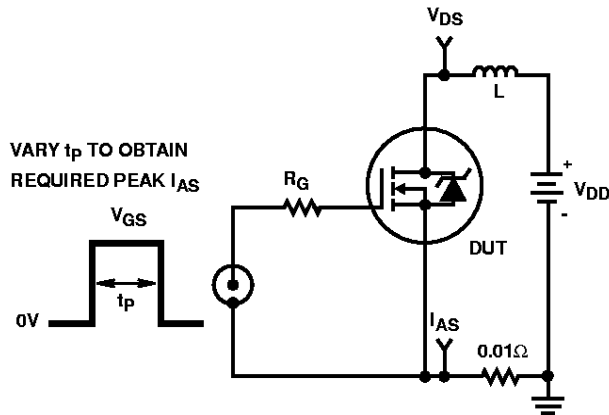


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

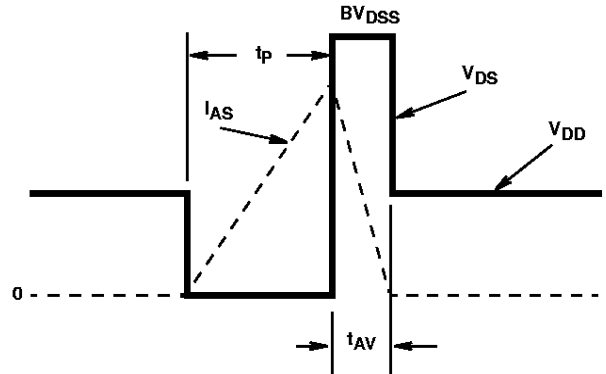


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

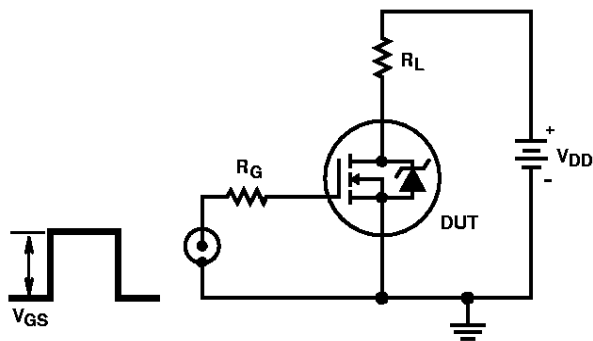


FIGURE 17. SWITCHING TIME TEST CIRCUIT

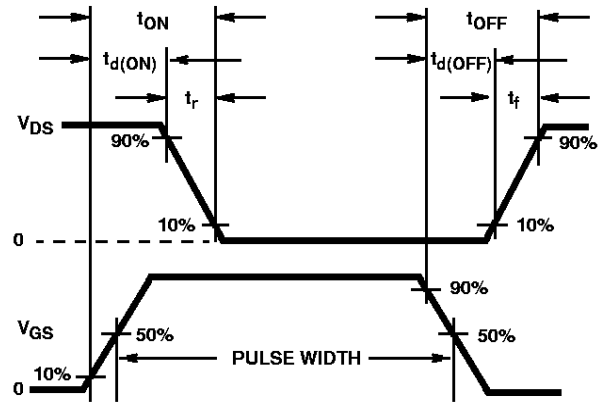


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

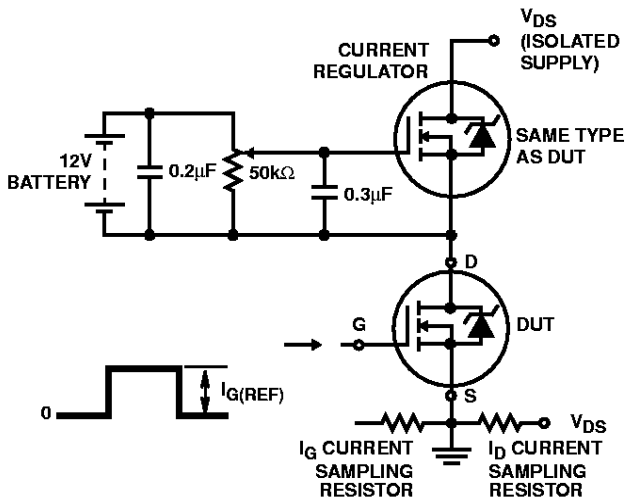


FIGURE 19. GATE CHARGE TEST CIRCUIT

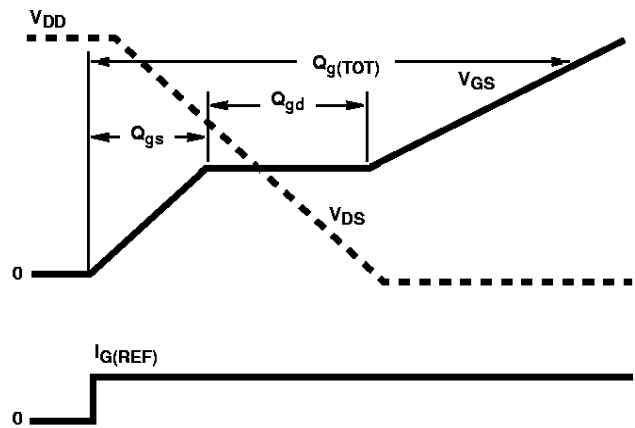


FIGURE 20. GATE CHARGE WAVEFORMS