

1K Microwire Serial EEPROM with EUI-48™ Node Identity

Device Selection Table

| Part Number | Vcc Range | Word Size | Temp. Ranges | Packages | Node Address |
|-------------|-----------|-----------|--------------|----------|--------------|
| 93AA46AE48 | 1.8V-5.5V | 8-bit | I | SN, OT | EUI-48™ |

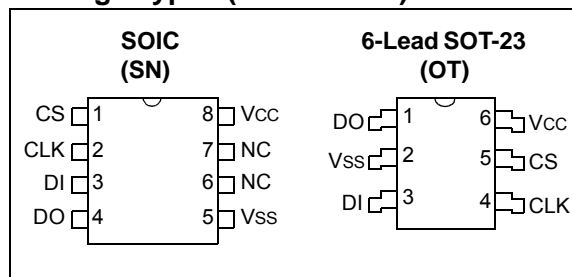
Features

- Preprogrammed Globally Unique 48-Bit Node Address
- Compatible with EUI-48™ and EUI-64™
- Compatible with LAN9210, LAN9211, LAN9215, LAN9217, LAN9218, LAN9220, LAN9221
- Low-Power CMOS Technology
- 128 x 8-Bit Organization
- Self-Timed Erase/Write Cycles (including Auto-Erase)
- Automatic Erase All (ERAL) before Write All (WRAL)
- Power-On/Off Data Protection Circuitry
- Industry Standard 3-Wire Serial I/O
- Device Status Signal (Ready/Busy)
- Sequential Read Function
- 1,000,000 Erase/Write Cycles
- Data Retention: >200 Years
- RoHS Compliant
- Temperature Ranges Supported:
 - Industrial (I): -40°C to +85°C

Description

The Microchip Technology Inc. 93AA46AE48 device is a 1 Kbit low-voltage Serial Electrically Erasable PROM (EEPROM) featuring an 8-bit word size. Advanced CMOS technology makes this device ideal for low-power, nonvolatile memory applications. The 93AA46AE48 is available in standard 8-lead SOIC and 6-lead SOT-23 packages.

Package Types (not to scale)



Pin Function Table

| Name | Function |
|------|------------------------|
| CS | Chip Select |
| CLK | Serial Data Clock |
| DI | Serial Data Input |
| DO | Serial Data Output |
| Vss | Ground |
| NC | No Internal Connection |
| Vcc | Power Supply |

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

| | |
|---|--------------------------------|
| V _{CC} | 7.0V |
| All inputs and outputs w.r.t. V _{SS} | -0.6V to V _{CC} +1.0V |
| Storage temperature | -65°C to +150°C |
| Ambient temperature with power applied..... | -40°C to +85°C |
| ESD protection on all pins..... | ≥4 kV |

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

| DC CHARACTERISTICS | | | Electrical Characteristics: Industrial (I): TA = -40°C to +85°C, V _{CC} = +1.8V to +5.5V | | | | |
|--------------------|---------------------------------------|---|--|------|---------------------|-------|---|
| Param. No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| D1 | V _{IH1} | High-Level Input Voltage | 2.0 | — | V _{CC} +1 | V | V _{CC} ≥ 2.7V |
| | V _{IH2} | | 0.7 V _{CC} | — | V _{CC} +1 | V | V _{CC} < 2.7V |
| D2 | V _{IL1} | Low-Level Input Voltage | -0.3 | — | 0.8 | V | V _{CC} ≥ 2.7V |
| | V _{IL2} | | -0.3 | — | 0.2 V _{CC} | V | V _{CC} < 2.7V |
| D3 | V _{OL1} | Low-Level Output Voltage | — | — | 0.4 | V | I _{OL} = 2.1 mA, V _{CC} = 4.5V |
| | V _{OL2} | | — | — | 0.2 | V | I _{OL} = 100 μA, V _{CC} = 2.5V |
| D4 | V _{OH1} | High-Level Output Voltage | 2.4 | — | — | V | I _{OH} = -400 μA, V _{CC} = 4.5V |
| | V _{OH2} | | V _{CC} - 0.2 | — | — | V | I _{OH} = -100 μA, V _{CC} = 2.5V |
| D5 | I _{LI} | Input Leakage Current | — | — | ±1 | μA | V _{IN} = V _{SS} or V _{CC} |
| D6 | I _{LO} | Output Leakage Current | — | — | ±1 | μA | V _{OUT} = V _{SS} or V _{CC} |
| D7 | C _{IN} , C _{OUT} | Pin Capacitance (all inputs/outputs) | — | — | 7 | pF | V _{IN} /V _{OUT} = 0V (Note 1) TA = 25°C, F _{CLK} = 1 MHz |
| D8 | I _{CCWRITE} | Write Current | — | — | 2 | mA | V _{CC} = 5.5V |
| | | | — | 500 | — | μA | V _{CC} = 2.5V |
| D9 | I _{CCREAD} | Read Current | — | — | 1 | mA | F _{CLK} = 2 MHz, V _{CC} = 5.5V |
| | | | — | — | 500 | μA | F _{CLK} = 2 MHz, V _{CC} = 3.0V |
| | | | — | 100 | — | μA | F _{CLK} = 2 MHz, V _{CC} = 2.5V |
| D10 | I _{CCS} | Standby Current | — | — | 1 | μA | CLK = CS = 0V DI = V _{SS} or V _{CC} (Note 2) |
| D11 | V _{POR} | V _{CC} Voltage Detect | — | 1.5 | — | V | Note 1 |

Note 1: This parameter is periodically sampled and not 100% tested.

2: Ready/Busy status must be cleared from DO; see [Section 4.4 “Data Out \(DO\)”](#).

TABLE 1-2: AC CHARACTERISTICS

| AC CHARACTERISTICS | | | Electrical Characteristics: Industrial (I): $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ | | | |
|--------------------|--------|--------------------------|---|------|-------|---|
| Param. No. | Symbol | Characteristic | Min. | Max. | Units | Conditions |
| A1 | FCLK | Clock Frequency | — | 2 | MHz | $2.5\text{V} \leq V_{CC} < 5.5\text{V}$ |
| | | | — | 1 | MHz | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ |
| A2 | TCKH | Clock High Time | 250 | — | ns | $2.5\text{V} \leq V_{CC} < 5.5\text{V}$ |
| | | | 450 | — | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ |
| A3 | TCKL | Clock Low Time | 200 | — | ns | $2.5\text{V} \leq V_{CC} < 5.5\text{V}$ |
| | | | 450 | — | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ |
| A4 | TCSS | Chip Select Setup Time | 50 | — | ns | $4.5\text{V} \leq V_{CC} < 5.5\text{V}$ |
| | | | 100 | — | ns | $2.5\text{V} \leq V_{CC} < 4.5\text{V}$ |
| | | | 250 | — | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ |
| A5 | TCSH | Chip Select Hold Time | 0 | — | ns | $1.8\text{V} \leq V_{CC} < 5.5\text{V}$ |
| A6 | TCSL | Chip Select Low Time | 250 | — | ns | $1.8\text{V} \leq V_{CC} < 5.5\text{V}$ |
| A7 | TDIS | Data Input Setup Time | 100 | — | ns | $2.5\text{V} \leq V_{CC} < 5.5\text{V}$ |
| | | | 250 | — | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ |
| A8 | TDIH | Data Input Hold Time | 100 | — | ns | $2.5\text{V} \leq V_{CC} < 5.5\text{V}$ |
| | | | 250 | — | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$ |
| A9 | TPD | Data Output Delay Time | — | 200 | ns | $4.5\text{V} \leq V_{CC} < 5.5\text{V}$, $C_L = 100\text{ pF}$ |
| | | | — | 250 | ns | $2.5\text{V} \leq V_{CC} < 4.5\text{V}$, $C_L = 100\text{ pF}$ |
| | | | — | 400 | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$, $C_L = 100\text{ pF}$ |
| A10 | Tcz | Data Output Disable Time | — | 100 | ns | $4.5\text{V} \leq V_{CC} < 5.5\text{V}$ (Note 1) |
| | | | — | 200 | ns | $1.8\text{V} \leq V_{CC} < 4.5\text{V}$ (Note 1) |
| A11 | Tsv | Status Valid Time | — | 200 | ns | $4.5\text{V} \leq V_{CC} < 5.5\text{V}$, $C_L = 100\text{ pF}$ |
| | | | — | 300 | ns | $2.5\text{V} \leq V_{CC} < 4.5\text{V}$, $C_L = 100\text{ pF}$ |
| | | | — | 500 | ns | $1.8\text{V} \leq V_{CC} < 2.5\text{V}$, $C_L = 100\text{ pF}$ |
| A12 | TWC | Program Cycle Time | — | 6 | ms | Erase/Write mode |
| A13 | TEC | | — | 6 | ms | ERAL mode, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ |
| A14 | TWL | | — | 15 | ms | WRAL mode, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ |
| A15 | | | Endurance | 1M | — | cycles |

Note 1: This parameter is periodically sampled and not 100% tested.

2: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which may be obtained from Microchip's website at www.microchip.com.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

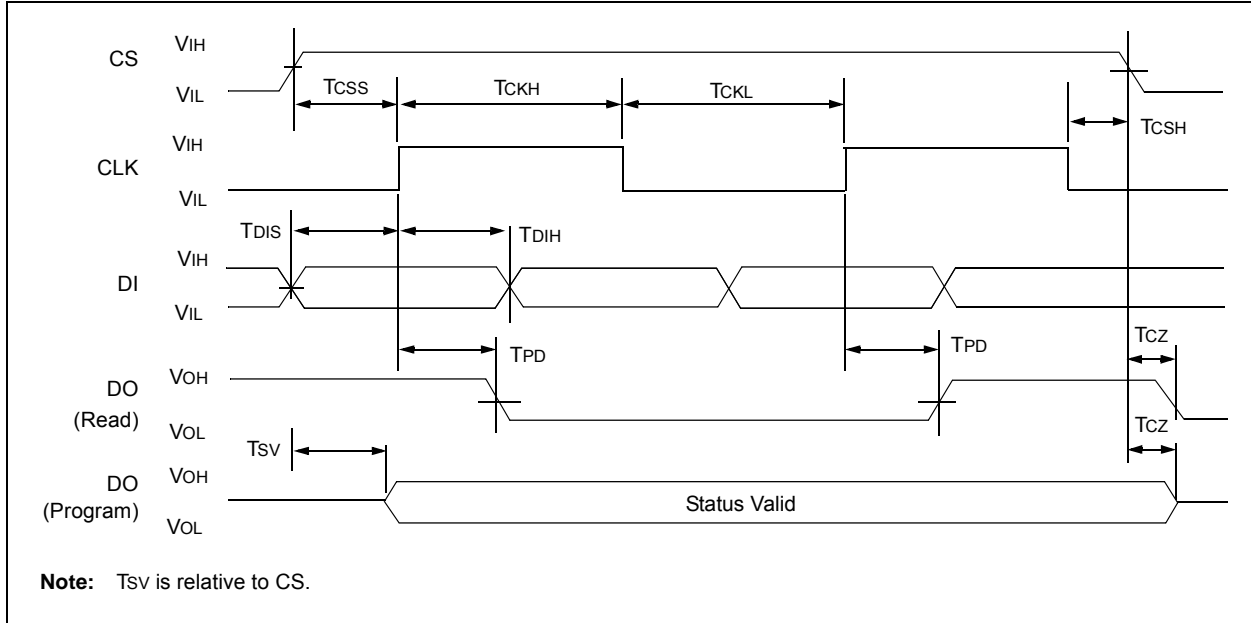


TABLE 1-3: INSTRUCTION SET

| Instruction | SB | Opcode | Address | Data In | Data Out | Req. CLK Cycles |
|-------------|----|--------|----------------------|---------|---------------------------------|-----------------|
| ERASE | 1 | 11 | A6 A5 A4 A3 A2 A1 A0 | — | (RDY/ $\overline{\text{BSY}}$) | 10 |
| ERAL | 1 | 00 | 1 0 X X X X X X | — | (RDY/ $\overline{\text{BSY}}$) | 10 |
| EWDS | 1 | 00 | 0 0 X X X X X X | — | High Z | 10 |
| EWEN | 1 | 00 | 1 1 X X X X X X | — | High Z | 10 |
| READ | 1 | 10 | A6 A5 A4 A3 A2 A1 A0 | — | D7-D0 | 18 |
| WRITE | 1 | 01 | A6 A5 A4 A3 A2 A1 A0 | D7-D0 | (RDY/ $\overline{\text{BSY}}$) | 18 |
| WRAL | 1 | 00 | 0 1 X X X X X X | D7-D0 | (RDY/ $\overline{\text{BSY}}$) | 18 |

2.0 FUNCTIONAL DESCRIPTION

Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a High Z state except when reading data from the device, or when checking the Ready/Busy status during a programming operation. The Ready/Busy status can be verified during an erase/write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the High Z state on the falling edge of CS.

2.1 Start Condition

The Start bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a Start condition is detected, CS, CLK and DI may change in any combination (except to that of a Start condition), without resulting in any device operation (Read, Write, Erase, EWEN, EWDS, ERAL or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a Start condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

Note: When preparing to transmit an instruction, either the CLK or DI signal levels must be at a logic low as CS is toggled active-high.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration, it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation if A0 is a logic high level. Under such a condition, the voltage level seen at Data Out is undefined and depends upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

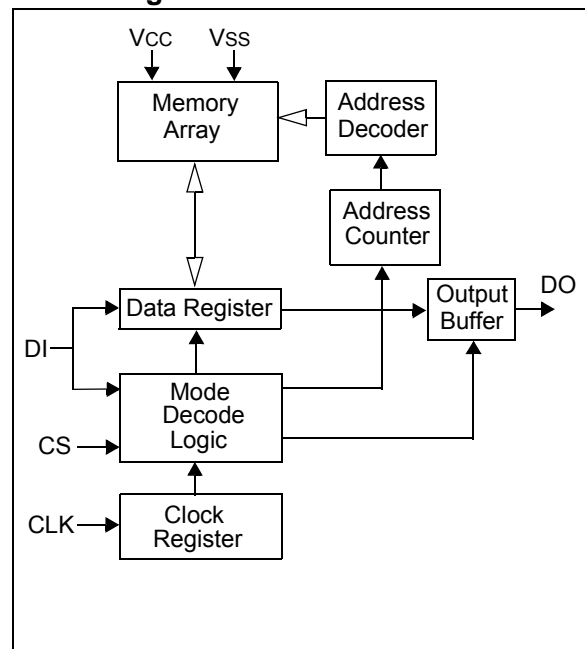
All modes of operation are inhibited when VCC is below a typical voltage of 1.5V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation and an external 10 kΩ pull-down protection resistor should be added to the CS pin.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Block Diagram



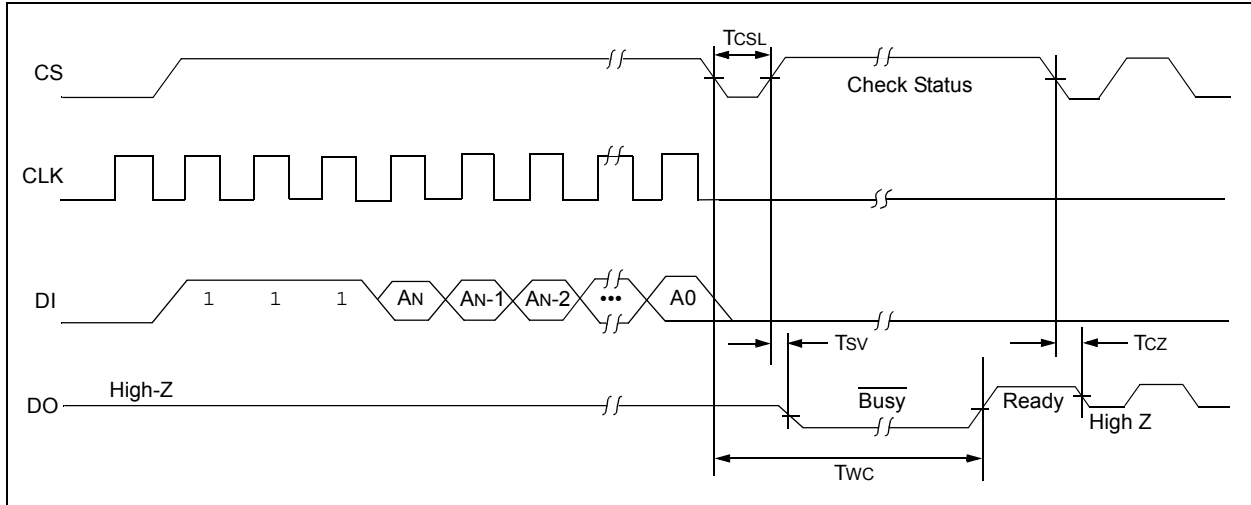
2.4 Erase

The `ERASE` instruction forces all data bits of the specified address to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: After the Erase cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-1: ERASE TIMING



2.5 Erase All (ERAL)

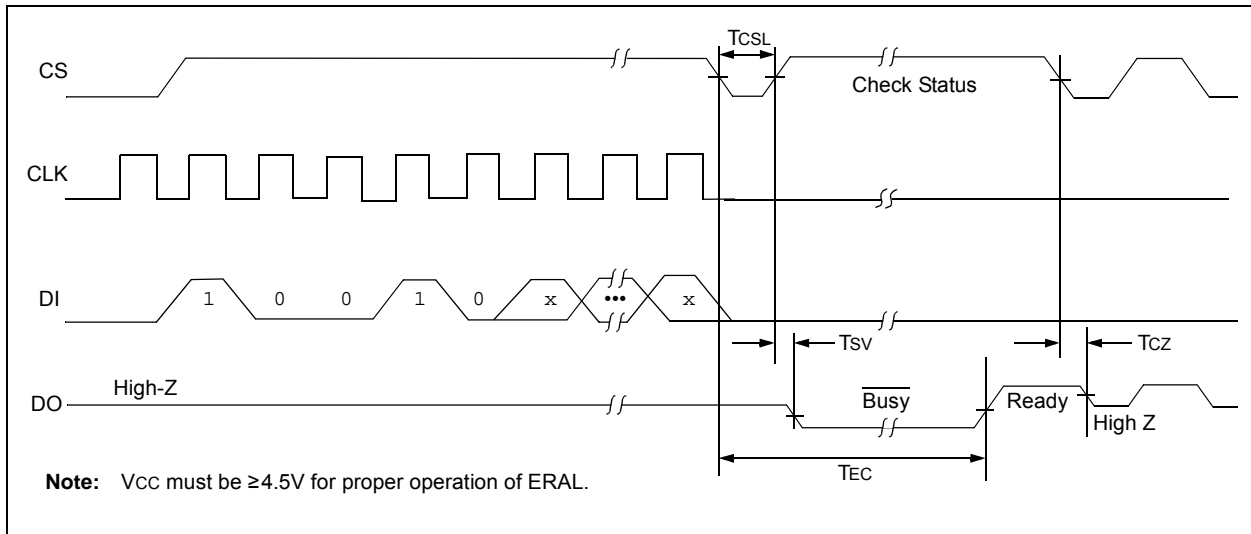
The Erase All (ERAL) instruction will erase the entire memory array to the logical '1' state. The ERAL cycle is identical to the erase cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

VCC must be $\geq 4.5V$ for proper operation of ERAL.

Note: After the ERAL command is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-2: ERAL TIMING



2.6 Erase/Write Disable and Enable (EWDS/EWEN)

The 93AA46AE48 powers up in the Erase/Write Disable (EWDS) state. All programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or Vcc is removed from the device.

To protect against accidental data disturbance, the EWDS instruction can be used to disable all erase/write functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-3: EWDS TIMING

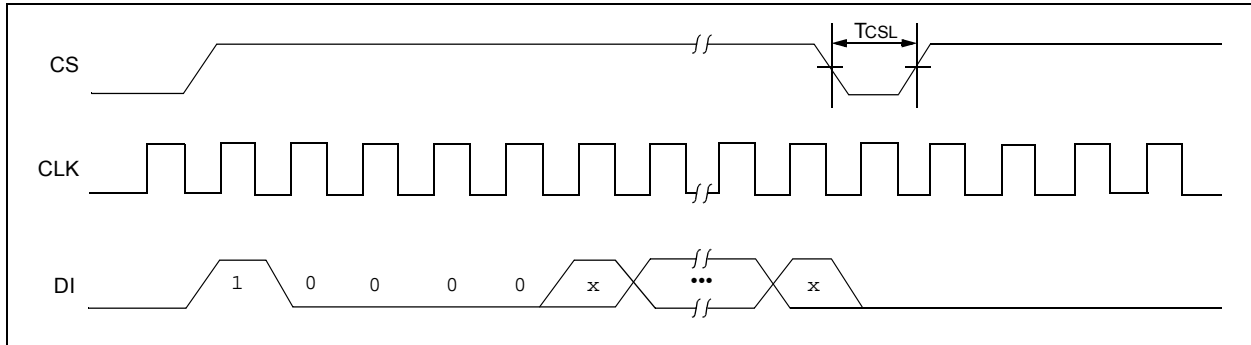
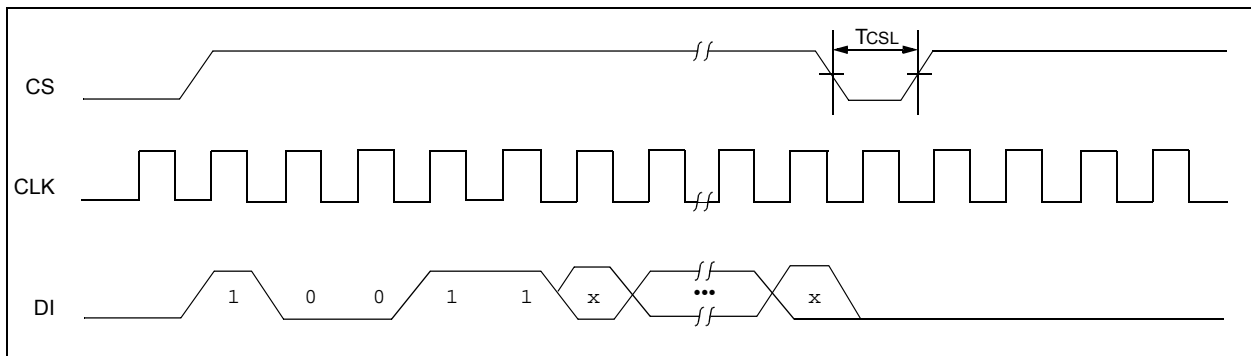


FIGURE 2-4: EWEN TIMING

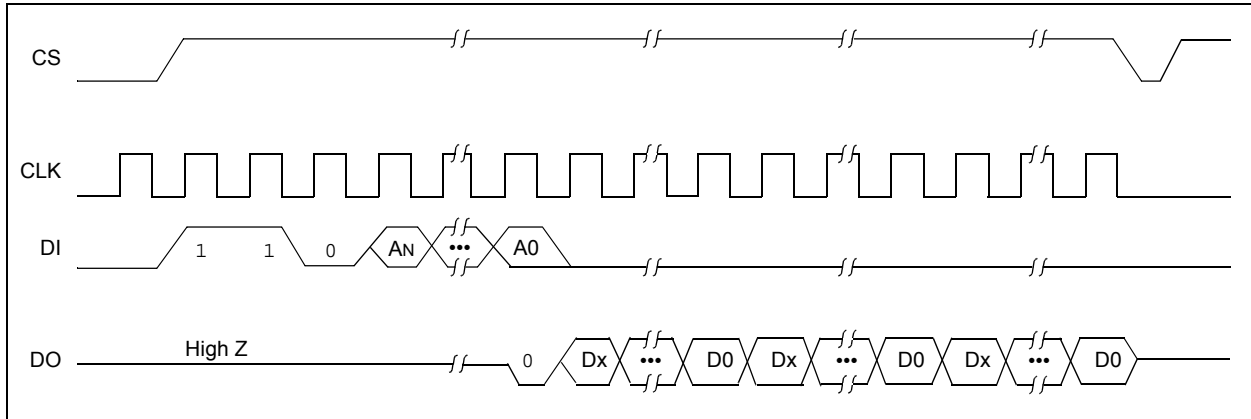


2.7 Read

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit output string.

The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-5: READ TIMING



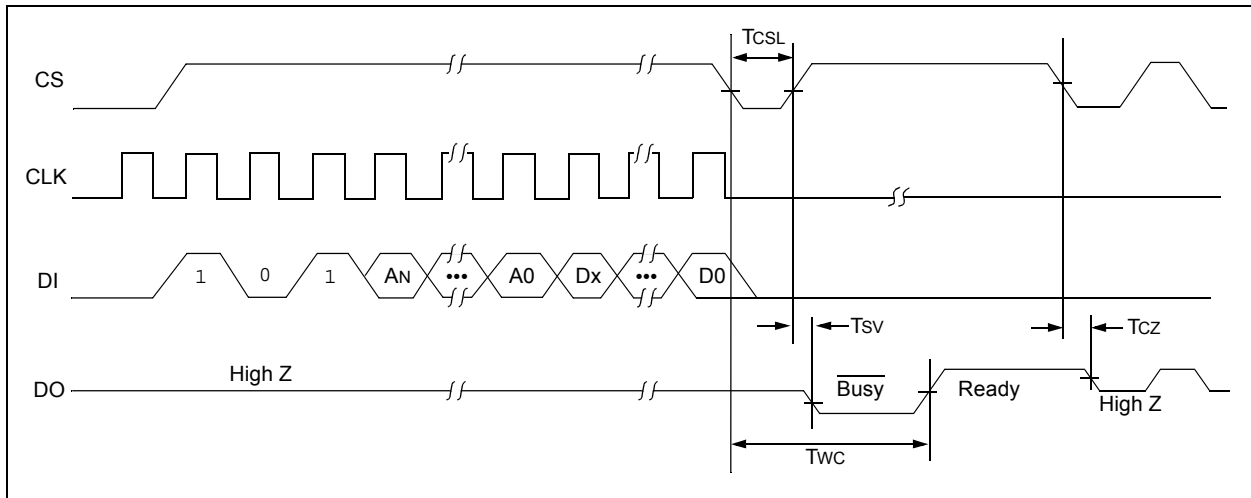
2.8 Write

The `WRITE` instruction is followed by eight bits of data, which are written into the specified address. For 93AA46AE48, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical '0' indicates that programming is still in progress. DO at logical '1' indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: After the Write cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-6: WRITE TIMING



2.9 Write All (WRAL)

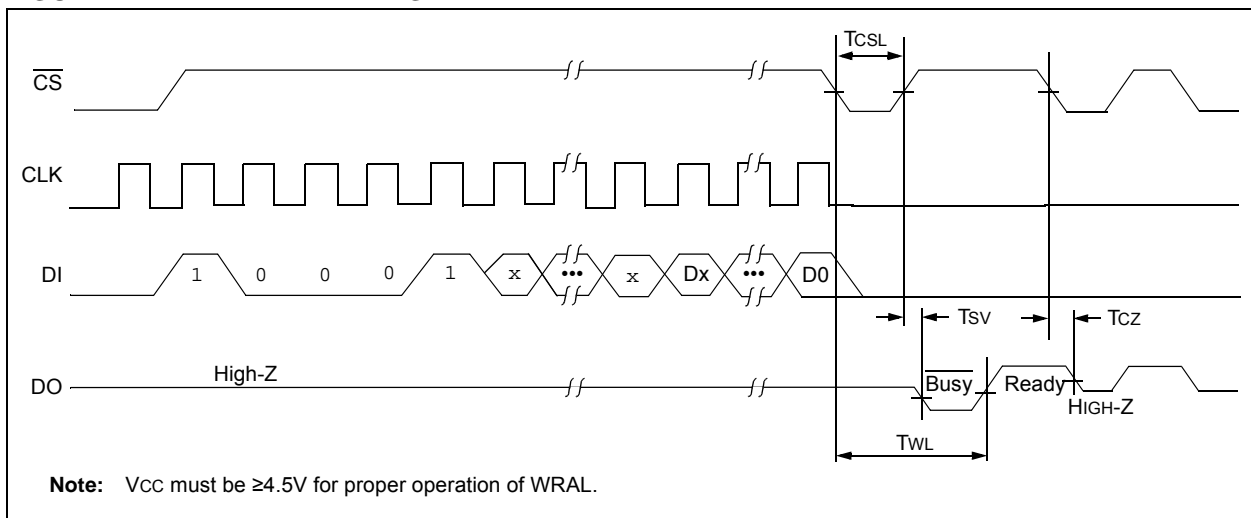
The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AA46AE48, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction, but the chip must be in the EWEN status.

The DO pin indicates the Ready/Busy status of the device if CS is brought high after a minimum of 250 ns low (TCSL).

VCC must be $\geq 4.5V$ for proper operation of WRAL.

Note: After the Write All cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

FIGURE 2-7: WRAL TIMING



3.0 PREPROGRAMMED EUI-48 NODE ADDRESS

The 93AA46AE48 is programmed at the factory with a globally unique node address stored at the beginning of the array. It is preceded by the EEPROM Programmed Indicator (EPI), which indicates valid programming.

The 93AA46AE48 is designed to be compatible with the following SMSC Ethernet controllers: LAN9210, LAN9211, LAN9215, LAN9217, LAN9218, LAN9220, and LAN9221. These controllers will automatically detect and load the EUI-48 node address from the 93AA46AE48 at start-up.

3.1 EUI-48 Node Address

The 6-byte EUI-48 node address value of the 93AA46AE48 is stored in array locations 0x01 through 0x06, as shown in [Figure 3-1](#). The first three bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. The remaining three bytes are the Extension Identifier, and are generated by Microchip to ensure a globally unique, 48-bit value.

3.1.0.1 Organizationally Unique Identifiers (OUIs)

Each OUI provides roughly 16M (2^{24}) addresses. Once the address pool for an OUI is exhausted, Microchip will acquire a new OUI from IEEE to use for programming this model. For more information on past and current OUIs see “*Organizationally Unique Identifiers For Preprogrammed EUI-48 and EUI-64 Address Devices*” Technical Brief (DS90003187).

Note: The OUI will change as addresses are exhausted. Customers are not guaranteed to receive a specific OUI and should design their application to accept new OUIs as they are introduced.

3.1.1 EUI-64 SUPPORT USING THE 93AA46AE48

The preprogrammed EUI-48 node address of the 93AA46AE48 can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFE between the OUI and the Extension Identifier as shown below.

3.2 EEPROM Programmed Indicator (EPI)

In addition to the node address, a programmed indicator code is stored at the location 0x00. The code is fixed as 0xA5. Its purpose is to let the master device know that the EEPROM has been programmed with a valid MAC address.

Note: The preprogrammed values are not write-protected and can be overwritten by the user. Care must be taken not to overwrite the values unintentionally.

FIGURE 3-1: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE

| Description | 24-bit Organizationally Unique Identifier | | | | 24-bit Extension Identifier | | |
|---------------|---|-----|-----|-----|-----------------------------|-----|-----|
| | EPI | | | | | | |
| Data | A5h | 00h | 04h | A3h | 12h | 34h | 56h |
| Array Address | 00h | 01h | 02h | 03h | 04h | 05h | 06h |

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56
Corresponding EUI-64™ Node Address After Encapsulation: 00-04-A3-FF-FE-12-34-56

4.0 PIN DESCRIPTIONS

The description of the pins are listed in [Table 4-1](#).

TABLE 4-1: PIN FUNCTION TABLE

| Name | SOIC | SOT-23 | Function |
|------|------|--------|------------------------|
| CS | 1 | 5 | Chip Select |
| CLK | 2 | 4 | Serial Clock |
| DI | 3 | 3 | Data In |
| DO | 4 | 1 | Data Out |
| Vss | 5 | 2 | Ground |
| NC | 6 | — | No Internal Connection |
| NC | 7 | — | No Internal Connection |
| Vcc | 8 | 6 | Power Supply |

4.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle that is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (T_{CSL}) between consecutive instructions. If CS is low, the internal control logic is held in a Reset status.

4.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93AA46AE48 series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T_{CKH}) and clock low time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “don't care” if CS is low (device deselected). If CS is high, but the Start condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a Start condition).

CLK cycles are not required during the self-timed write (i.e., auto erase/write) cycle.

After detection of a Start condition, the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become “don't care” inputs waiting for a new Start condition to be detected.

4.3 Data In (DI)

Data In (DI) is used to clock in a Start bit, opcode, address and data synchronously with the CLK input.

4.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK).

This pin also provides Ready/Busy status information during erase and write cycles. Ready/Busy status information is available on the DO pin if CS is brought high after being low for minimum Chip Select low time (T_{CSL}) and an erase or write operation has been initiated.

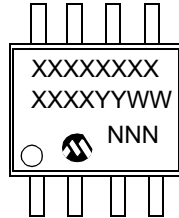
The Status signal is not available on DO if CS is held low during the entire erase or write cycle. In this case, DO is in the High Z mode. If status is checked after the erase/write cycle, the data line will be high to indicate the device is ready.

Note: After a programming cycle is complete, issuing a Start bit and then taking CS low will clear the Ready/Busy status from DO.

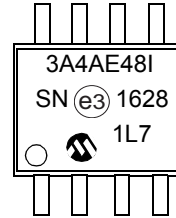
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

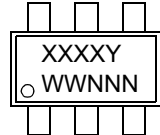
8-Lead SOIC



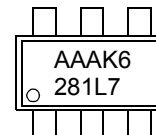
Example



6-Lead SOT-23



Example



| Part Number | 1st Line Marking Codes | |
|-------------|------------------------|--------|
| | SOIC | SOT-23 |
| 93AA46AE48 | 3A4AE48T | AAAKY |

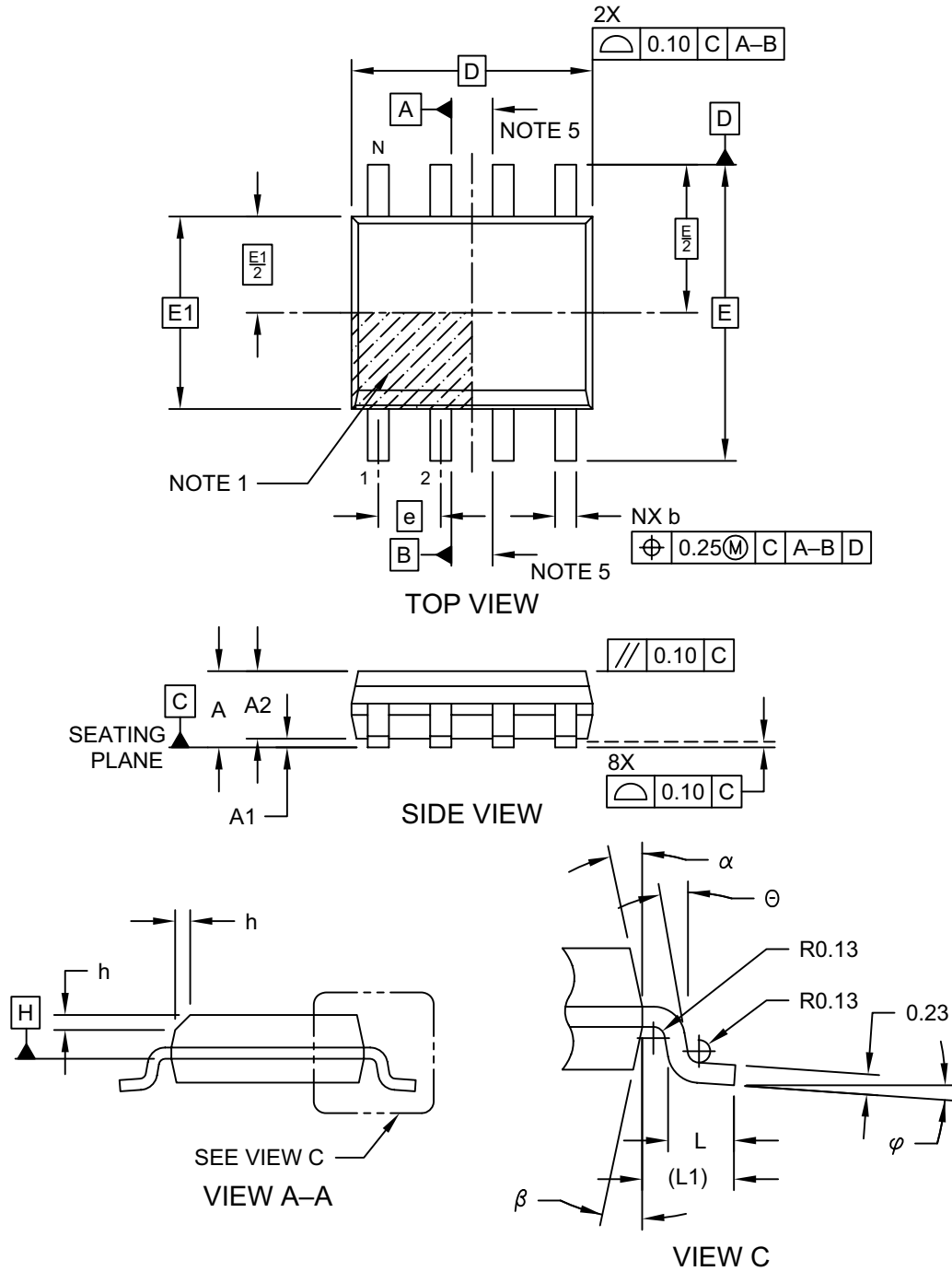
| | | |
|----------------|--------|--|
| Legend: | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | e3 | Pb-free JEDEC® designator for Matte Tin (Sn) |

Note: For very small packages with no room for the Pb-free JEDEC® designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

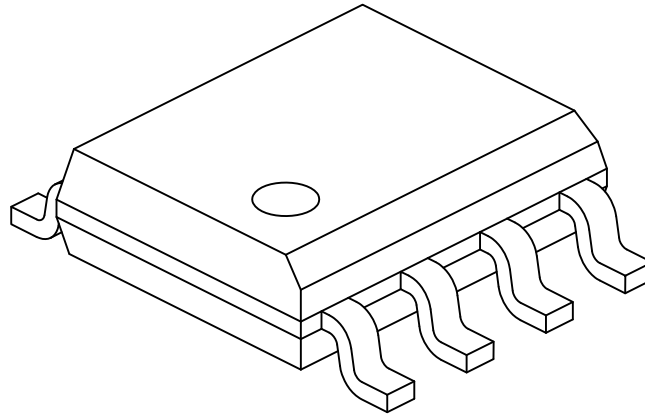
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|-----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

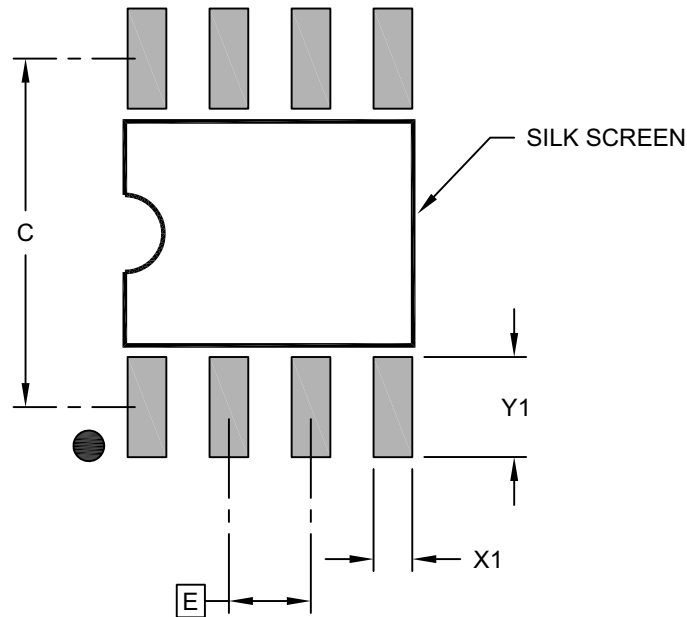
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|----------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

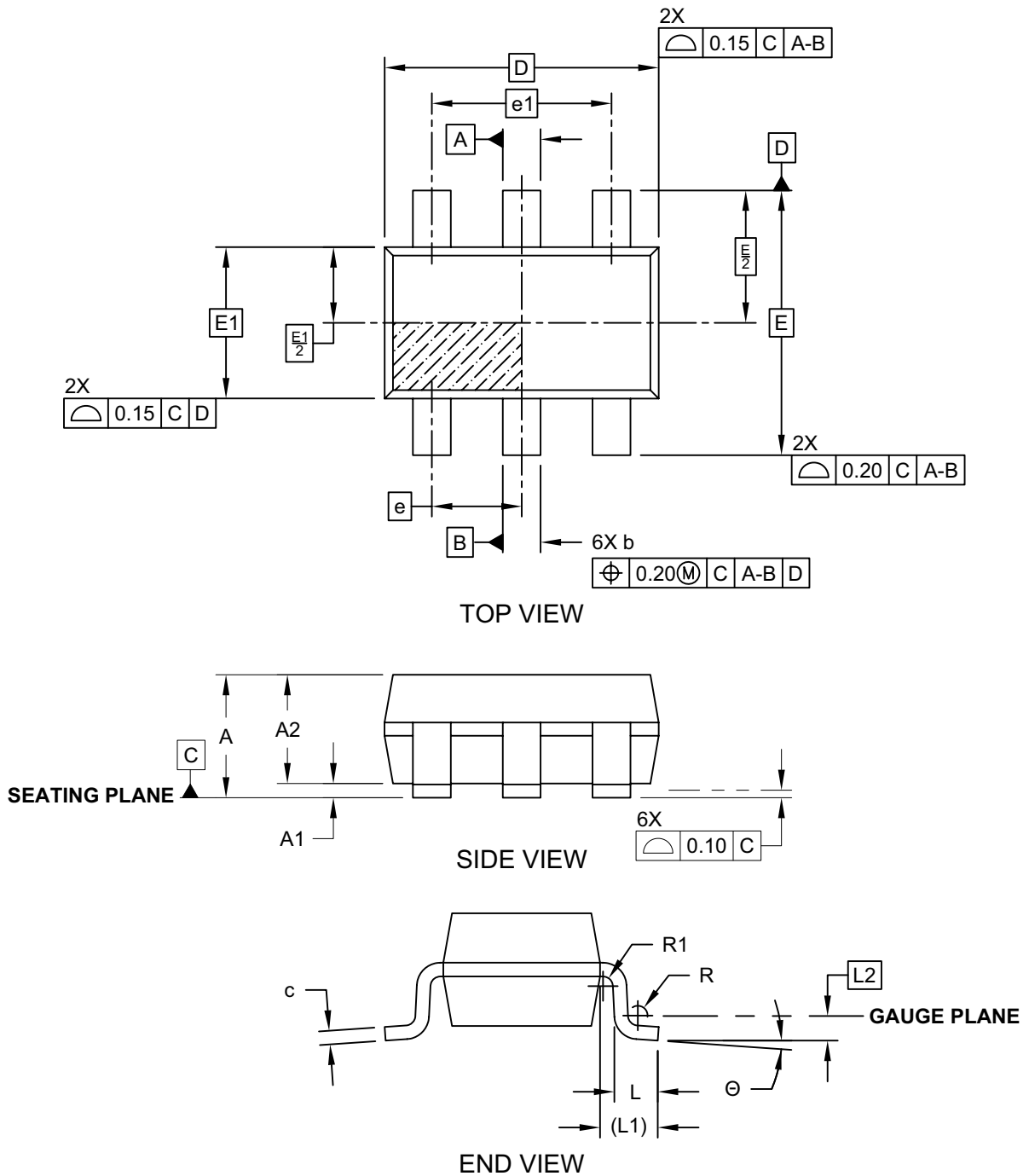
Notes:

- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

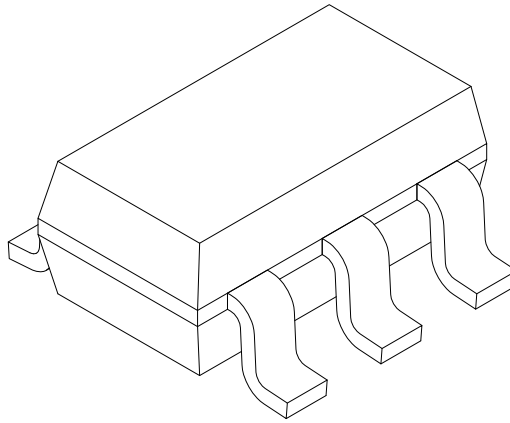
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-028C (OT) Sheet 1 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Leads | N | 6 | | |
| Pitch | e | 0.95 BSC | | |
| Outside lead pitch | e1 | 1.90 BSC | | |
| Overall Height | A | 0.90 | - | 1.45 |
| Molded Package Thickness | A2 | 0.89 | 1.15 | 1.30 |
| Standoff | A1 | 0.00 | - | 0.15 |
| Overall Width | E | 2.80 BSC | | |
| Molded Package Width | E1 | 1.60 BSC | | |
| Overall Length | D | 2.90 BSC | | |
| Foot Length | L | 0.30 | 0.45 | 0.60 |
| Footprint | L1 | 0.60 REF | | |
| Seating Plane to Gauge Plane | L1 | 0.25 BSC | | |
| Foot Angle | ϕ | 0° | - | 10° |
| Lead Thickness | c | 0.08 | - | 0.26 |
| Lead Width | b | 0.20 | - | 0.51 |

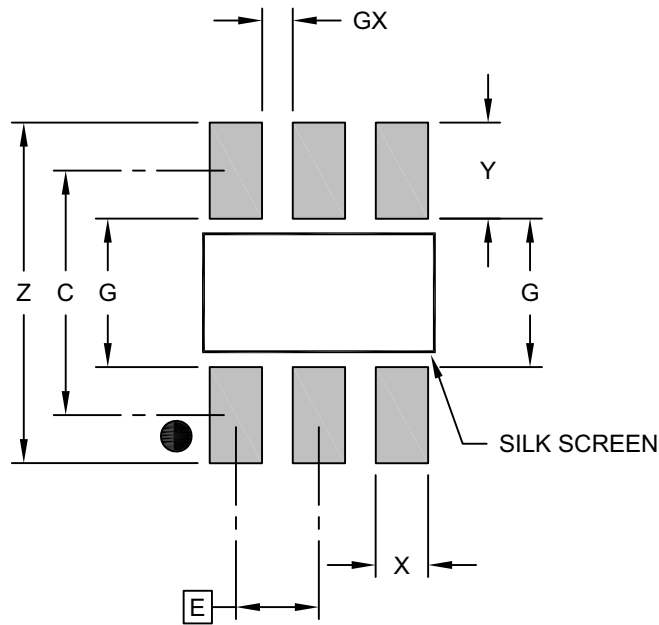
Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-028C (OT) Sheet 2 of 2

6-Lead Plastic Small Outline Transistor (OT, OTY) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

| Dimension Limits | Units | MILLIMETERS | | |
|-------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Contact Pitch | E | 0.95 BSC | | |
| Contact Pad Spacing | C | | 2.80 | |
| Contact Pad Width (X3) | X | | | 0.60 |
| Contact Pad Length (X3) | Y | | | 1.10 |
| Distance Between Pads | G | 1.70 | | |
| Distance Between Pads | GX | 0.35 | | |
| Overall Width | Z | | | 3.90 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028B (OT)

APPENDIX A: REVISION HISTORY

Revision A (October 2013)

Initial release of this document.

Revision B (December 2014)

Updated Section 3.0 “Preprogrammed EUI-48 Node Address”; Updated “[Product Identification System](#)” section; Minor typographical corrections.

Revision C (August 2016)

Added new OUI (54-10-EC) to list.

Revision D (02/2018)

Added detailed description of OUIs.

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PRODUCT IDENTIFICATION SYSTEM

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| <u>PART NO.</u> | | <u>X</u> ⁽¹⁾ | <u>X</u> | <u>/XX</u> |
|------------------------------|----------------|---|--|------------|
| Device | | Tape & Reel | Temperature Range | Package |
| Device: | 93AA46AE48: | | 1K 1.8V Microwire Serial EEPROM with EUI-48™ Node Identity | |
| Tape and Reel Option: | Blank = T = | Standard packaging (tube or tray) Tape and Reel ⁽¹⁾ | | |
| Temperature Range: | I = | -40°C to +85°C | | |
| Package: | OT = SN = | Plastic SOT-23, 6-lead (Tape & Reel only) Plastic SOIC (3.9 mm body), 8-lead | | |

Examples:

a) 93AA46AE48-I/SN: 1K, 128x8 Serial EEPROM, with EUI-48 Node Identity, 1.8V, Industrial Temperature, SOIC package.

b) 93AA46AE48T-I/SN: 1K, 128x8 Serial EEPROM with EUI-48 Node Identity, 1.8V, Tape & Reel, Industrial Temperature SOIC package.

c) 93AA46AE48T-I/OT: 1K, 128x8 Serial EEPROM with EUI-48 Node Identity, 1.8V, Tape & Reel, Industrial Temperature, SOT-23 package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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