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This document, MC74HC4316/D has been canceled and replaced by MC74HC4316A/D LAN was sent 9/28/01

Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

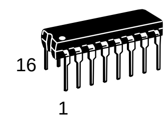
High–Performance Silicon–Gate CMOS

The MC74HC4316 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power–supply range (from V_{CC} to V_{EE}).

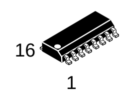
The HC4316 is similar in function to the metal–gate CMOS MC14016 and MC14066, and to the High–Speed CMOS HC4016 and HC4066. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances (R_{ON}) are much more linear over input voltage than R_{ON} of metal–gate CMOS analog switches. Logic–level translators are provided so that the On/Off Control and Enable logic–level voltages need only be V_{CC} and GND, while the switch is passing signals ranging between V_{CC} and V_{EE}. When the Enable pin (active–low) is high, all four analog switches are turned off.

- Logic–Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power–Supply Voltage Range (V_{CC} – V_{EE}) = 2.0 to 12.0 Volts
- Digital (Control) Power–Supply Voltage Range (V_{CC} – GND) = 2.0 to 6.0 Volts, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates

MC74HC4316



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

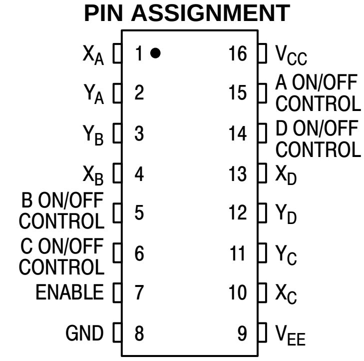


D SUFFIX
SOIC PACKAGE
CASE 751B–05

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC74HCXXXXD	SOIC

PIN ASSIGNMENT

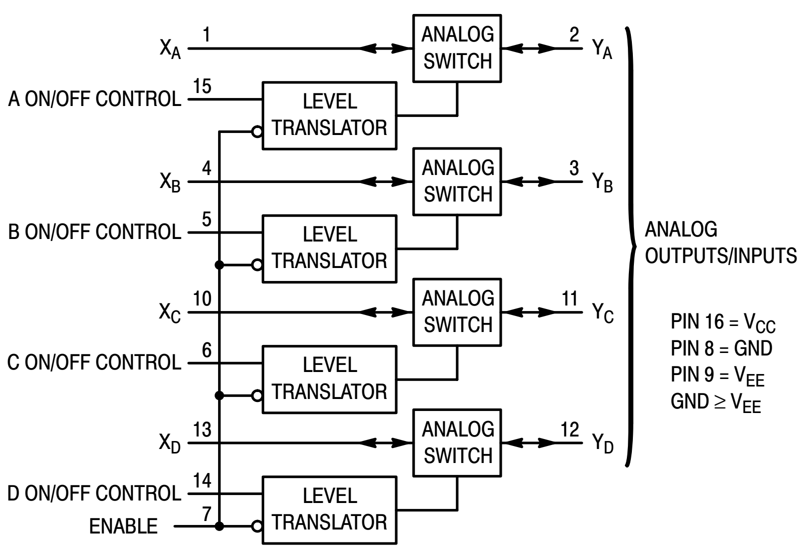


FUNCTION TABLE

Inputs		State of Analog Switch
Enable	On/Off Control	
L	H	On
L	L	Off
H	X	Off

X = don't care

LOGIC DIAGRAM



ANALOG INPUTS/OUTPUTS = X_A, X_B, X_C, X_D

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND) (Ref. to V_{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 7.0 to + 0.5	V
V_{IS}	Analog Input Voltage	V_{EE} – 0.5 to V_{CC} + 0.5	V
V_{in}	DC Input Voltage (Ref. to GND)	– 1.5 to V_{CC} + 1.5	V
I	DC Current Into or Out of Any Pin	± 25	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage (Ref. to GND)	2.0	6.0	V
V_{EE}	Negative DC Supply Voltage (Ref. to GND)	– 6.0	GND	V
V_{IS}	Analog Input Voltage	V_{EE}	V_{CC}	V
V_{in}	Digital Input Voltage (Ref. to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch	—	1.2	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Control or Enable Inputs) (Figure 10) V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit – 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V_{IH}	Minimum High–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low–Level Voltage, Control or Enable Inputs	R_{on} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I_{in}	Maximum Input Leakage Current, Control or Enable Inputs	V_{in} = V_{CC} or GND V_{EE} = – 6.0 V	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND V_{IO} = 0 V V_{EE} = GND V_{EE} = – 6.0	 6.0 6.0	 2 8	 20 80	 40 160	µA

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ to V_{EE} $I_S \leq 2.0$ mA (Figures 1, 2)	2.0* 4 5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 210 95 75	— 230 105 85	— 250 110 90	Ω
		$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq 2.0$ mA (Figures 1, 2)	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 100 80 70	— 110 90 80	— 130 100 90	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IH}$ $V_{IS} = 1/2 (V_{CC} – V_{EE})$ $I_S \leq 2.0$ mA	2.0 4.5 4.5 6.0	0.0 0.0 – 4.5 – 6.0	— 20 15 10	— 30 25 20	— 40 30 25	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or V_{EE} Switch Off (Figure 3)	6.0	– 6.0	0.1	0.5	1.0	µA
I_{on}	Maximum On–Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Figure 4)	6.0	– 6.0	0.1	0.5	1.0	µA

* At supply voltage (V_{CC} – V_{EE}) approaching 2 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable $t_r = t_f$ = 6 ns, V_{EE} = GND)

Symbol	Parameter	V_{CC} V	Guaranteed Limit – 55 to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 4.5 6.0	50 10 10	75 15 13	90 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	250 50 43	312 63 54	375 75 64	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	185 53 45	220 66 56	265 75 68	ns
C	Maximum Capacitance — ON/OFF Control and Enable Inputs	—	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough	 — —	 35 1.0	 35 1.0	 35 1.0	

Symbol	Parameter	Typical @ 25°C, V_{CC} = 5.0 V	Unit
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in} = 1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequency Until dB Meter Reads – 3 dB R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	150 160 160	MHz
—	Off–Channel Feedthrough Isolation (Figure 6)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 50 – 50 – 50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 40 – 40 – 40	
—	Feedthrough Noise, Control to Switch (Figure 7)	$V_{in} \leq$ 1 MHz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	60 130 200	mV_{PP}
		R_L = 10 kΩ, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	30 65 100	
—	Crosstalk Between Any Two Switches (Figure 12)	$f_{in} \equiv$ Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 70 – 70 – 70	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	2.25 4.50 6.00	– 2.25 – 4.50 – 6.00	– 80 – 80 – 80	
THD	Total Harmonic Distortion (Figure 14)	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{Measured} - THD_{Source}$ V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 8.0 V_{PP} sine wave V_{IS} = 11.0 V_{PP} sine wave	 2.25 4.50 6.00	 – 2.25 – 4.50 – 6.00	 0.10 0.06 0.04	%

* Limits not tested. Determined by design and verified by qualification.

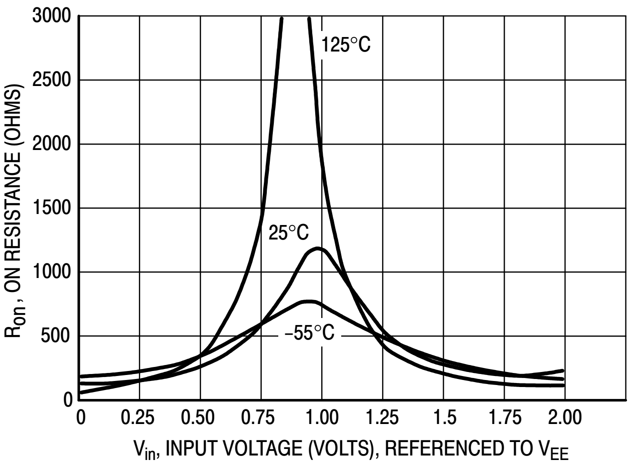


Figure 1a. Typical On Resistance, $V_{CC} - V_{EE} = 2.0$ V

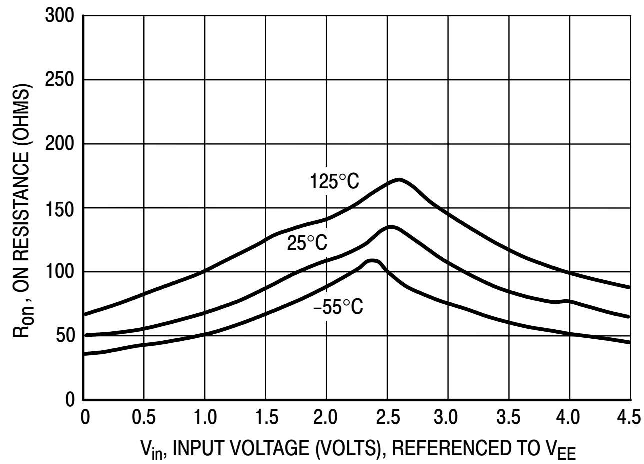


Figure 1b. Typical On Resistance, $V_{CC} - V_{EE} = 4.5$ V

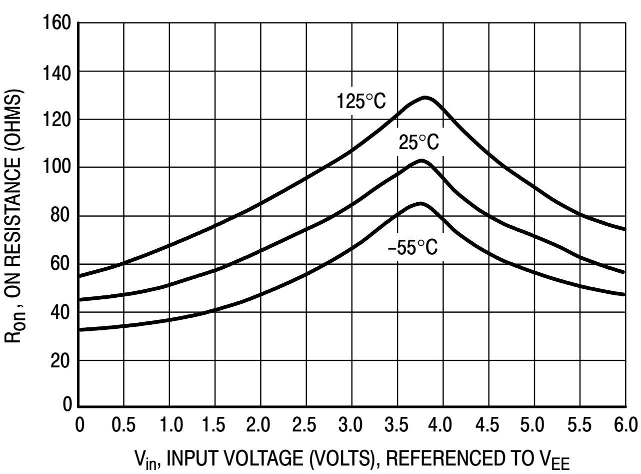


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 6.0$ V

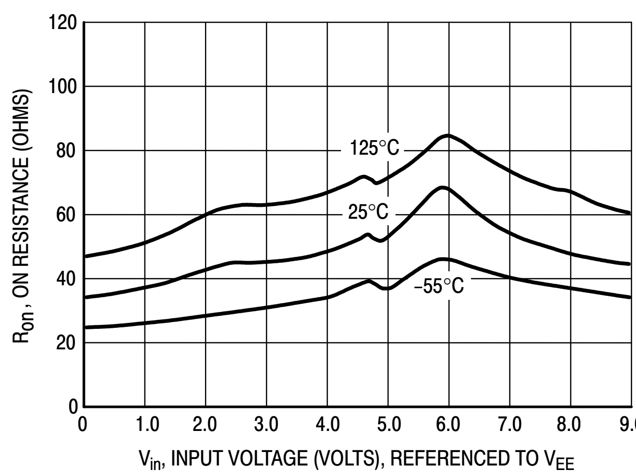


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 9.0$ V

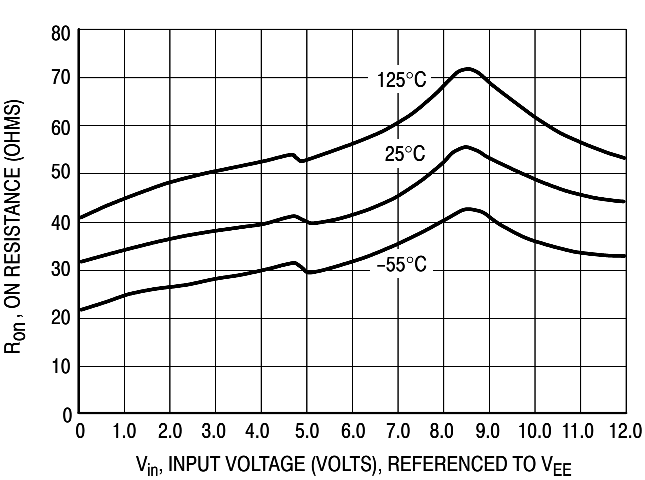


Figure 1e. Typical On Resistance,

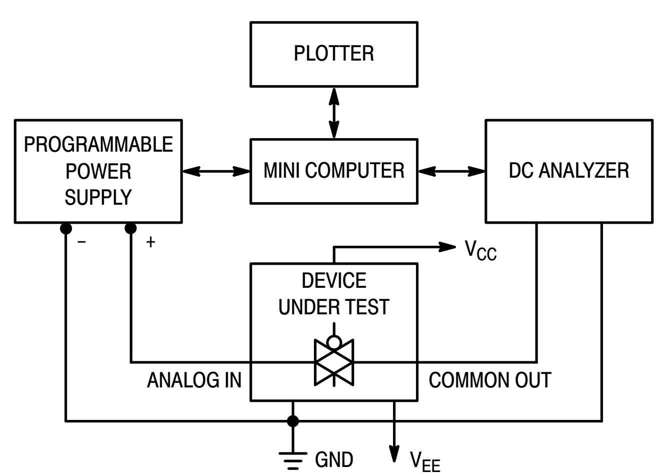


Figure 2. On Resistance Test Set–Up

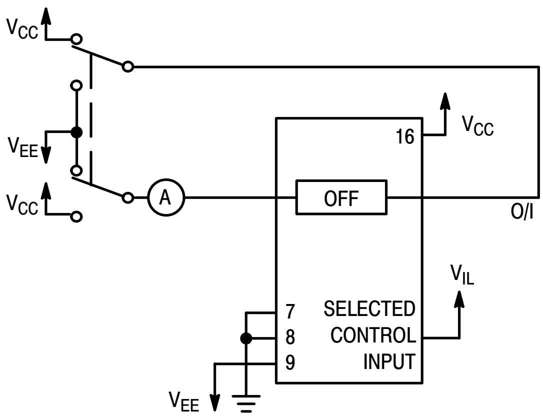


Figure 3. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

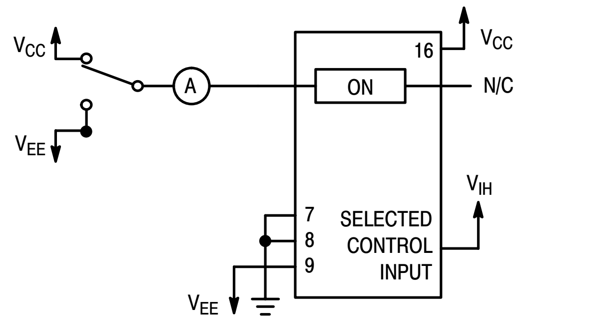
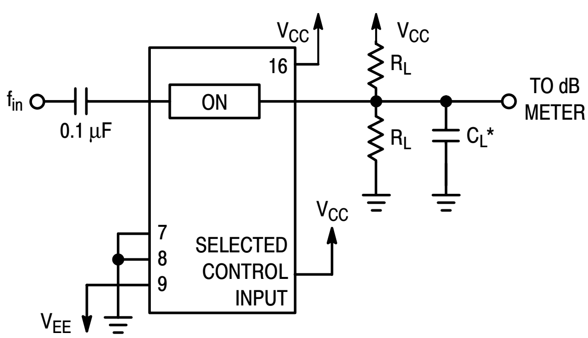
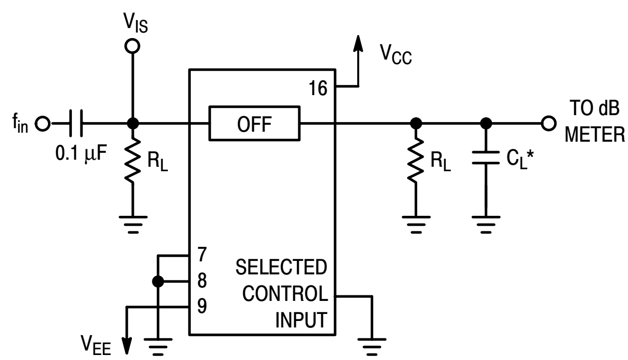


Figure 4. Maximum On Channel Leakage Current, Test Set–Up



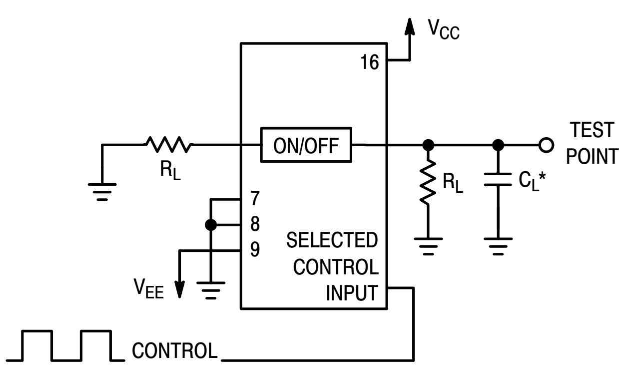
*Includes all probe and jig capacitance.

Figure 5. Maximum On–Channel Bandwidth Test Set–Up



*Includes all probe and jig capacitance.

Figure 6. Off–Channel Feedthrough Isolation, Test Set–Up



*Includes all probe and jig capacitance.

Figure 7. Feedthrough Noise, Control to Analog Out, Test Set–Up

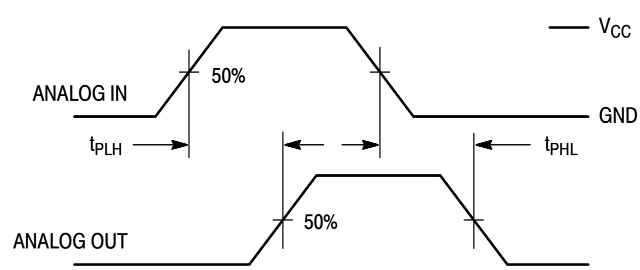
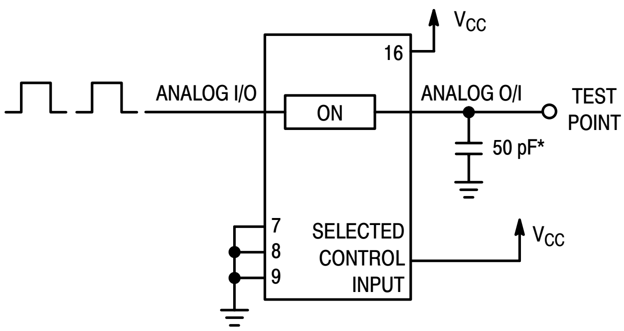


Figure 8. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance.

Figure 9. Propagation Delay Test Set–Up

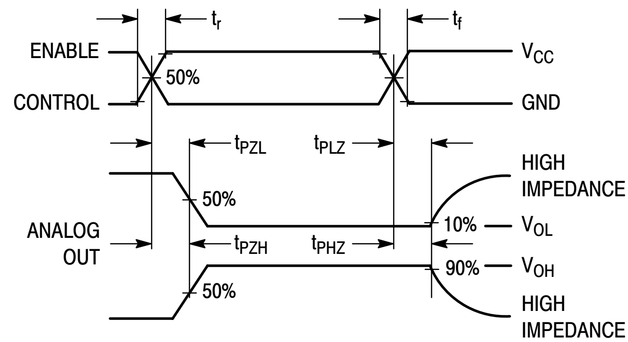
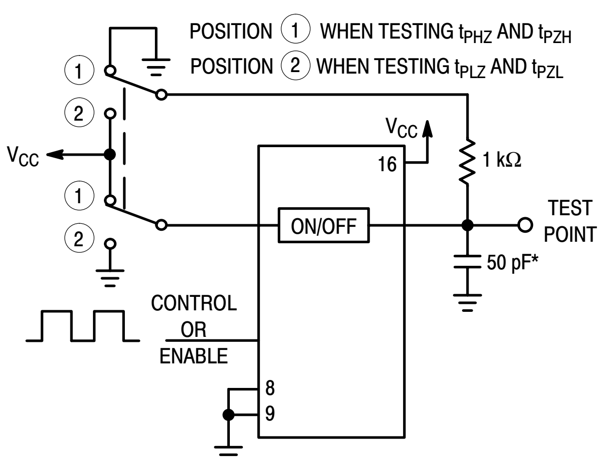
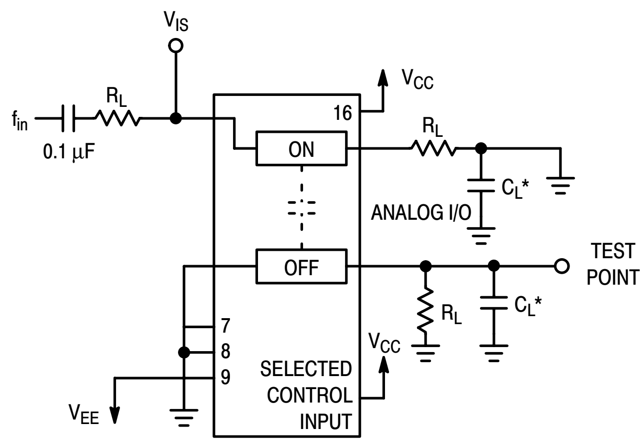


Figure 10. Propagation Delay, ON/OFF Control to Analog Out



*Includes all probe and jig capacitance.

Figure 11. Propagation Delay Test Set–Up



*Includes all probe and jig capacitance.

Figure 12. Crosstalk Between Any Two Switches, Test Set–Up (Adjacent Channels Used)

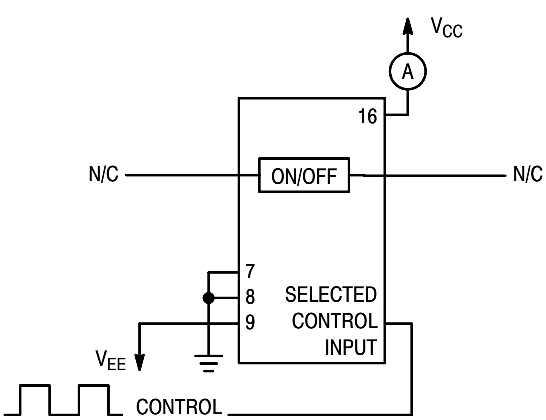
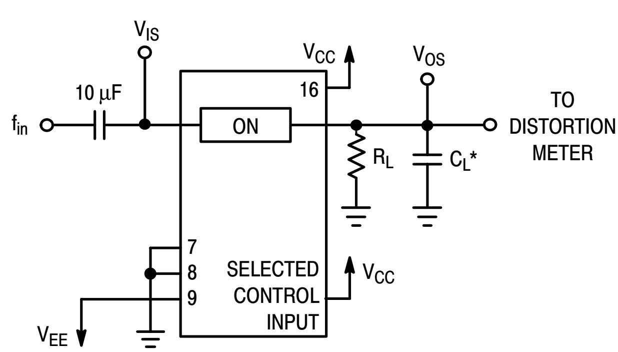


Figure 13. Power Dissipation Capacitance Test Set–Up



*Includes all probe and jig capacitance.

Figure 14. Total Harmonic Distortion, Test Set–Up

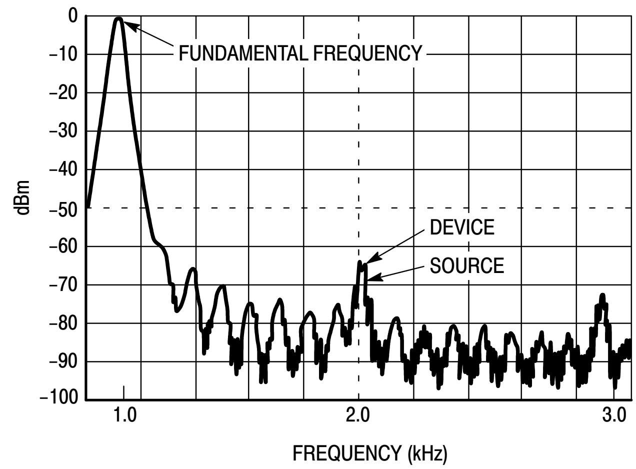


Figure 15. Plot, Harmonic Distortion

APPLICATION INFORMATION

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In the example below, the difference between V_{CC} and V_{EE} is twelve volts. Therefore, using the configuration in Figure 16, a maximum analog signal of twelve volts peak–to–peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 17. These diodes should be small signal, fast turn–on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MO•sorbs (high current surge protectors). MO•sorbs are fast turn–on devices ideally suited for precise dc protection with no inherent wear out mechanism.

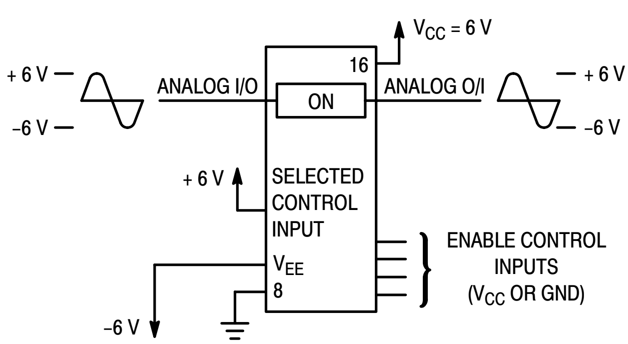


Figure 16.

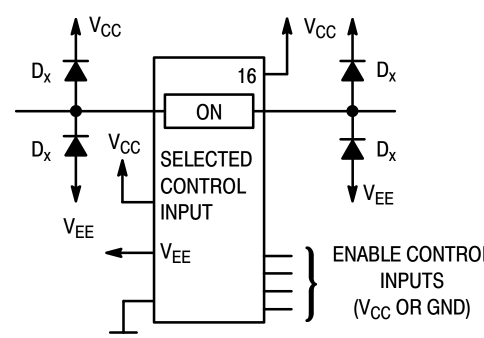
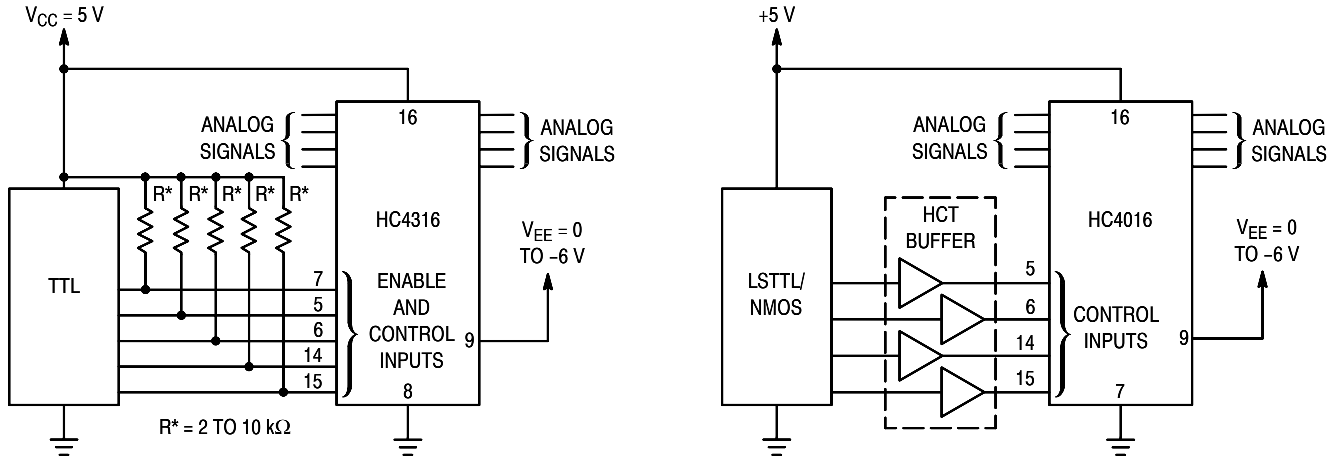


Figure 17. Transient Suppressor Application



a. Using Pull–Up Resistors

b. Using HCT Buffer

Figure 18. LSTTL/NMOS to HCMOS Interface

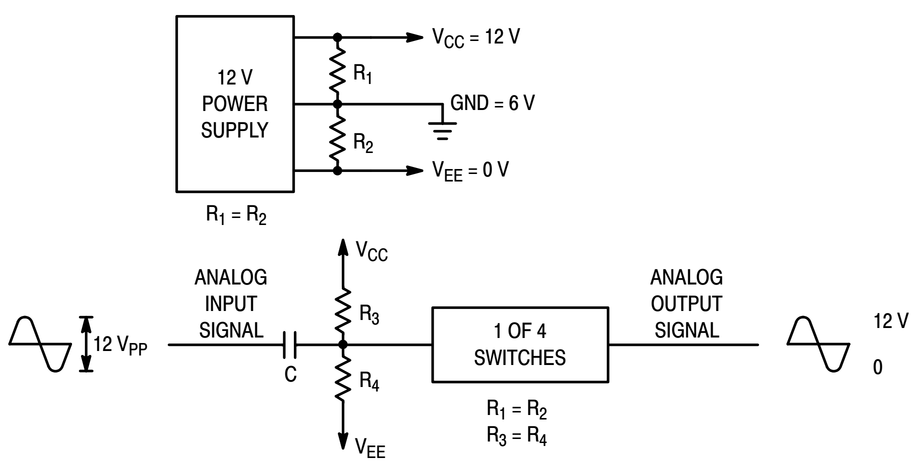


Figure 19. Switching a 0–to–12 V Signal Using a Single Power Supply (GND ≠ 0 V)

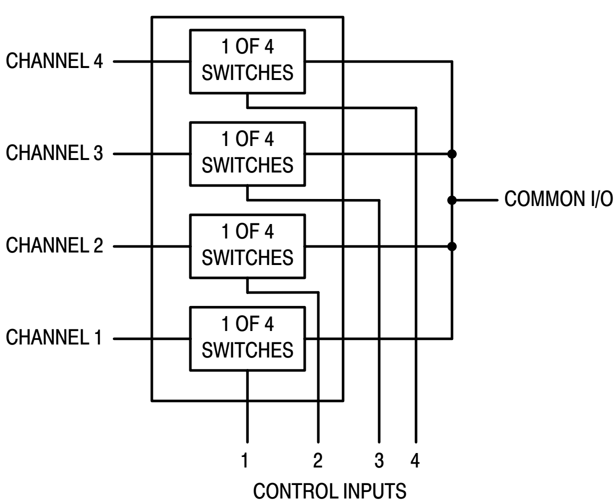


Figure 20. 4–Input Multiplexer

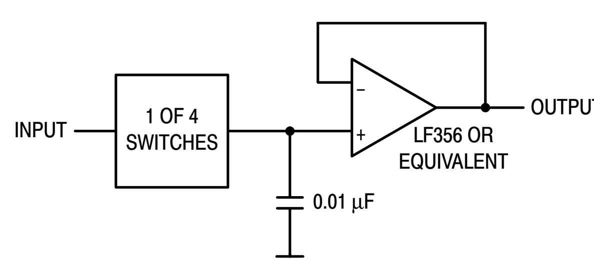
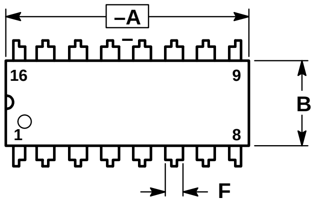
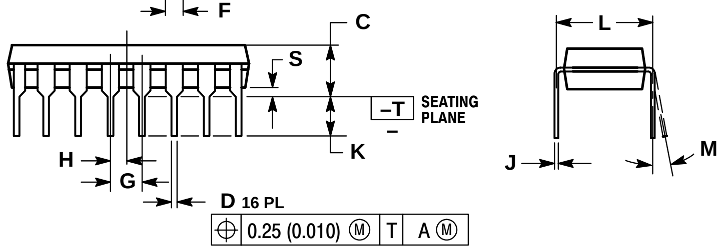


Figure 21. Sample/Hold Amplifier

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

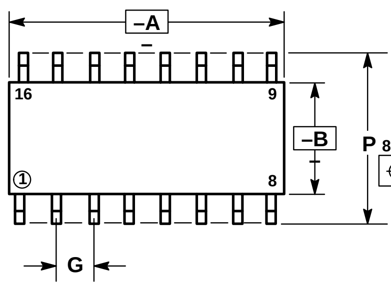


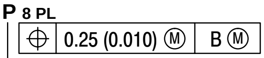


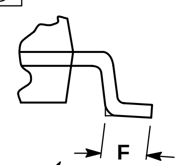
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

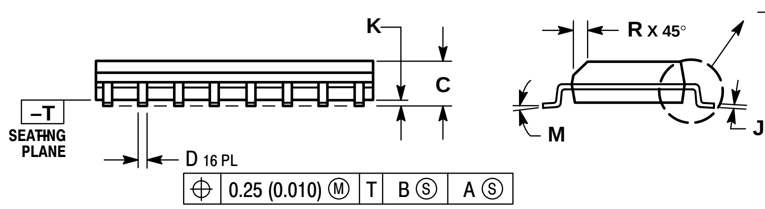
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J









NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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