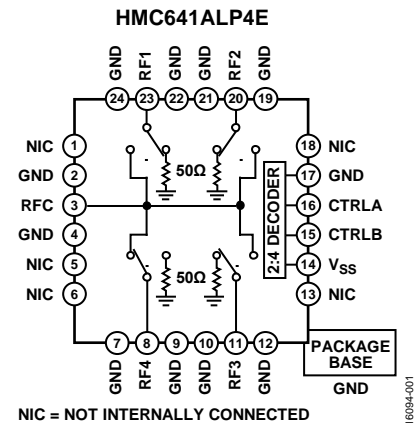


FEATURES
Broadband frequency range: 0.1 GHz to 20 GHz
Nonreflective 50 Ω design
Low insertion loss: 3.0 dB at 20 GHz
High isolation: 40 dB at 20 GHz
High input linearity at 250 MHz to 20 GHz
P1dB: 24 dBm typical
IP3: 41 dBm typical
High power handling
26.5 dBm through path
23 dBm terminated path
Integrated 2 to 4 line decoder
24-lead, 4 mm × 4 mm LFCSP package
ESD rating: 250 V (Class 1A)
APPLICATIONS
Test instrumentation
Microwave radios and very small aperture terminals (VSATs)
Military radios, radars, and electronic counter measures (ECMs)
Broadband telecommunications systems
GENERAL DESCRIPTION

The HMC641ALP4E is a general-purpose, nonreflective, single-pole, four-throw (SP4T) switch manufactured using a gallium arsenide (GaAs) process. This switch offers high isolation, low insertion loss, and on-chip termination of the isolated ports.

The switch operates with a negative supply voltage range of -5 V to -3 V and requires two negative logic control voltages.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

The HMC641ALP4E includes an on-chip, binary 2 to 4 line decoder that provides logic control from two logic input lines.

The HMC641ALP4E comes in a 4 mm × 4 mm, 24-lead LFCSP package and operates from 0.1 GHz to 20 GHz.

TABLE OF CONTENTS

Features	1	Interface Schematics	5
Applications.....	1	Typical Performance Characteristics	6
Functional Block Diagram	1	Insertion Loss, Return Loss, and Isolation	6
General Description	1	Input Power Compression and IP3	7
Revision History	2	Theory of Operation	8
Specifications.....	3	Application Information.....	9
Absolute Maximum Ratings.....	4	Evaluation Board	9
Power Derating Curves.....	4	Outline Dimensions	11
ESD Caution.....	4	Ordering Guide	11
Pin Configuration and Function Descriptions.....	5		

REVISION HISTORY

8/2018—Rev. A to Rev. B

Changes to Insertion Loss, Between RFC and RF1 to RF4 (On) Parameter, Table 1.....	3
Changed Reflow (MSL1 Rating) to Reflow, Table 2.....	4
Deleted Note 2, Table 2; Renumbered Sequentially.....	4
Updated Outline Dimensions	11
Changes to Ordering Guide	11

7/2017—Rev. 00.1013 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Changes to Features Section, Applications Section, General Description Section, and Figure 1	1
Deleted Truth Table, Bias Voltage and Current Table, and TTL/CMOS Control Voltages Table	3
Changes to Table 1	3

Added Power Derating Curves Section and Figure 2; Renumbered Sequentially	4
Changes to Table 2.....	4
Added Figure 4.....	5
Changes to Figure 3, Table 3, and Figure 5	5
Deleted GND Interface Schematic.....	5
Changes to Typical Performance Characteristics Section	6
Added Theory of Operation Section and Table 4; Renumbered Sequentially	8
Added Applications Information Section and Figure 14	9
Changes to Table 5.....	9
Added Figure 16	10
Updated Outline Dimensions	11
Changes to Ordering Guide	11

SPECIFICATIONS

$V_{SS} = -3\text{ V}$ or -5 V , $V_{CTRL} = 0\text{ V}$ or V_{SS} , $T_{CASE} = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS						
Between RFC and RF1 to RF4 (On)		0.1 GHz to 12 GHz		2.0	3.2	dB
		12 GHz to 20 GHz		3.0	4.2	dB
ISOLATION						
Between RFC and RF1 to RF4 (Off)		0.1 GHz to 12 GHz	30	42		dB
		12 GHz to 20 GHz	30	40		dB
RETURN LOSS						
RFC and RF1 to RF4 (On)		0.1 GHz to 12 GHz		18		dB
		12 GHz to 20 GHz		17		
RF1 to RF4 (Off)		0.1 GHz to 20 GHz		13		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		30		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		100		ns
INPUT LINEARITY ¹		250 MHz to 20 GHz				
1 dB Power Compression	P1dB	$V_{SS} = -5\text{ V}$	20	24		dBm
		$V_{SS} = -3\text{ V}$		22		dBm
Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		$V_{SS} = -5\text{ V}$		41		dBm
		$V_{SS} = -3\text{ V}$		41		dBm
SUPPLY		V_{SS} pin				
Voltage	V_{SS}		-5		-3	V
Current	I_{SS}			1.7	5	mA
DIGITAL CONTROL INPUTS		CTRLA and CTRLB pins				
Voltage	V_{CTL}					
Low	V_{INL}	$V_{SS} = -5\text{ V}$	-3		0	V
		$V_{SS} = -3\text{ V}$	-1		0	V
High	V_{INH}	$V_{SS} = -5\text{ V}$	-5		-4.2	V
		$V_{SS} = -3\text{ V}$	-3		-2.2	V
Current	I_{CTL}					
Low	I_{INL}			30		μA
High	I_{INH}			0.5		μA

¹ Input linearity performance degrades at frequencies less than 250 MHz.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Negative Supply Voltage (V_{SS})	-7 V
Digital Control Input Voltage	$V_{SS} - 0.5 \text{ V}$ to +1 V
RF Input Power ¹ ($f = 250 \text{ MHz}$ to 20 GHz, $T_{CASE} = 85^\circ\text{C}$)	
$V_{SS} = -5 \text{ V}$	
Through Path	26.5 dBm
Terminated Path	23 dBm
Hot Switching	20 dBm
$V_{SS} = -3 \text{ V}$	
Through Path	21 dBm
Terminated Path	20 dBm
Hot Switching	17 dBm
Temperature	
Junction, T_J	150°C
Storage	-65°C to +150°C
Reflow	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	201°C/W
Terminated Path	321°C/W
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

¹ For power derating at frequencies less than 250 MHz, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

POWER DERATING CURVES

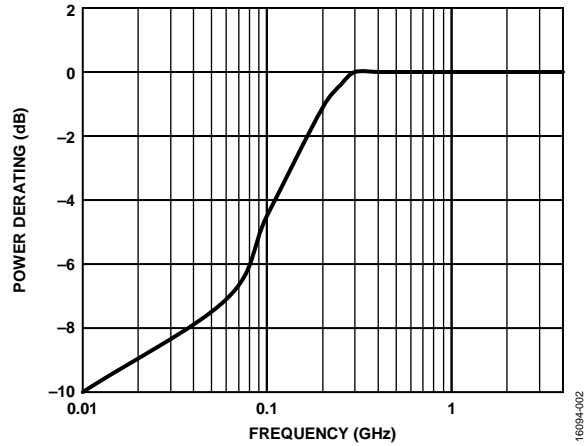


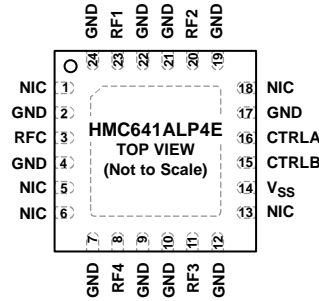
Figure 2. Power Derating at Frequencies Less than 250 MHz

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. NIC = NOT INTERNALLY CONNECTED. THE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA SHOWN IN THIS DATA SHEET IS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.
 2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF/DC GROUND OF THE PCB.

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 6, 13, 18	NIC	Not Internally Connected. The pins are not connected internally; however, all data shown in this data sheet is measured with these pins connected to RF/dc ground externally.
2, 4, 7, 9, 10, 12, 17, 19, 21, 22, 24	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
8	RF4	RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
11	RF3	RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
14	V _{ss}	Negative Supply Voltage Pin.
15	CTRLB	Control Input 2 Pin. See Table 4 for the control voltage truth table.
16	CTRLA	Control Input 1 Pin. See Table 4 for the control voltage truth table.
20	RF2	RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
23	RF1	RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

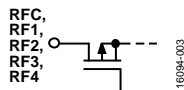


Figure 4. RFC to RF4 Interface Schematic

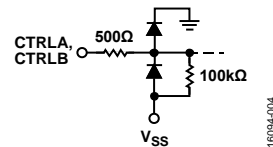


Figure 5. CTRLA and CTRLB Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS
INSERTION LOSS, RETURN LOSS, AND ISOLATION

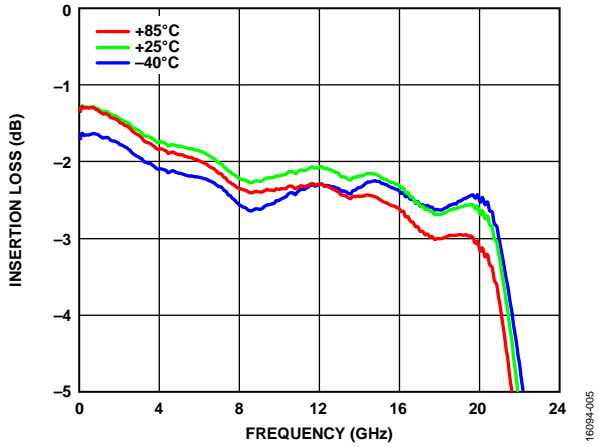


Figure 6. Insertion Loss Between RFC and RF1 vs. Frequency at Various Temperatures

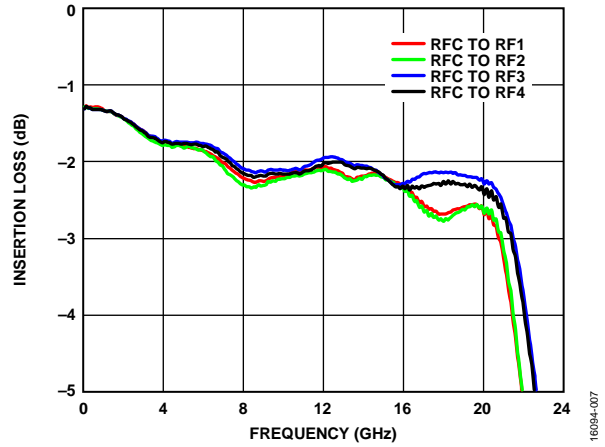


Figure 8. Insertion Loss Between RFC to RFx vs. Frequency

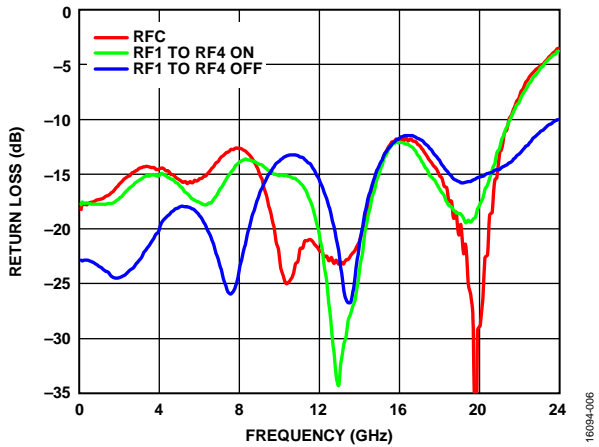


Figure 7. Return Loss for RFC, RF1 to RF4 On, and RF1 to RF4 Off vs. Frequency

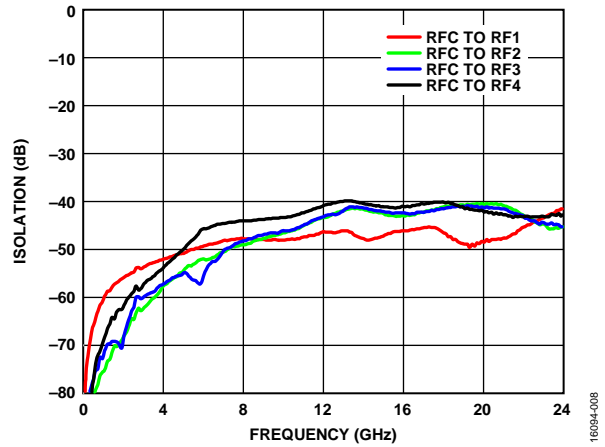


Figure 9. Isolation Between RFC and RFx vs. Frequency

INPUT POWER COMPRESSION AND IP3

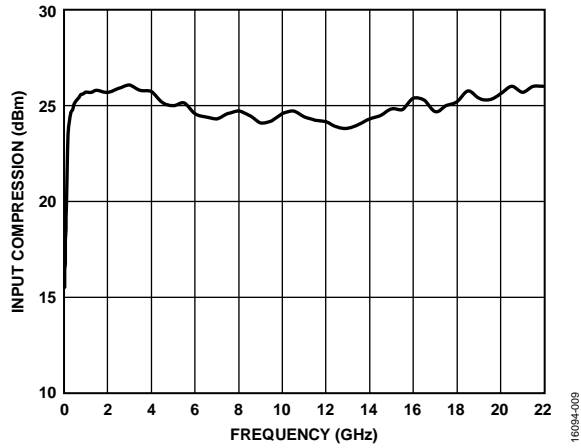


Figure 10. Input Compression vs. Frequency at Room Temperature, $V_{SS} = -5V$

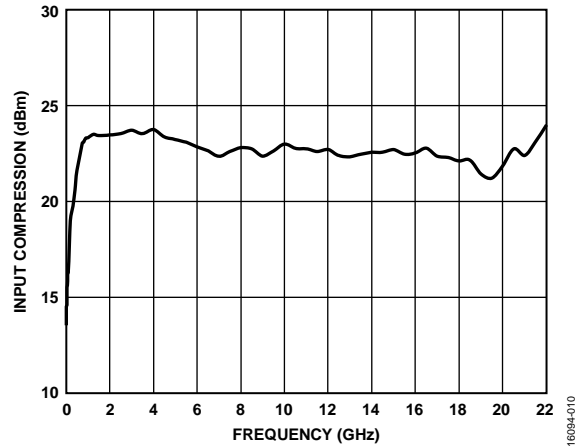


Figure 12. Input Compression vs. Frequency at Room Temperature, $V_{SS} = -3V$

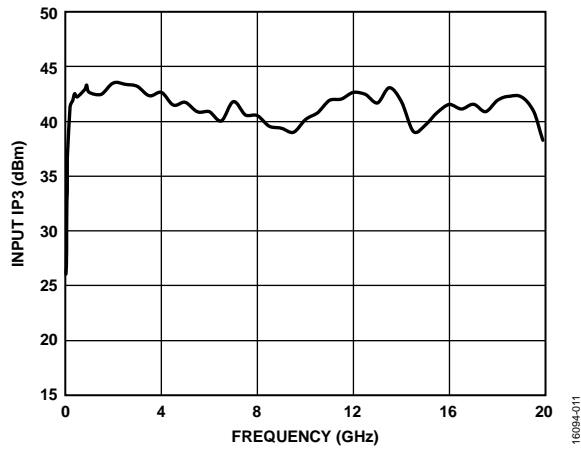


Figure 11. Input IP3 vs. Frequency at Room Temperature, $V_{SS} = -5V$

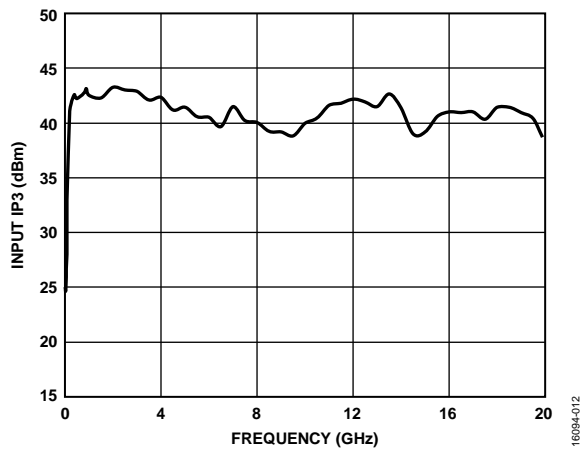


Figure 13. Input IP3 vs. Frequency at Room Temperature, $V_{SS} = -3V$

THEORY OF OPERATION

The HMC641ALP4E requires a negative supply voltage at the V_{SS} pin and two logic control inputs at the CTRLA and CTRLB pins to control the state of the RF paths.

Depending on the logic level applied to the CTRLA pin and the CTRLB pin, one RF path is in the insertion loss state while the other three paths are in an isolation state (see Table 4). The insertion loss path conducts the RF signal between the RF throw pin and RF common pin while the isolation paths provide high loss between RF throw pins terminated to internal 50 Ω resistors and the insertion loss path.

The ideal power-up sequence is as follows:

1. Ground to the die bottom.
2. Power up V_{SS} .
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{SS} supply can inadvertently become forward-biased and damage the internal ESD protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC pin while the RF throw pins are the outputs, or the RF input signal can be applied to the RF throw pins while the RFC pin is the output. All of the RF pins are dc-coupled to 0 V, and no dc blocking is required at the RF pins when the RF line potential is equal to 0 V.

The power-down sequence is the reverse of the power-up sequence.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths			
CTRLA	CTRLB	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)

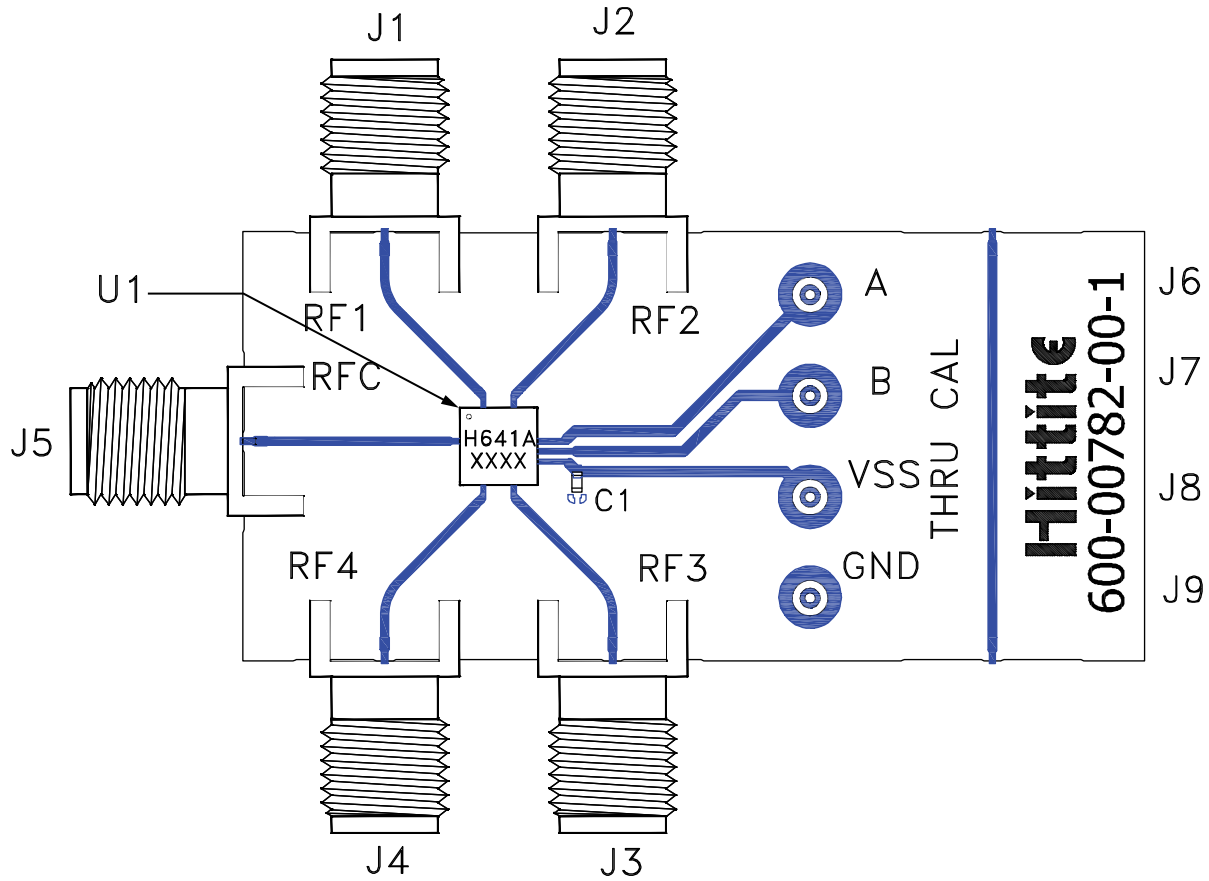


Figure 15. The EV1HMC641ALP4 Evaluation Board Component Placement

16094-014

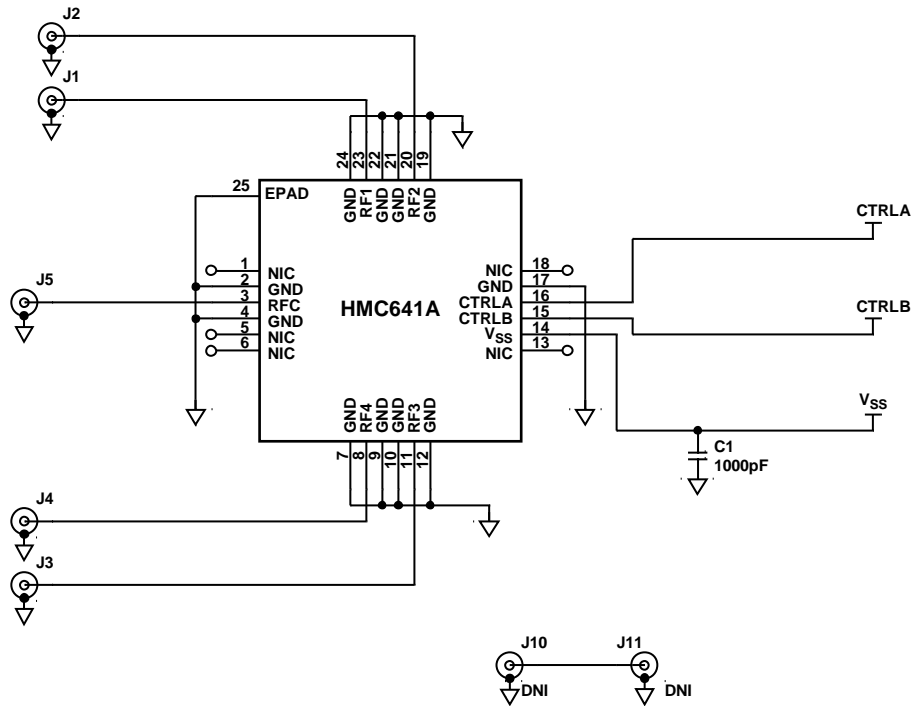


Figure 16. The EV1HMC641ALP4 Evaluation Board Schematic

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OUTLINE DIMENSIONS

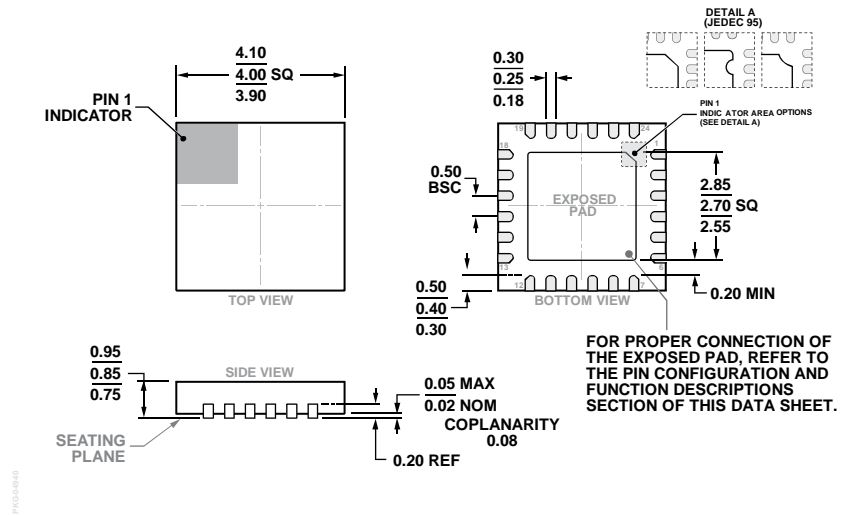


Figure 17. 24-Terminal Lead Frame Chip Scale Package [LFCSP]
 4 mm × 4 mm Body and 0.90 mm Package Height
 (HCP-24-3)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
HMC641ALP4E	−40°C to +85°C	24-Terminal Lead Frame Chip Scale Package [LFCSP]	HCP-24-3
HMC641ALP4ETR	−40°C to +85°C	24-Terminal Lead Frame Chip Scale Package [LFCSP]	HCP-24-3
EV1HMC641ALP4		Evaluation Board	

¹ All models are RoHS compliant.