National Semiconductor

# 74FR245
# Octal Bidirectional Transceiver with TRI-STATE® Outputs

## General Description

The 'FR245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 64 mA on both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

## Features

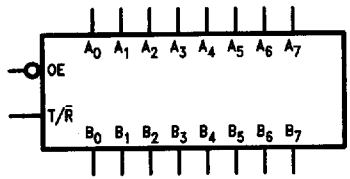
- Non-inverting buffers
- Bidirectional data path
- A and B output sink capability of 64 mA, source capability of 15 mA
- Guaranteed 4000V minimum ESD protection
- Guaranteed pin to pin skew

## Ordering Code: See Section 11

| Commercial | Package Number | Package Description |
|---|---|---|
| 74FR245PC | N20A | 20-Lead (0.300" Wide) Molded Dual-In-Line |
| 74FR245SC (Note 1) | M20B | 20-Lead (0.300" Wide) Molded Small Outline, JEDEC |
| 74FR245SJ (Note 1) | M20D | 20-Lead (0.300" Wide) Molded Small Outline, EIAJ |

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

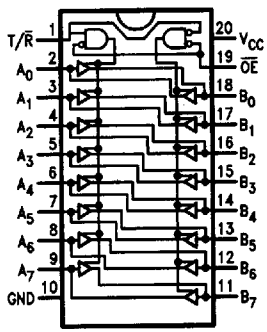
## Logic Symbol




TL/F/10887–1

## Connection Diagram

**Pin Assignment for DIP and SOIC**




TL/F/10887–2

## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| $T/\overline{R}$ | Transmit/Receive Input |
| $A_0$–$A_7$ | Side A Inputs or TRI-STATE Outputs |
| $B_0$–$B_7$ | Side B Inputs or TRI-STATE Outputs |

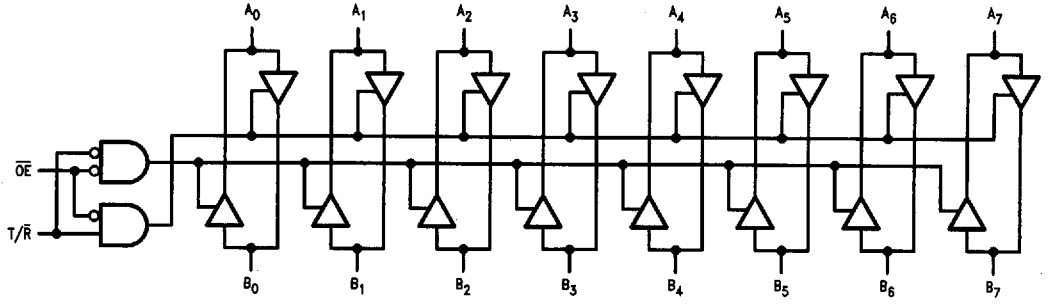
## Truth Table

| Inputs | | Output |
|---|---|---|
| $\overline{OE}$ | $T/\overline{R}$ | |
| L | L | Bus B Data to Bus A |
| L | H | Bus A Data to Bus B |
| H | X | High Z State |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

## Logic Diagram

'FR245




TL/F/10887–3

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | |
| Ceramic | −55°C to +175°C |
| Plastic | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| TRI-STATE Output | −0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Commercial | +4.5V to +5.5V |

## DC Electrical Characteristics

| Symbol | Parameter | 74FR | | | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | Min | $I_{OH}$ = −3 mA ($A_n$, $B_n$) |
| | | 2.0 | | | V | Min | $I_{OH}$ = −15 mA ($A_n$, $B_n$) |
| $V_{OL}$ | Output LOW Voltage | | | 0.55 | V | Min | $I_{OL}$ = 64 mA ($A_n$, $B_n$) |
| $I_{IH}$ | Input HIGH Current | | | 5 | μA | Max | $V_{IN}$ = 2.7V ($\overline{OE}$, T/$\overline{R}$) |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | 7 | μA | Max | $V_{IN}$ = 7.0V ($\overline{OE}$, T/$\overline{R}$) |
| $I_{BVIT}$ | Input HIGH Current Breakdown Test (I/O) | | | 100 | μA | Max | $V_{IN}$ = 5.5V ($A_n$, $B_n$) |
| $I_{IL}$ | Input LOW Current | | | −250 | μA | Max | $V_{IN}$ = 0.5V ($\overline{OE}$, T/$\overline{R}$) |
| $V_{ID}$ | Input Leakage Test | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 μA All Other Pins Grounded |
| $I_{OD}$ | Output Circuit Leakage Current | | | 3.75 | μA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{IH} + I_{OZH}$ | Output Leakage Current | | | 25 | μA | Max | $V_{OUT}$ = 2.7V ($A_n$, $B_n$) |
| $I_{IL} + I_{OZL}$ | Output Leakage Current | | | −150 | μA | Max | $V_{OUT}$ = 0.5V ($A_n$, $B_n$) |
| $I_{OS}$ | Output Short-Circuit Current | −100 | | −225 | mA | Max | $V_{OUT}$ = 0.0V ($A_n$, $B_n$) |
| $I_{CEX}$ | Output High Leakage Current | | | 50 | μA | Max | $V_{OUT}$ = $V_{CC}$ ($A_n$, $B_n$) |
| $I_{ZZ}$ | Bus Drainage Test | | | 100 | μA | 0.0 | $V_{OUT}$ = 5.25V ($A_n$, $B_n$) |
| $I_{CCH}$ | Power Supply Current | | 55 | 75 | mA | Max | All Outputs HIGH |
| $I_{CCL}$ | Power Supply Current | | 75 | 110 | mA | Max | All Outputs LOW |
| $I_{CCZ}$ | Power Supply Current | | 55 | 75 | mA | Max | Outputs TRI-STATE |
| $C_{IN}$ | Input Capacitance | | 8.0 | | pF | 5.0 | $\overline{OE}$, T/$\overline{R}$ |
| | | | 17.0 | | pF | 5.0 | $A_n$, $B_n$ |

## AC Electrical Characteristics: See Section 2 for waveforms and load configurations

| Symbol | Parameter | 74FR $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | 74FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.0<br>1.0 | 2.6<br>1.7 | 3.9<br>3.9 | 1.0<br>1.0 | 3.9<br>3.9 | ns | 2–3 |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | 2.5<br>2.5 | 5.0<br>4.3 | 7.0<br>7.0 | 2.5<br>2.5 | 7.0<br>7.0 | ns | 2–5 |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | 1.7<br>1.7 | 3.7<br>3.6 | 6.5<br>6.5 | 1.7<br>1.7 | 6.5<br>6.5 | ns | 2–5 |

## Extended AC Characteristics: See Section 2 for waveforms and load configurations

| Symbol | Parameter | 74FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 50$ pF, Eight Outputs Switching (Note 2) | | 74FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 250$ pF (Note 3) | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.0<br>1.0 | 5.9<br>5.9 | 2.5<br>2.5 | 7.5<br>7.5 | ns | 2–3 |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time | 2.5<br>2.5 | 11.9<br>11.9 | | | ns | 2–5 |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time | 1.3<br>1.3 | 6.5<br>6.5 | | | ns | 2–5 |
| $t_{OSHL}$<br>(Note 1) | Pin to Pin Skew<br>for HL Transitions | | 1.7 | | | ns | |
| $t_{OSLH}$<br>(Note 1) | Pin to Pin Skew<br>for LH Transitions | | 1.0 | | | ns | |
| $t_{OST}$<br>(Note 1) | Pin to Pin Skew<br>for HL/LH Transitions | | 3.3 | | | ns | |

**Note 1:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching high to low ($t_{OSHL}$), low to high ($t_{OSLH}$), or high to low and/or low to high ($t_{OST}$). Specifications guaranteed with all outputs switching in phase.

**Note 2:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all low-to-high, high-to-low, TRI-STATE-to-high, etc.

**Note 3:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.