IS2083

IS2083 Bluetooth® Stereo Audio SoC Data Sheet

Introduction

The IS2083 is a System-on-Chip (SoC) for dual mode Bluetooth stereo audio applications. It contains an on-board Bluetooth stack, audio profiles and supports 24-bit/96 kHz high-resolution (Hi-Res) audio formats to enable high-fidelity wireless audio. An integrated Digital Signal Processor (DSP) decodes (LDAC, Advanced Audio Codec (AAC), and Sub-band Codec (SBC) codecs) and executes advanced audio and voice processing (wideband speech, Acoustic Echo Cancellation (AEC), and Noise Reduction (NR)). This platform provides a Microcontroller (MCU) core for application implementation via Software Development Kit (SDK) with debug support and a GUI (Config Tool) tool for easy customization of peripheral settings and DSP functionality.

Additionally, the Audio Transceiver (AT) solution enables Bluetooth capability in non-Bluetooth Audio equipment. The AT receives audio inputs through the Aux-In or I^2S pin and streams the audio to up to two Bluetooth paired sink devices.

Note: Contact your local sales representative for more information about the Software Development Kit (SDK).

The IS2083 SoC is offered in a BGA package and contains in-package Flash, and is referred to as IS2083BM.

The IS2083BM supports an Over-the-Air (OTA) firmware upgrade and controls the end-application via Bluetooth Low Energy using the Microchip Bluetooth Audio (MBA) mobile app.

Features

- Qualified for Bluetooth v5.0 specification
  - Hands-free Profile (HFP) 1.7.2, Headset Profile (HSP) 1.2, Advanced Audio Distribution Profile (A2DP) 1.3, Serial Port Profile (SPP) 1.2, Audio/Video Remote Control Profile (AVRCP) 1.6 and Phone Book Access Profile (PBAP) 1.2
  - Bluetooth classic (BR/EDR) and Bluetooth Low Energy
  - General Attribute Profile (GATT) and General Access Profile (GAP)
  - Bluetooth Low Energy Data Length Extension (DLE) and secure connection
- Software Development Kit
  - 8051 microcontroller debugging
  - 24-bit program counter and Data Pointer modes
- Multi-Speaker (MSPK) solution
  - Microchip's proprietary solution to connect a central speaker to one or more peripheral speakers
  - With MSPK firmware, the IS2083 can provide Concert mode and Stereo mode
- Audio Transceiver (AT) solution
  - With AT firmware, the IS2083 can work as either an A2DP source (where IS2083 is the transmitter) or A2DP/HFP sink (where IS2083 is a receiver)
- Audio Interfaces
  - Stereo line input
  - Two analog microphones
  - One stereo digital microphone
  - Stereo audio Digital-to-Analog Converter (DAC)
  - I^2S input/output

  - I^2S Primary clock (MCLK)/reference clock
- USB, UART and Over-the-Air (OTA) firmware upgrade
- Built-in lithium-ion and lithium polymer battery charger (up to 350 mA)
- Integrated 3V and 1.8V configurable switching regulator and Low-Dropout (LDO)

Radio Frequency (RF)/Analog

- Bluetooth 5.0 dual mode RF radio
- Receive sensitivity: -90 dBm (2 Mbps EDR)
- Programmable transmit output power:
  - Up to +11 dBm (typical) for Basic Data Rate (BDR)
  - Up to +9.5 dBm (typical) for Enhanced Data Rate (EDR)
- Integrated Medium Power Amplifier (MPA) and Low Power Amplifier (LPA)

MCU Features

- 8051 8-bit core
- 8-bit data
- 24-bit program counter (PC24) mode
- 24-bit data pointer (DPTR24) mode
- Operating speed:
  - DC – 48 MHz clock input
  - 0.33-1 MIPS/MHz, depending on instruction

DSP Voice and Audio Processing

- 16/32-bit DSP core with enhanced 32-bit precision, single cycle multiplier
- Synchronous Connection-Oriented (SCO) channel operation
- Modified Sub-Band Coding (mSBC) decoder for wideband speech
- Built-in High-definition Clean Audio (HCA) algorithms for both narrowband and wideband speech processing
- Built-in audio effect algorithms to enhance audio streaming
- 64 Kbps A-Law, μ-Law Pulse Code Modulation (PCM) or Continuous Variable Slope Delta (CVSD) modulation for SCO channel operation
- 8/16 kHz Noise Reduction (NR)
- 8/16 kHz Acoustic Echo Cancellation (AEC)
- Packet Loss Concealment (PLC) for SBC and mSBC codecs only

Audio Codec

- Sub-band Codec (SBC), Advanced Audio Codec (AAC) and LDAC Decoding (IS2083BM-2L2 only)
- 20-bit audio stereo DAC with SNR 95 dB
- 16-bit audio stereo ADC with SNR 90 dB
- 24-bit, I^2S digital audio:
  - 96 kHz output sampling frequency
  - 48 kHz input sampling frequency

Peripherals

- Successive Approximation Register Analog-to-Digital Converter (SAR ADC) with dedicated channels:
  - Battery voltage detection and adapter voltage detection
  - Charger thermal protection and ambient temperature detection
- UART (with hardware flow control)
- USB (full-speed USB 1.1 interface)
- $I^2C™$ Host
- One Pulse Width Modulation (PWM) channel

- Two LED drivers
- Up to 19 General Purpose Inputs/Outputs (GPIOs)

8051 MCU Debug Features

- Two-wire 8051 MCU Joint Test Action Group (JTAG) debug
- CPU registers to write Flash for software downloading
- Debug features supported
  - Run/Stop control
  - Single Step mode
  - Software breakpoint
  - Debug program
  - Hardware breakpoint
  - Program trace
  - Access to ACC

Operating Condition

- Operating voltage: 3.2V to 4.2V
- Operating temperature: -40ºC to +85ºC

Applications

- Portable speakers
- Multiple speakers
- Headphones
- Bluetooth audio transmitter

Compliance

- Bluetooth Special Interest Group (SIG) QDID: 134083 (Class1) and 134099 (Class2)

Table of Contents

1. Quick References

1.1 Reference Documentation

For further information, refer to the following:

- *BM83 Bluetooth® Stereo Audio Module Data Sheet* (DS70005402)
- *BM83 Bluetooth® Audio Development Board User's Guide* (DS50002902)
- *IS2083 SDK User Guide* (DS50002894)
- *BM83 Host MCU Firmware Development Guide* (DS50002896)
- *IS2083/BM83 Bluetooth® Application Design Guide* (DS00003118)
- *IS2083 SDK Debugger User's Guide* (DS50002892)
- *IS2083 Reference Design Application Note*
- *IS2083/BM83 Battery Charger Application Note* (AN3490)
- *Serial Quad Interface (SQI) Family Reference Manual* (DS60001244)

Notes:

1. For a complete list of development support tools and documents, visit:
   - www.microchip.com/BM83
   - www.microchip.com/IS2083
2. Contact your local sales representative for more information about the Software Development Kit (SDK).

1.2 Acronyms/Abbreviations

Table 1-1. Acronyms/Abbreviations

Acronyms/Abbreviations	Description
A2DP	Advanced Audio Distribution Profile
AAC	Advanced Audio Codec
ADC	Analog-to-Digital Converter
AEC	Acoustic Echo Cancellation
AFH	Adaptive Frequency Hopping
ANCS	Apple Notification Center Service
API	Application Programming Interfaces
AVRCP	Audio/Video Remote Control Profile
AW	Audio Widening
BDR	Basic Data Rate
BER	Bit Error Rate
BLE	Bluetooth Low Energy
BOM	Bill of Materials
BPF	Band Pass Filter
BR	Basic Rate
CVSD	Continuous Variable Slope Delta
DAC	Digital-to-Analog Converter
DFU	Device Firmware Upgrade
DIS	Device Information Service

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Acronyms/Abbreviations	Description
DLE	Data Length Extension
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DR	Receive Data
DSP	Digital Signal Processor
DT	Transmit Data
EDR	Enhanced Data Rate
EMC	Electromagnetic Compatibility
EVB	Evaluation Board
FET	Field Effect Transistor
GAP	General Access Profile
GATT	General Attribute Profile
GFSK	Gaussian Frequency Shift Keying
GPIO	General Purpose Input Output
GUI	Graphical User Interface
HFP	Hands-Free Profile
HPF	High Pass Filter
HSP	Headset Profile
HW	Hardware
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IC	Integrated Circuit
ICSP™	In-Circuit Serial Programming™
IDE	Integrated Development Environment
IF	Intermediate Frequency
IPE	Integrated Programming Environment
JTAG	Joint Test Action Group
LDO	Low-Dropout
LED	Light Emitting Diode
LNA	Low-Noise Amplifier
LPA	Linear Power Amplifier
LSB	Least Significant Bit
MAC	Medium Access Control
MB DRC	Multi-Band Dynamic Range Compression
MCLK	Primary Clock
MCU	Microcontroller
MEMS	Micro-Electro-Mechanical Systems
MFB	Multi-Function Button
Modem	Modulator-demodulator
MPA	Medium Power Amplifier

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Acronyms/Abbreviations	Description
mSBC	Modified Sub-Band Coding
MSPK	Multi-Speaker
NR	Noise Reduction
OTA	Over-the-Air
PBAP	Phone Book Access Profile
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PIM	Plug-In Module
PLC	Packet Loss Concealment
PMU	Power Management Unit
POR	Power-On Reset
PWM	Pulse Width Modulation
RF	Radio Frequency
RFS	Receive Frame Sync
RoHS	Restriction of Hazardous Substances
RSSI	Received Signal Strength Indicator
RX	Receiver
SAR	Successive Approximation Register
SBC	Sub-Band Coding
SCO	Synchronous Connection-Oriented
SDK	Software Development Kit
SIG	Special Interest Group
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SPP	Serial Port Profile
SW	Software
TX	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UI	User Interface
USB	Universal Serial Bus
VB	Virtual Bass Enhancement
VCO	Voltage-Controlled Oscillator
WDT	Watchdog Timer

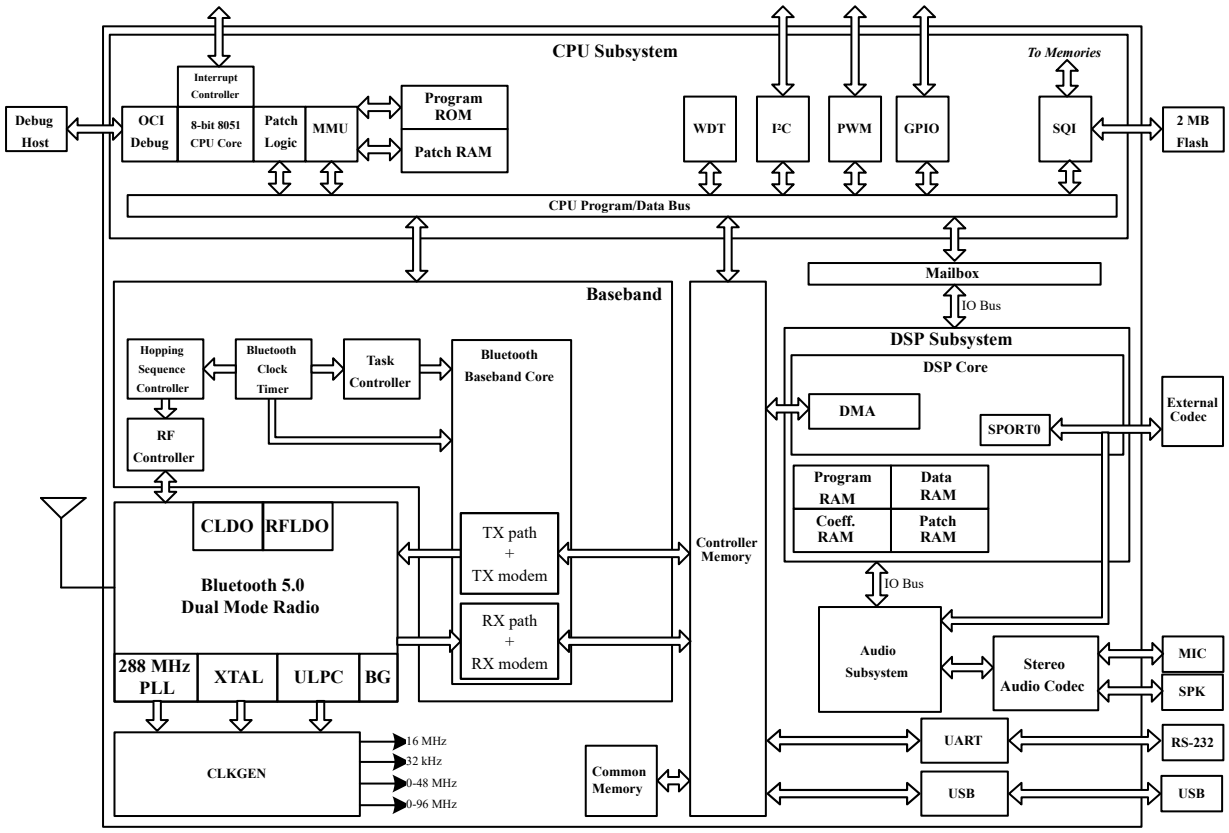
2. Device Overview

The IS2083BM uses a single-cycle 8-bit 8051 MCU core connected to the system components via an MCU system bus. The MCU system bus provides interface memory map address decode for the Read Only Memory (ROM), Static Random Access Memory (SRAM), and peripherals.

IS2083BM contains the following major blocks:

- Bluetooth Link Controller (BTLC) – Bluetooth clock, task scheduler, and Bluetooth hopping
- Bluetooth modulator-demodulator (modem) – TX/RX baseband and RF
- DSP audio subsystem – DSP with audio codec
- Program ROM Memory
- Bluetooth DMA – Common Memory Access
- Power Management Unit (PMU)
- Clock/Reset – Low power logic

Figure 2-1. IS2083BM SoC Architecture



The IS2083BM device variants are:

- IS2083BM variant supports analog output from the internal DAC
- IS2083BM-2L2 variant supports LDAC and does not support analog output

The following table provides the features of IS2083BM SoC variants.

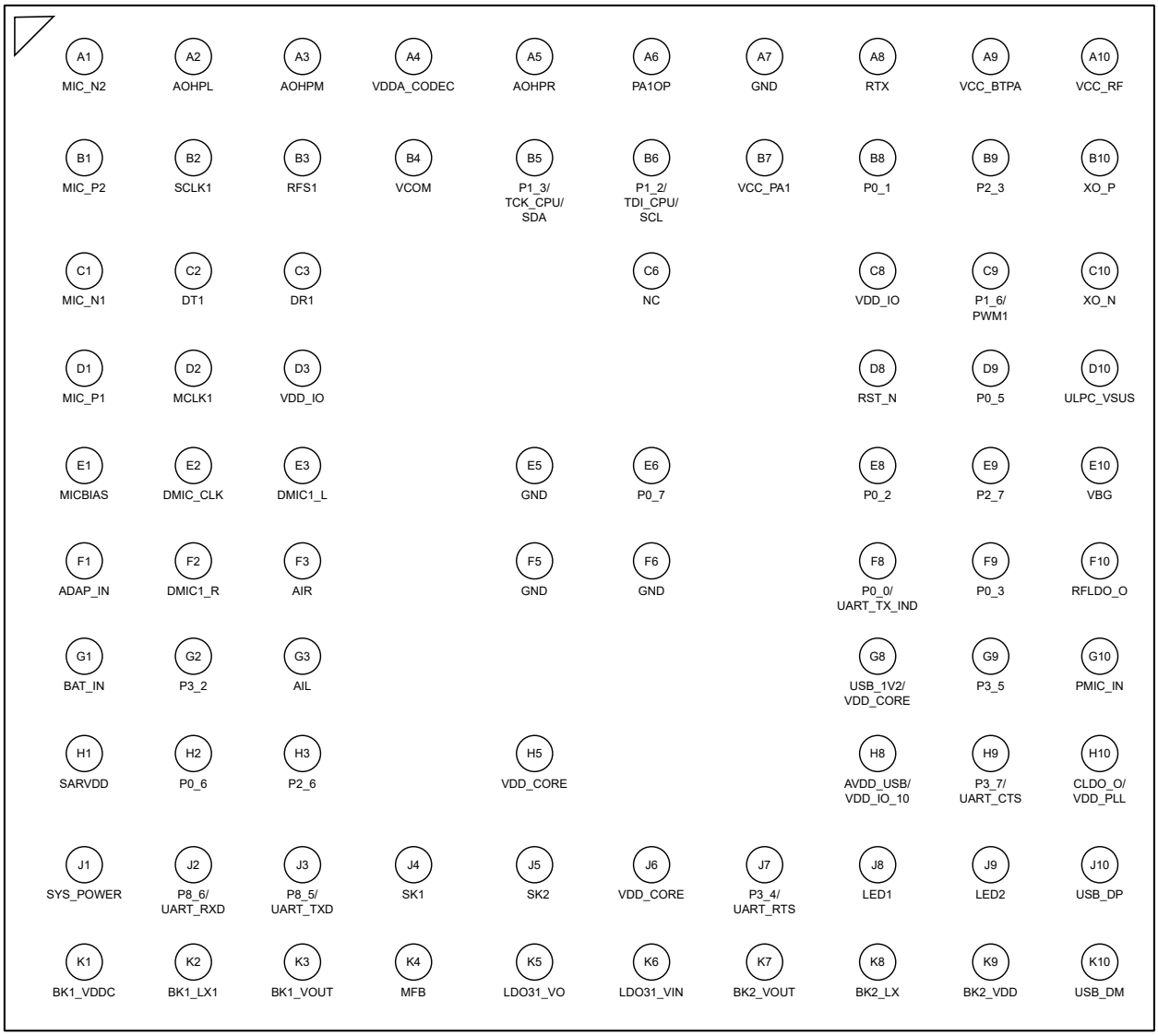
Table 2-1. IS2083BM Features

Features	IS2083BM	IS2083BM-2L2
Application	• Headset/Speaker • Bluetooth Audio Transmitter	Headset/Speaker
Memory	Flash	Flash
Stereo/Concert mode	Yes	Yes
Package	BGA	BGA
Pin/Ball count	82	82
Dimensions	5.5 mm x 5.5 mm	5.5 mm x 5.5 mm
Audio DAC output	2 channel	—
DAC (single-ended) SNR	95 dB	—
DAC (cap-less) SNR	95 dB	—
ADC SNR at 1.8V	-88 dB	-88 dB
I^2S audio input	Yes	Yes
I^2S digital output	Yes	Yes
MCLK output	Yes	Yes
Analog output	Yes	—
Analog Line-In	Yes	Yes
Analog microphone	2 channel	2 channel
Digital microphone	2 channel	2 channel
External audio amplifier interface	Yes	Yes
UART with hardware flow control	1	1
USB (Full-speed USB 1.1 interface and battery charging)	Yes	Yes
I^2C	1	1
PWM	1 channel	1 channel
LED driver	2	2
Battery charger (350 mA maximum)	Yes	Yes
ADC for battery voltage and temperature monitoring	Yes	Yes
GPIO	Up to 19	Up to 19
Multitone	Yes	Yes
Integrated MPA and LPA	Yes	Yes

2.1 IS2083BM Device Ball Diagram

The following figure illustrates the ball diagram of the IS2083BM and IS2083BM-2L2.

Figure 2-2. IS2083BM and IS2083BM-2L2 Ball Diagram



Note: The IS2083BM-2L2 does not support an analog output from the internal DAC. The AOHPR, AOHPM and AOHPL are affected pins.

2.2 IS2083BM Device Ball Description

Table 2-2. IS2083BM and IS2083BM-2L2 Ball Description

IS2083BM Ball Number	IS2083BM-2L2 Ball Number	Ball Name	Ball Type	Description
A1	A1	MIC_N2	I	MIC2 mono differential analog negative input
A2	—	AOHPL(1)	O	Left channel, analog headphone output
A3	—	AOHPM(1)	O	Headphone common mode output/sense input

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IS2083BM Ball Number	IS2083BM-2L2 Ball Number	Ball Name	Ball Type	Description
A4	A4	VDDA_CODEC	P	• Analog audio codec power supply (1.8V) • Connect to BK2_VOUT pin
A5	—	AOHPR(1)	O	Right channel, analog headphone output
A6	A6	PA1OP	I/O	RF output pin for MPA
A7	A7	GND	P	Ground reference
A8	A8	RTX	I/O	• RF path (transmit/receive) • TX LPA output multiplexed with RX LNA input
A9	A9	VCC_BTPA	P	• Power supply for RF power amplifier • Connect to BK1_VOUT
A10	A10	VCC_RF	P	• RF power input (1.28V) for both synthesizer and TX/RX block • Connect to RFLDO_O
B1	B1	MIC_P2	I	MIC2 mono differential analog positive input
B2	B2	SCLK1	I/O	I^2S interface for bit clock
B3	B3	RFS1	I/O	I^2S interface for DAC digital left/right clock
B4	B4	VCOM	P	• Internal biasing voltage for codec • Connect a 4.7 µF capacitor to ground
B5	B5	P1_3/ TCK_CPU/ SDA	I/O	• General purpose I/O port P1_3 • CPU two-wire debug clock • I^2C SDA
B6	B6	P1_2/ TDI_CPU/ SCL	I/O	• General purpose I/O port P1_2 • CPU two-wire debug data • I^2C SCL
B7	B7	VCC_PA1	P	• Power supply for MPA • Connect to BK1_VOUT
B8	B8	P0_1	I/O	• General purpose I/O port P0_1 • By default, this is configured as forward button (user configurable button)
B9	B9	P2_3	I/O	General purpose I/O port P2_3
B10	B10	XO_P	I	16 MHz crystal positive input
C1	C1	MIC_N1	I	MIC1 mono differential analog negative input
C2	C2	DT1	O	I^2S interface: ADC digital left/right data
C3	C3	DR1	I/O	I^2S interface: DAC digital left/right data
C6	C6	NC	—	Not connected

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IS2083BM Ball Number	IS2083BM-2L2 Ball Number	Ball Name	Ball Type	Description
C8	C8	VDD_IO	P	• I/O power supply input • Connect to ground through a 1 µF (X5R/X7R) capacitor
C9	C9	P1_6/ PWM1	I/O	• General purpose I/O port P1_6 • PWM1 output
C10	C10	XO_N	I	16 MHz crystal negative input
D1	D1	MIC_P1	I	MIC1 mono differential analog positive input
D2	D2	MCLK1	O	Primary clock output provided to an external I^2S device/codec
D3	D3	VDD_IO	P	• I/O power supply input • Connect to LDO31_VO and ground through a 1 µF (X5R/X7R) capacitor
D8	D8	RST_N	I	System Reset pin (active-low)
D9	D9	P0_5	I/O	• General purpose I/O port P0_5 • By default, this is configured as volume down button (user configurable button)
D10	D10	ULPC_VSUS	P	• 1.2V ULPC output power • Maximum loading 1 mA • Connect to ground through a 1 µF capacitor
E1	E1	MICBIAS	P	Electric microphone biasing voltage
E2	E2	DMIC_CLK	O	Digital microphone clock
E3	E3	DMIC1_L	I	Digital microphone left channel
E5	E5	GND	P	Ground reference
E6	E6	P0_7	I/O	General purpose I/O port P0_7
E8	E8	P0_2	I/O	• General purpose I/O port P0_2 • By default, this is configured as play/ pause button (user configurable button)
E9	E9	P2_7	I/O	• General purpose I/O port P2_7 • By default, this is configured as volume up button (user configurable button)
E10	E10	VBG	P	• Bandgap output reference for decoupling interference • Connect to ground through a 1 µF capacitor
F1	F1	ADAP_IN	P	5V power adapter input to charge the battery in the battery powered applications
F2	F2	DMIC1_R	I	Digital microphone right channel
F3	F3	AIR	I	Right channel, single-ended analog input

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IS2083BM Ball Number	IS2083BM-2L2 Ball Number	Ball Name	Ball Type	Description
F5	F5	GND	P	Ground reference
F6	F6	GND	P	Ground reference
F8	F8	P0_0/ UART_TX_IND	I/O	• General purpose I/O port P0_0 • By default, this is configured as an external codec reset (Embedded mode) • UART_TX_IND (active-high); used to wake-up host MCU (Host mode)
F9	F9	P0_3	I/O	• General purpose I/O port P0_3 • By default, this is configured as reverse button (user configurable button)
F10	F10	RFLDO_O	P	• 1.28V RF LDO output for internal use only • Connect to ground through a 1 µF capacitor
G1	G1	BAT_IN	P	• Input power supply • Source can either be a battery or any other power rail on the host board
G2	G2	P3_2	I/O	• General purpose I/O port P3_2 • By default, this is configured as AUX_IN DETECT
G3	G3	AIL	I	Left channel, single-ended analog input
G8	G8	USB_1V2/ VDD_CORE	P	• 1.2V core power input • Connect to ground through a 1 µF (X5R/X7R) capacitor
G9	G9	P3_5	I/O	General purpose I/O port P3_5
G10	G10	PMIC_IN	P	• 1.8V power input for internal blocks • Connect to BK1_VOUT
H1	H1	SARVDD	P	• SAR ADC 1.8V input • Connect to BK2_O pin
H2	H2	P0_6	I/0	General purpose I/O port P0_6
H3	H3	P2_6	I/O	General purpose I/O port P2_6
H5	H5	VDD_CORE	P	• Core 1.2V power input • Connect to CLDO_O pin
H8	H8	AVDD_USB/ VDD_IO_10	P	• USB power input • Connect to LDO31_VO pin • Do not connect if USB functionality is not required

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IS2083BM Ball Number	IS2083BM-2L2 Ball Number	Ball Name	Ball Type	Description
H9	H9	P3_7/ UART_CTS	I/O	• General purpose I/O port P3_7 (this pin should not be pulled low during start-up) • UART CTS
H10	H10	CLDO_O/ VDD_PLL	P	• 1.2V core LDO output for internal use only • Connect to ground through a 1 µF capacitor
J1	J1	SYS_POWER	P	• System power output derived from the ADAP_IN or BAT_IN input • Do not connect to any other devices • Only for internal use
J2	J2	P8_6/ UART_RXD	I/O	• General purpose I/O port P8_6 • UART data input
J3	J3	P8_5/ UART_TXD	I/O	• General purpose I/O port P8_5 • UART data output
J4	J4	SK1	I	ADC channel 1
J5	J5	SK2	I	ADC channel 2
J6	J6	VDD_CORE	P	• 1.2V core input power supply • Connect to ground through a 1 µF (X5R/X7R) capacitor
J7	J7	P3_4/ UART_RTS	I/O	• General purpose I/O port P3_4 • System configuration pin (Application mode or Test mode) • UART RTS
J8	J8	LED1	O	LED driver 1
J9	J9	LED2	O	LED driver 2
J10	J10	USB_DP	I/O	Differential data-plus USB
K1	K1	BK1_VDDC	P	• 1.5V buck VDD power input • Connect to SYS_POWER pin
K2	K2	BK1_LX1	P	1.5V buck regulator feedback path
K3	K3	BK1_VOUT	P	• 1.5V buck regulator output • Do not connect to other devices • Only for internal use
K4	K4	MFB	I	Multifunction push button and Power On key
K5	K5	LDO31_VO	P	• 3V LDO output for VDD_IO power • Do not calibrate
K6	K6	LDO31_VIN	P	• LDO input • Connect to SYS_POWER

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IS2083BM Ball Number	**IS2083BM-2L2 Ball Number**	**Ball Name**	**Ball Type**	**Description**
K7	K7	BK2_VOUT	P	• 1.8V buck regulator output • Do not connect to other devices • Only for internal use
K8	K8	BK2_LX	P	1.8V buck regulator feedback path
K9	K9	BK2_VDD	P	• 1.8V buck VDD power input • Connect to SYS_POWER pin
K10	K10	USB_DM	I/O	Differential data-minus USB

Notes:

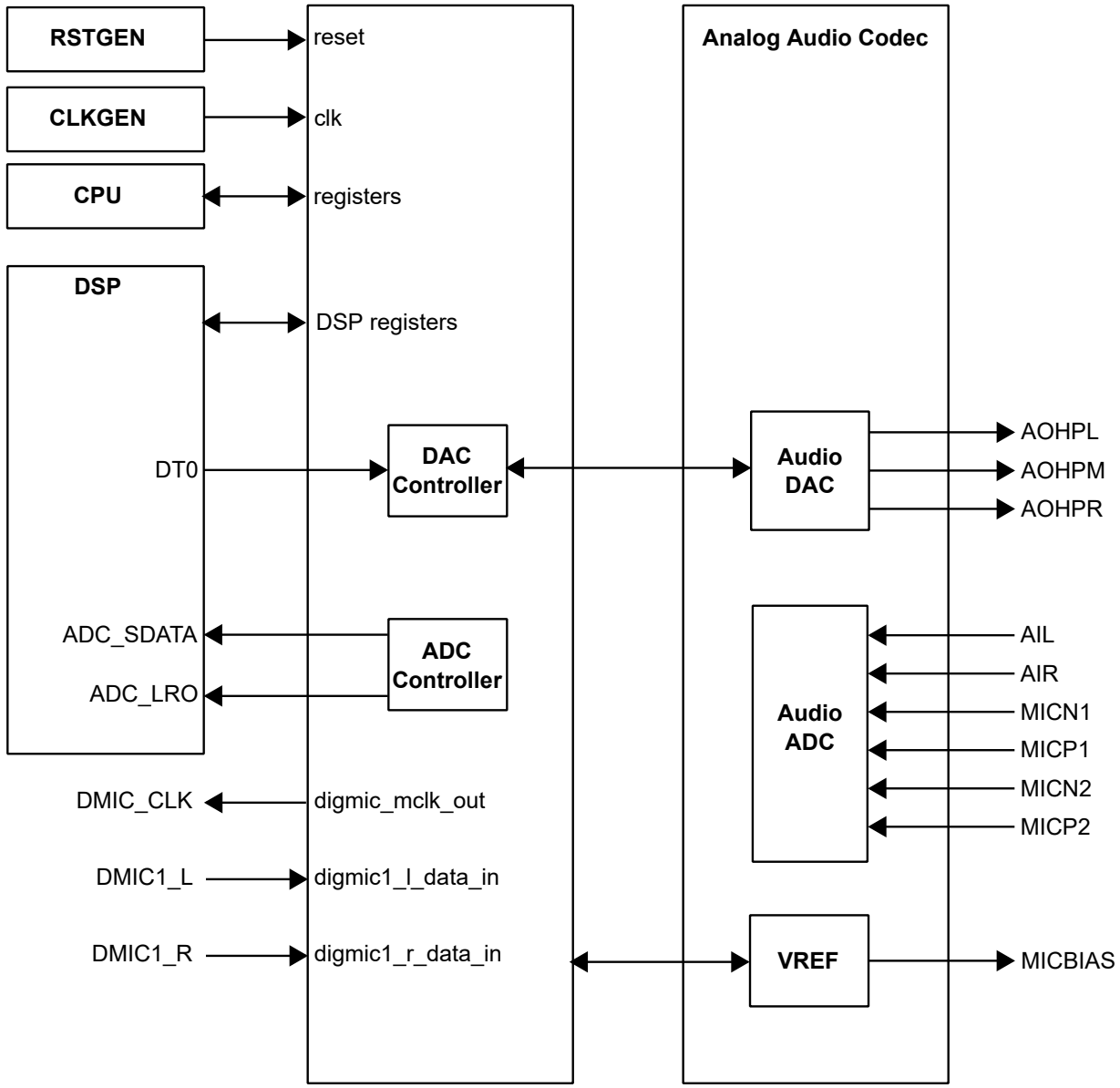
1. The AOHPR, AOHPM and AOHPL pins are not available in the IS2083BM-2L2 variant as it does not support an analog output from the internal DAC.
2. The conventions used in the preceding table are indicated as follows:
   – I = Input pin
   – O = Output pin
   – I/O = Input/Output pin
   – P = Power pin

3. Audio Subsystem

The input and output audio have different stages and each stage can be programmed to vary the gain response characteristics. For microphones, both single-ended inputs and differential inputs are supported. To maintain a high-quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors can be used at both positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

The following figure shows the audio subsystem.

Figure 3-1. Audio Subsystem



Note: The AOHPL, AOHPM, AOHPR pins are not available in the IS2083BM-2L2 variant.

3.1 Digital Signal Processor

A Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as AES and NR are inbuilt. To reduce nonlinear distortion and to help echo cancellation, an outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. In addition, adaptive filtering is applied to track the echo path impulse in response to provide echo free and full-duplex user experience.

The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by the microphones and improves mutual understanding in communication. The advanced audio features, such as multiband dynamic range control, parametric multiband equalizer, audio widening and virtual bass are inbuilt. The audio effect algorithms improve the user's audio listening experience in terms of better-quality audio after audio signal processing.

Note: DSP parameters can be configured using the Config Tool.

The following figures illustrate the processing flow of speaker phone applications for speech and audio signal processing.

Figure 3-2. Speech Signal Processing

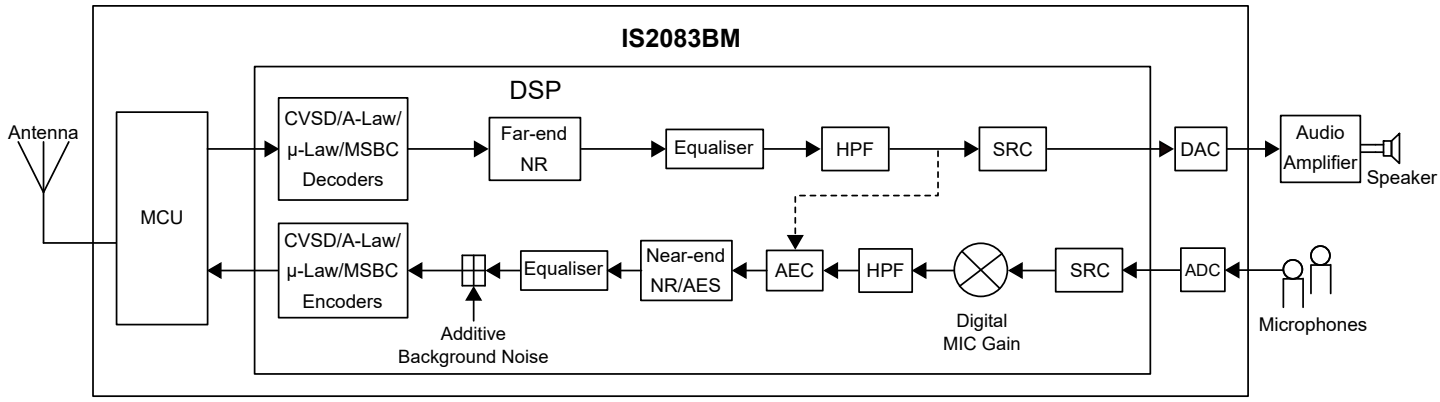
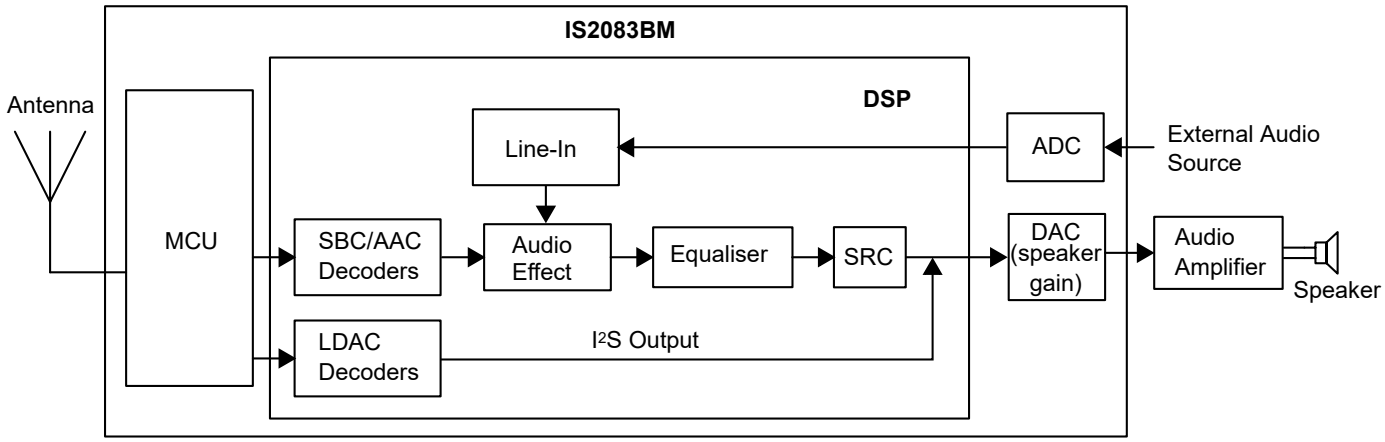


Figure 3-3. Audio Signal Processing



Note: LDAC is supported only in the IS2083BM-2L2 device.

The DSP core consists of three computational units (ALU, MAC, and Barrel Shifter), two data address generators, PMD-DMD bus exchanger, program sequencer, bi-directional serial ports (SPORT), DMA controller, interrupt controller, programmable I/O, on-chip program, and on-chip data memory.

The DSP memory subsystem defines the address ranges for the following addressable memory regions:

- Program space
  - 96 KB of Program RAM
  - 12 KB of Patch RAM
  - 64 KB of Coefficient RAM
- Data space
  - 96 KB of Data RAM
- I/O Space
  - Memory-mapped registers

The DSP core implements a modified Harvard architecture in which data memory stores data and program memory stores both instructions and data (coefficients).

3.2 Codec

The built-in codec has a high signal-to-noise ratio (SNR) performance and it consists of an Analog-to-Digital Converter (ADC), a Digital-to-Analog Converter (DAC), and an additional analog circuitry.

- Interfaces
  - Two mono differential or single-ended microphone inputs
  - One stereo single-ended line input
  - One stereo single-ended line output
  - One stereo single-ended earphone output (capacitor-less connection)
- Built-in circuit
  - Microphone bias (MICBIAS)
  - Reference and biasing circuitry
- Optional digital High Pass Filter (HPF) on ADC path
- Silence detection
  - Typically, used for Line-In inputs. For some applications, the Line-In input has high priority. After the Line-In input source is plugged in and before streaming out an audio, the Line-In noise cannot be ignored. So, the silence detection feature is used to mute this background noise.
- Anti-pop function to reduce audible glitches
  - Pop reduction system
  - Soft Mute mode
  - Typically used when the codec analog gain is changed suddenly (for example, turning OFF the power or switching the volume dial very quickly), in which case the RCL circuits in the external audio amplifier would cause "pop" noise. The anti-pop function is used to lower or increase the gain in many small steps, 1- or 2-dB change for each step, rather than a single large gain decrease or increase.
- ADC supports 8 kHz, 16 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz sampling rates.

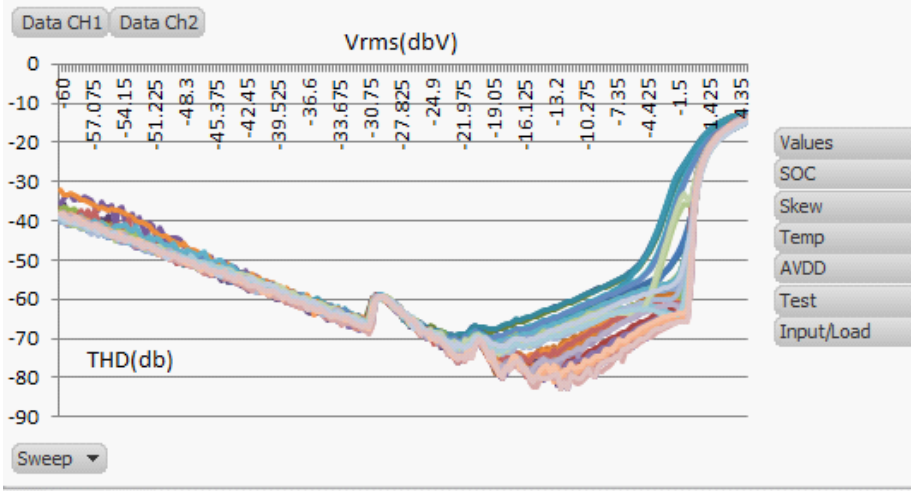
3.2.1 Audio Performance

This section provides characteristics of the internal codec in the IS2083BM device.

Table 3-1. Test Conditions

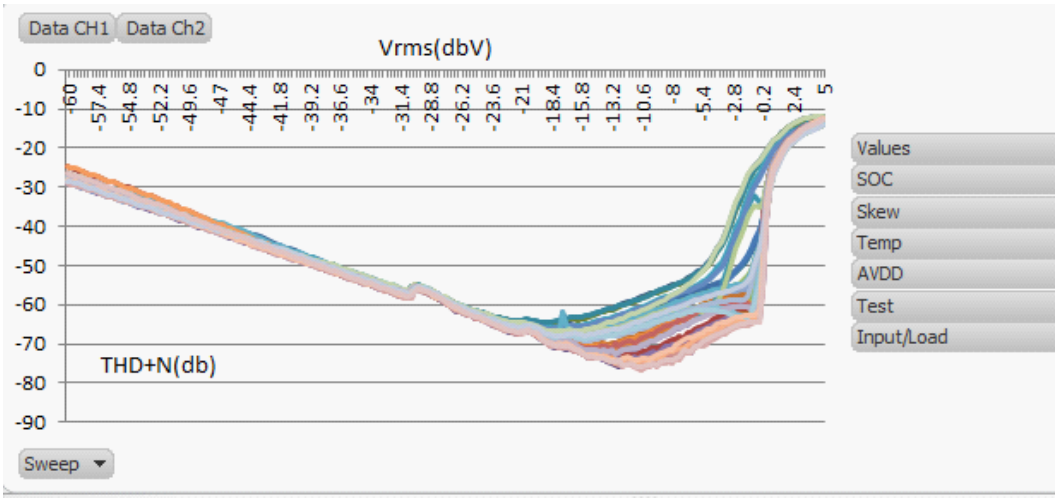
Parameter (Condition)	Value
FS	48 kHz
Analog gain setting for ADC	0 dB
Digital gain setting for ADC	0 dB
Analog gain setting for DAC	-3 dB
Digital gain setting for DAC	0 dB

Figure 3-4. ADC Signal Quality – THD



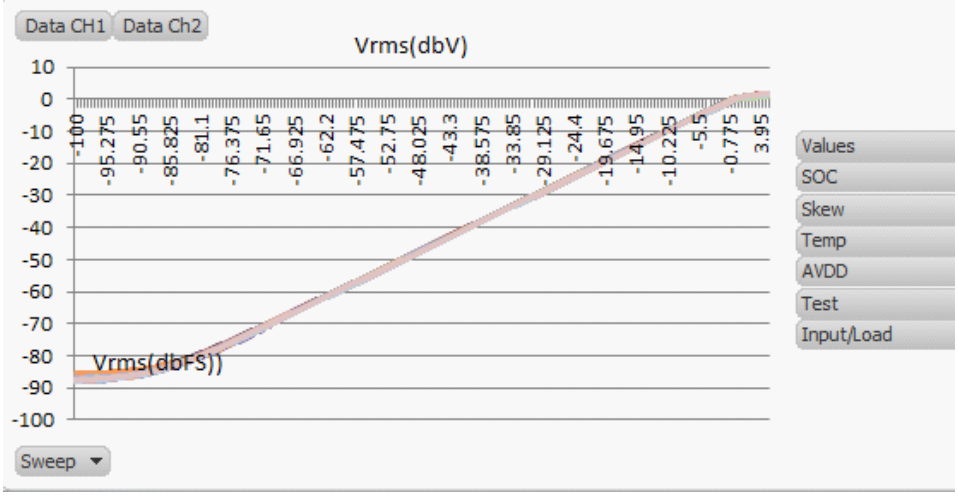
Note: Analog Gain = 0 dB, Digital Gain = 0 dB, Sweep V_{in}= -60 dbV to 5 dbV @ 1 kHz.

Figure 3-5. ADC Signal Quality – THD+N



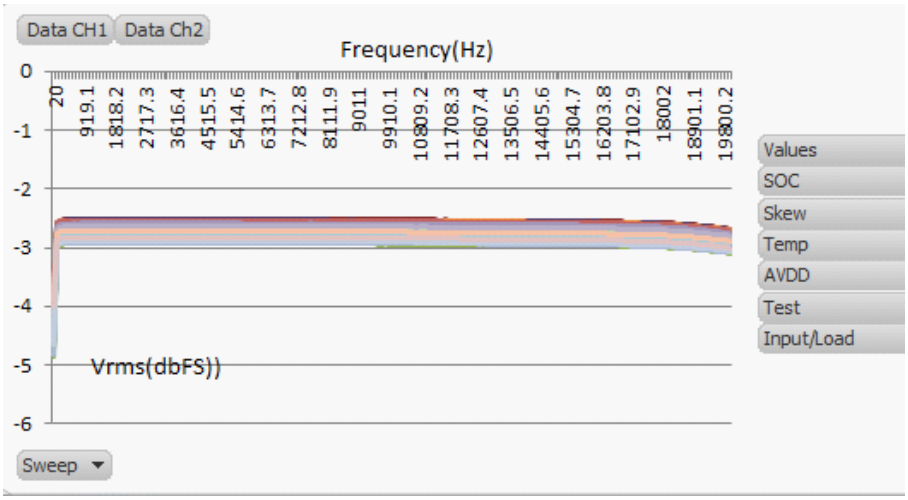
Note: Analog Gain = 0 dB, Digital Gain = 0 dB, Sweep V_{in}= -60 dbV to 5 dbV @ 1 kHz.

Figure 3-6. ADC Dynamic Range



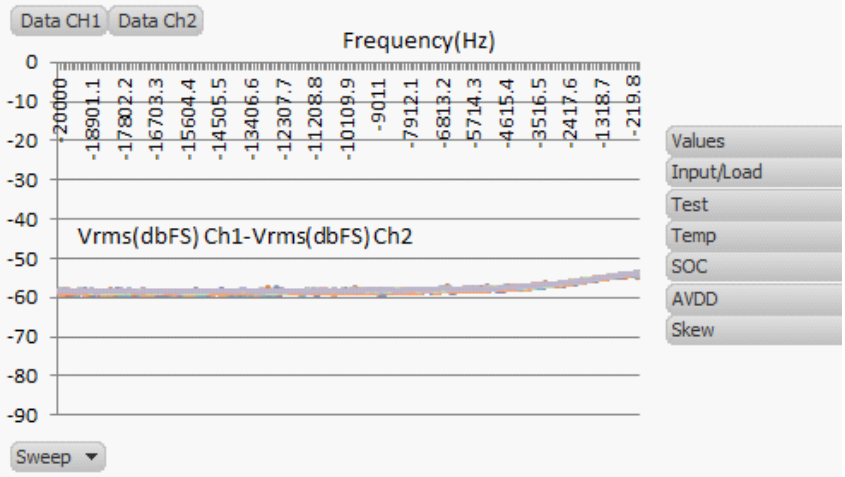
Note: Analog Gain = 0 dB, Digital Gain = 0 dB, Sweep V_{in}= -100 dbV to 5 dbV @ 1 kHz.

Figure 3-7. ADC Frequency Response



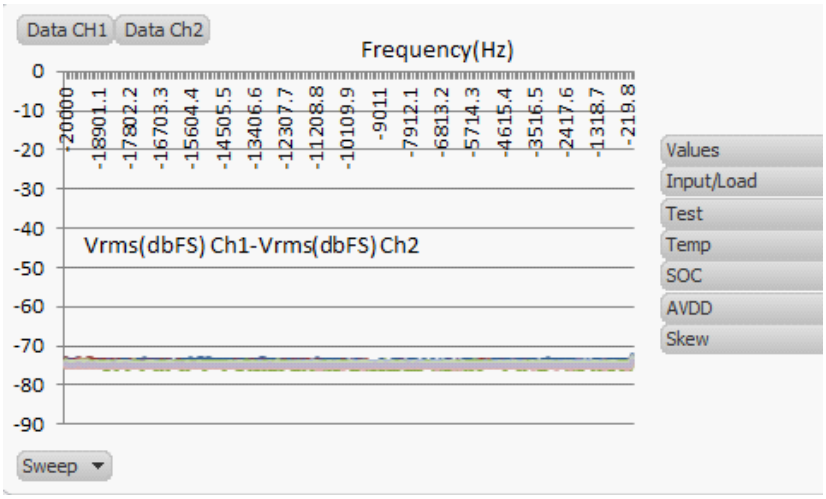
Note: Analog Gain = 0 dB, Digital Gain = 0 dB Sweep F_{in}= 20 Hz to 20 kHz @ -3 dbV.

Figure 3-8. ADC Crosstalk – Line-In



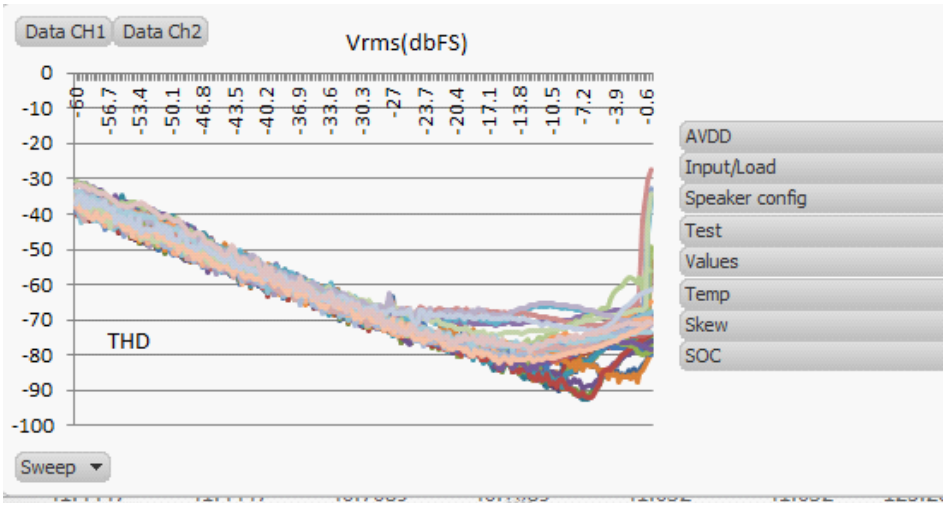
Note: Analog Gain = 0 dB, Digital Gain = 0 dB Sweep F_{in}= 20 Hz to 20 kHz @ -3 dbV.

Figure 3-9. ADC Crosstalk – Mic-in



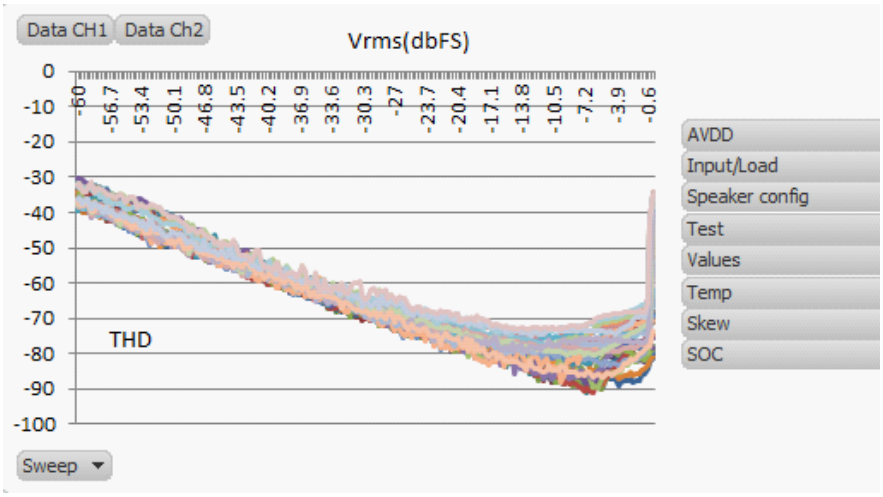
Note: Analog Gain = 0 dB, Digital Gain = 0 dB Sweep F_{in}= 20 Hz to 20 kHz @ -3 dbV.

Figure 3-10. DAC Signal Quality – THD (Single-ended)



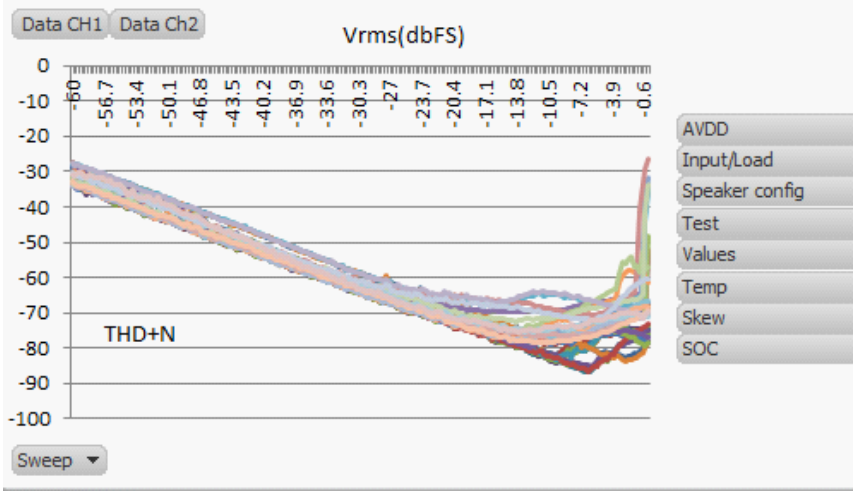
Note: Analog gain = -3 dB, digital gain = 0 dB, sweep V_{in} = -60 dBFS to 0 dBFS @ 1 kHz.

Figure 3-11. DAC Signal Quality – THD (Capless)



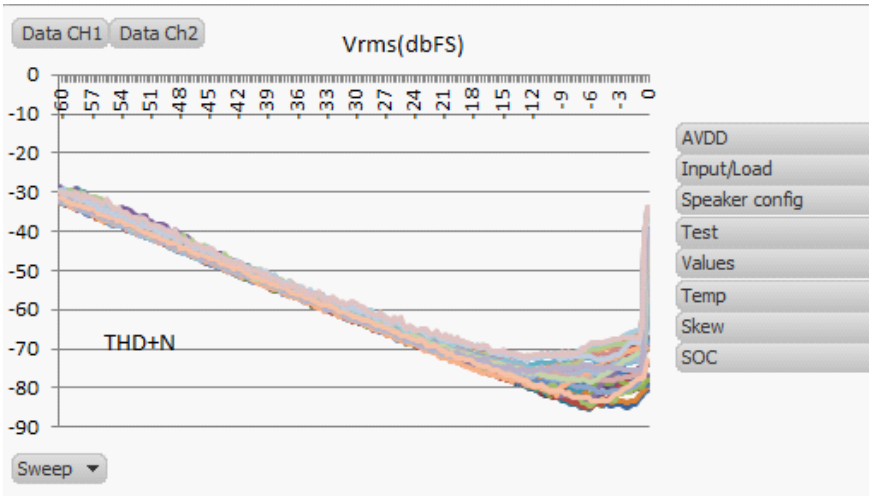
Note: Analog gain = -3 dB, digital gain = 0 dB, sweep V_{in} = -60 dBFS to 0 dBFS @ 1 kHz.

Figure 3-12. DAC Signal Quality − THD+N (Single-ended)



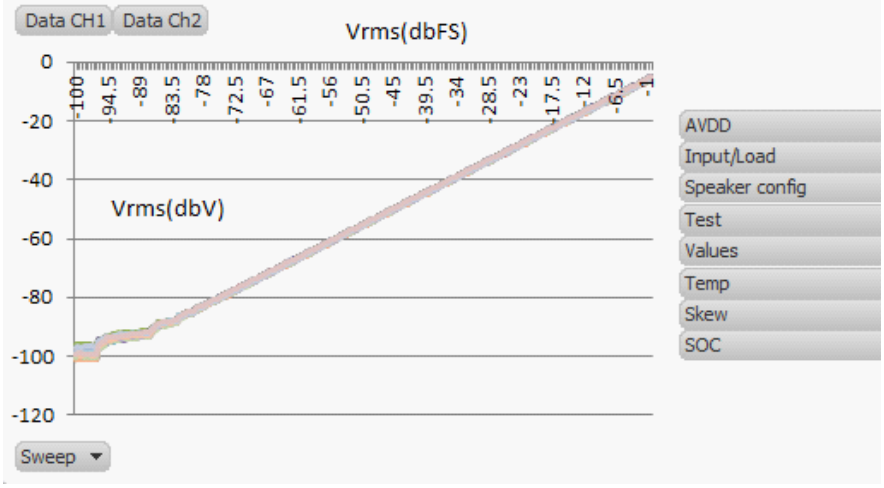
Note: Analog gain = -3 dB, digital gain = 0 dB, sweep V_{in} = -60 dBFS to 0 dbFS @ 1 kHz.

Figure 3-13. DAC Signal Quality − THD+N (Capless)



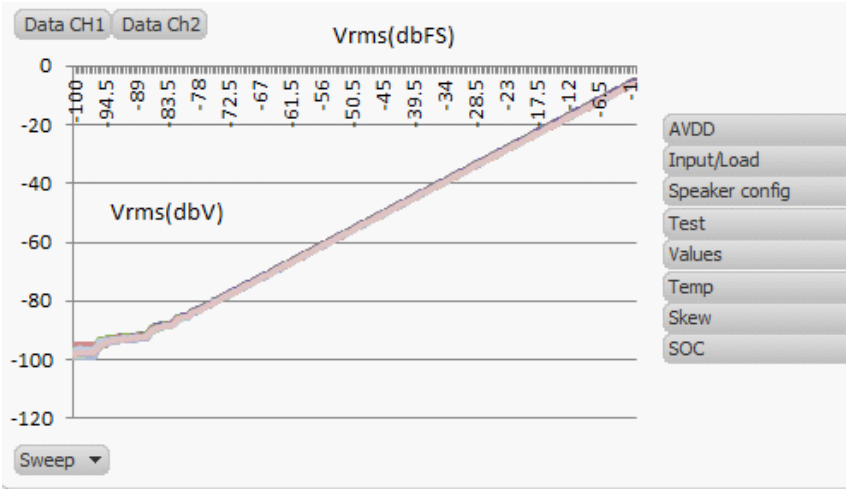
Note: Analog gain = -3 dB, digital gain = 0 dB, sweep V_{in} = -60 dBFS to 0 dBFS @ 1 kHz.

Figure 3-14. DAC Dynamic Range (Single-ended)



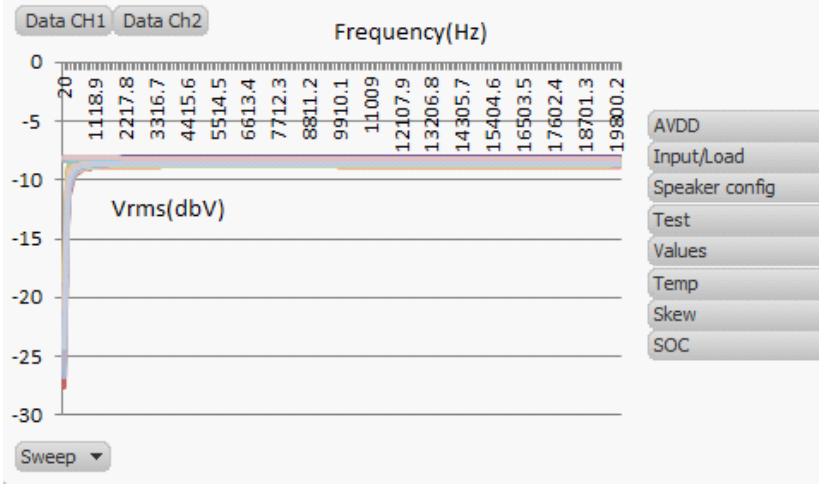
Note: Analog gain = 3 dB, digital gain = 0 dB, sweep V_{in} = -100 dBFS to 0 dBFS @ 1 kHz.

Figure 3-15. DAC Dynamic Range (Capless)



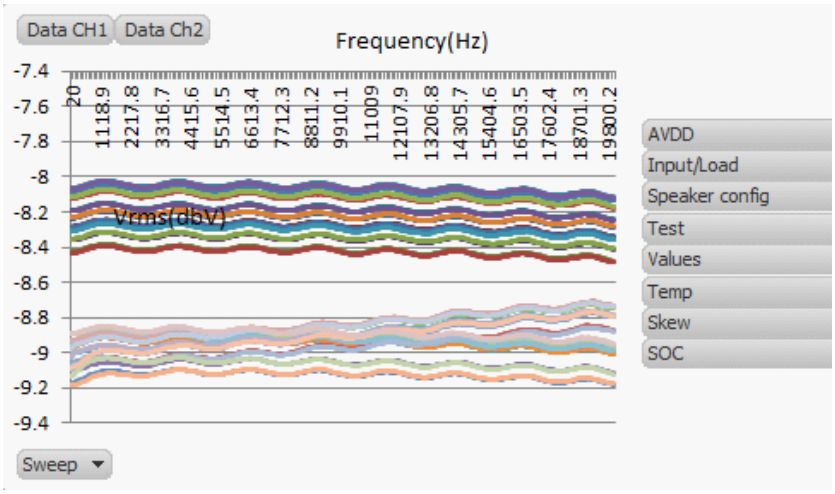
Note: Analog gain = 3 dB, digital gain = 0 dB, sweep V_{in} = -100 dBFS to 0 dBFS @ 1 kHz.

Figure 3-16. DAC Frequency Response (Single-ended)



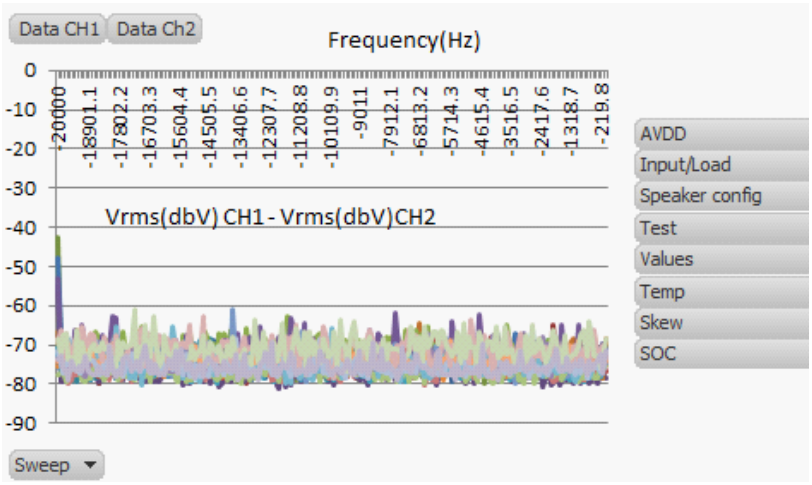
Note: Analog gain = -3 dB, sweep f_{in} = 20 Hz to 20 kHz @ -3 dBFS.

Figure 3-17. DAC Frequency Response (Capless)



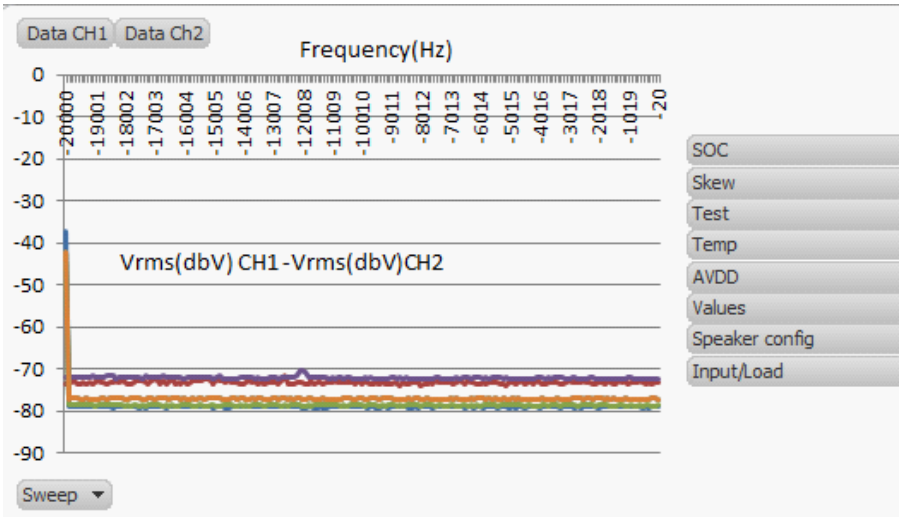
Note: Analog gain = -3 dB, sweep f_{in} = 20 Hz to 20 kHz @ -3 dBFS.

Figure 3-18. DAC Crosstalk (Single-ended)



Note: Analog gain = -3 dB, sweep f_{in} = 20 Hz to 20 kHz @ -3 dBFS.

Figure 3-19. DAC Crosstalk (Capless)



Note: Analog gain = -3 dB, sweep f_{in} = 20 Hz to 20 kHz @ -3 dBFS.

3.3 Auxiliary Port

The IS2083BM SoC supports one analog (Line-In, also called as Aux-In) signal from the external audio source. The analog (Line-In) signal can be processed by the DSP to generate different sound effects (multiband dynamic range compression and audio widening), which can be configured by using the Config Tool.

3.4 Microphone Inputs

The IS2083BM SoC supports:

- One digital microphone with one (mono) or two channels (stereo L and R)
- Two analog microphones (left and right)

Note: Do not use analog and digital microphones simultaneously.

The DIGMIC interfaces should only be used for PDM digital microphones (typically, MEMS microphones) up to 4 MHz of clock frequency. I^2S-based digital microphones should use the external I^2S port.

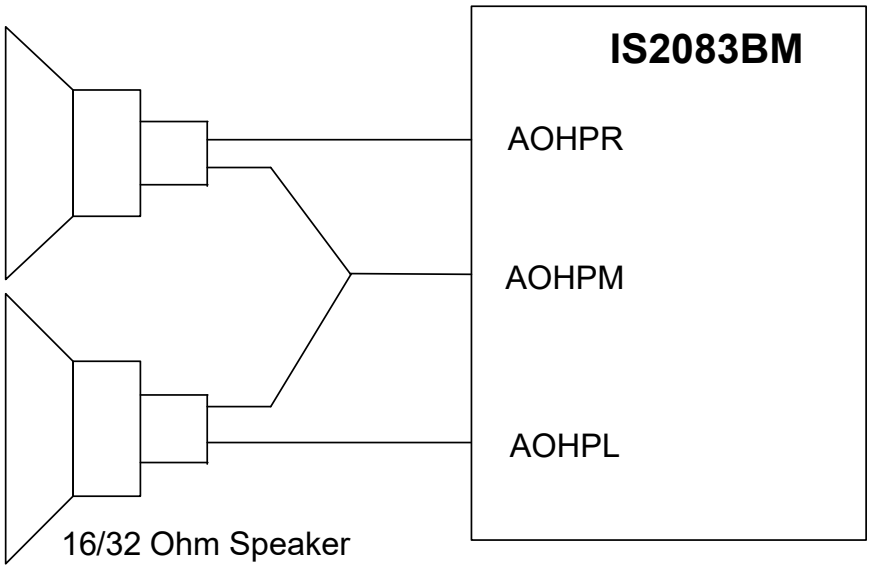
Note: To avoid saturation in the PDM Digital Microphone path, Microchip recommends to limit the PDM maximum input level to -6 dBFS.

3.5 Analog Speaker Output

The IS2083BM SoC supports the following speaker output modes:

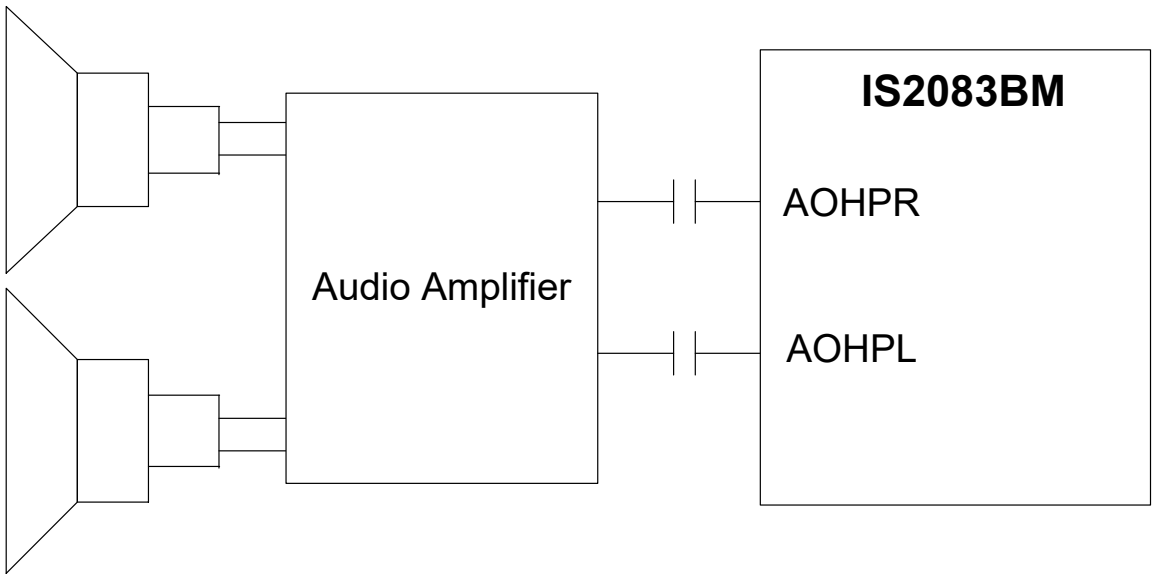
- Capless mode − Used for headphone applications in which capacitor less (capless) output connection helps to save the Bill of Material (BoM) cost by avoiding a large DC blocking capacitor. The following figure illustrates the Capless mode analog speaker output.

Figure 3-20. Capless Mode Analog Speaker Output



- Single-Ended mode − Used for driving an external audio amplifier where a DC blocking capacitor is required. The following figure illustrates the Single-Ended mode analog speaker output.

Figure 3-21. Single-ended Mode Analog Speaker Output



4. Bluetooth Transceiver

The IS2083BM SoC is designed and optimized for Bluetooth 2.4 GHz systems. It contains a complete radio frequency transmitter (TX)/receiver (RX) section. An internal synthesizer generates a stable clock for synchronizing with another device.

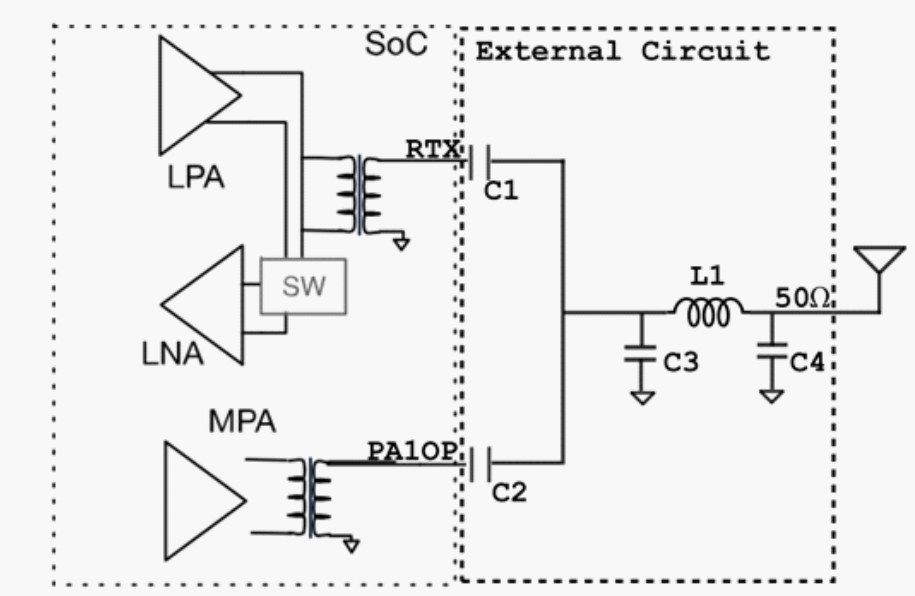
4.1 Transmitter

The IS2083BM has Lower Power Amplifier (LPA) and Medium Power Amplifier (MPA). The MPA supports up to +11 dBm power level for Bluetooth Class1 configuration and LPA supports up to about +1 dBm power level for Bluetooth Class2 configuration. The MPA output is connected to the PA1OP pin of the SoC. The LPA output and LNA input are multiplexed and connected to the RTX pin of the device.

The IS2083BM supports shared port configuration, in which the MPA and LPA pins are wired together as shown in the following figure. In shared port configuration, the external series capacitors on RTX, PA1OP pins and PI filter circuit implements a low BoM cost solution to combine the MPA and LPA/LNA signals. Typical value of these components are C1 = 2 pF, C2 = 3 pF, C3 = 1.3 pF/1.4 pF, L1 = 2.7 nH/2.8 nH, C4 = 3 pF (use the BM83 RF schematics as it is to achieve the desired RF performance).

Note: For more details, refer to the *IS2083 Reference Design Application Note*.

Figure 4-1. Shared Port Configuration



4.2 Receiver

The Low-Noise Amplifier (LNA) operates in a TR-combined mode for a single port application. It saves a pin on the package without having an external TX/RX switch.

The ADC is used to sample the analog input signal and convert it into a digital signal for demodulator analysis. A channel filter is integrated into the receiver channel before the ADC to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject the image frequency for the low-IF architecture, and it also intended to reduce the external Band Pass Filter (BPF) component for a super heterodyne architecture.

The Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

4.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. There is a Voltage Controlled Oscillator (VCO) inside with a tunable internal LC tank that can reduce components variation. A crystal oscillator with an internal digital trimming circuit provides a stable clock for the synthesizer.

4.4 Modulator-Demodulator

For Bluetooth 1.2 specification and below, 1 Mbps is the standard data rate based on the Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modulator-demodulator (Modem) meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with Enhanced Data Rate (EDR) specifications.

For Bluetooth 2.0 and above specifications, EDR is introduced to provide the data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of the EDR packet represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8 DPSK.

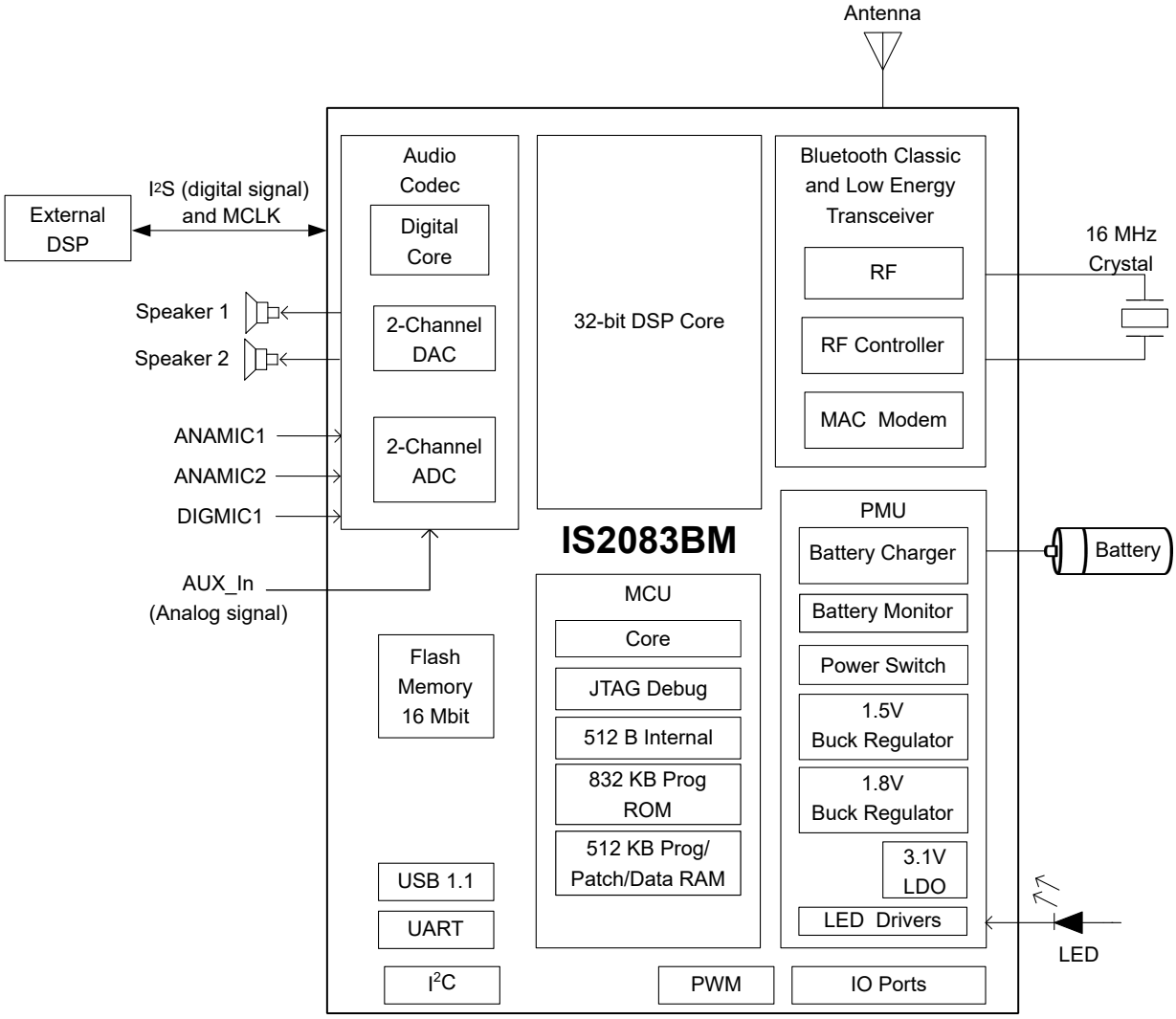
4.5 Adaptive Frequency Hopping

The IS2083BM SoC has an Adaptive Frequency Hopping (AFH) function to avoid RF interference. It has an algorithm to check the nearby interference and to choose a clear channel for transceiver Bluetooth signal.

5. Microcontroller

A 8051 microcontroller is built into the SoC to execute the Bluetooth protocols. It operates from 16 MHz to higher frequencies where the firmware can dynamically adjust the trade-off between the computing power and the power consumption.

Figure 5-1. IS2083BM SoC Block Diagram



The MCU core contains Bluetooth stack and profiles, which are hard-coded into ROM to minimize power consumption for the firmware execution and to save the external Flash cost. This core is responsible for the following system functions:

- Boot-up
- On-the-Air Device Firmware Upgrade (OTA DFU)
- Executing the Bluetooth stack and Bluetooth profiles
- Sending the packets to DSP core for audio processing
- Loading audio codec registers with values read the Flash
- Managing low-power modes
- Executing UART commands

- Device programming
- GPIO button control
- PWM control
- LED control
- Bluetooth role swap for multi-speakers
- Adjusting the Bluetooth clock
- External audio codec control/configuration, if needed
- USB battery charge detection and configuration of the PMU battery charger
- Configuration of PMU power regulation
- Changing the audio subsystem clocks On-the-Fly (OTF) for different audio sampling rates

5.1 Memory

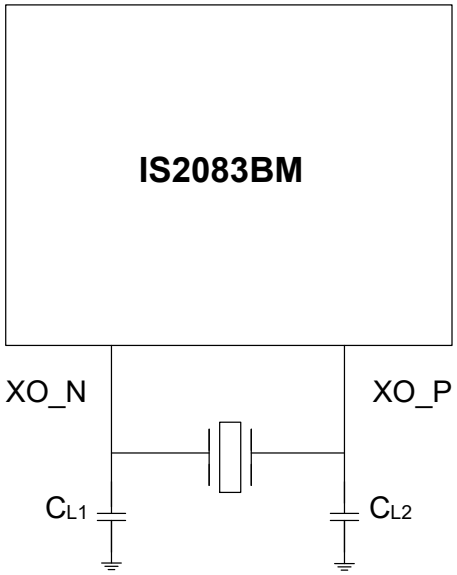
A synchronous single port RAM interface is used to fulfill the ROM and RAM requirements of the processor. The register bank, dedicated single port memory and Flash memory are connected to the processor bus. The processor coordinates with all link control procedures and the data movement happens using a set of pointer registers.

5.2 Clock

The IS2083BM SoC is composed of an integrated crystal oscillator that uses a 16 MHz ±10 ppm external crystal and two specified loading capacitors to provide a high-quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors, which are associated with the crystal and its equivalent loading capacitance in the mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors (C_{trim}).

The crystal trimming can be done using manufacturing tools provided by Microchip. The following figure illustrates the crystal oscillator connection of the IS2083BM SoC with two capacitors.

Figure 5-2. Crystal Oscillator in the IS2083BM



The clock module controls switching and synchronization of clock sources. Clock sources include:

- System Phase-locked Loop (PLL)
- Primary oscillator
- External clock oscillator
- Ultra Low-power internal RC oscillator (UPLC) with nominal frequency as 32 kHz.

The clock module provides gated clock output for 8051 and its peripheral modules, gated clock output for Bluetooth modules as well as DSP audio subsystem. The system enters low power mode by switching OFF clocks driven from the PLL and external oscillator. Only ULPC is operated to maintain Bluetooth timing.

6. Power Management Unit

The IS2083BM SoC has an integrated Power Management Unit (PMU). The PMU includes buck switching regulator, LDO, battery charger, SAR ADC for voltage sensing, and LED drivers. The power switch is provided to switch between battery and adapter. It also provides current to the LED drivers.

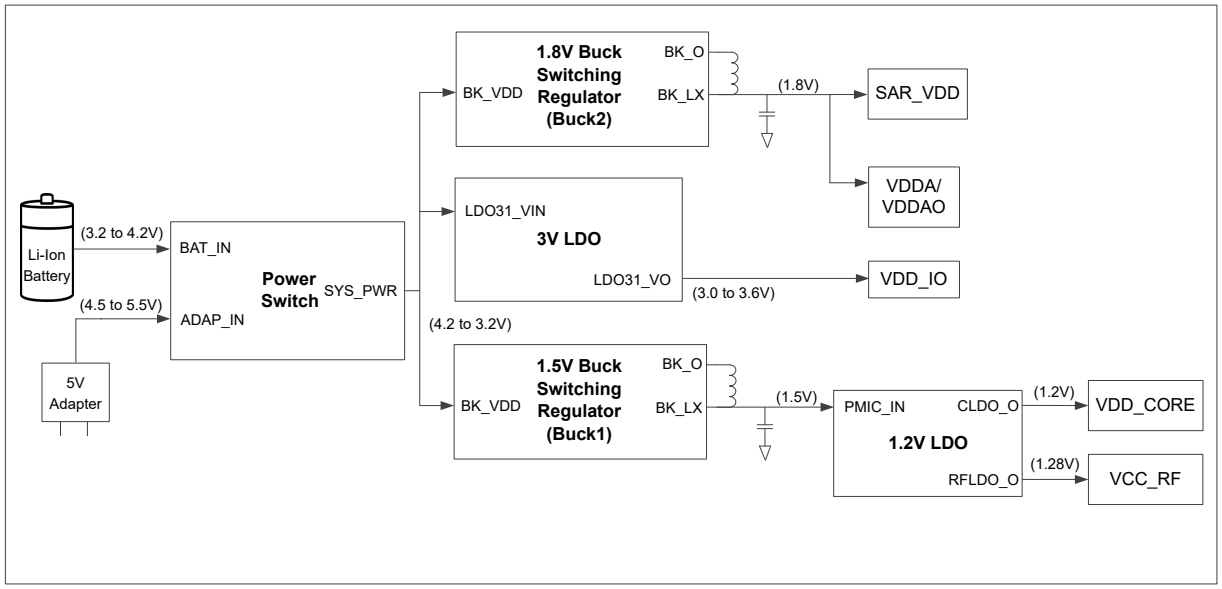
6.1 Device Operation

The IS2083BM SoC is powered through the BAT_IN input pin. The external 5V power adapter can be connected to the ADAP_IN pin to charge the battery.

For normal operation, it is recommend to use the BAT_IN pin to power the IS2083BM SoC and ADAP_IN only for charging the battery. The following figure illustrates the connection from the BAT_IN pin to other voltage supply pins of the IS2083BM. The IS2083BM has two buck switching regulators:

- Buck1 DC/DC regulator provides 1.5V and is used to supply power to RF and baseband.
- Buck2 DC/DC regulator provides 1.8V and is used to supply power to I/O pads and internal codec.

Figure 6-1. Power Tree Diagram



6.2 Power Supply

Typically, the PWR (MFB) pin is connected to a mechanical button on the device. When pressed, it connects the BAT_IN pin to the power detection block of the PMU. The PMU keeps the V_{BAT_IN} connected once the PWR pin is released.

6.3 Adapter Input

The adapter input (ADAP_IN) is used for charging the battery. If the total power consumed by IS2083BM SoC is less than 120 mA, ADAP_IN pin can also be used as power supply input. If the current to be driven is more than 120 mA, it is recommended to use the BAT_IN pin as the power supply input and the ADAP_IN pin can be left floating.

6.4 Buck1 (BK1) Switching Regulator

The IS2083BM includes a built-in programmable output voltage regulator which converts the battery voltage to 1.5V to supply the RF and baseband power supply. This converter has high conversion efficiency and fast transient response.

Note: Do not connect any other devices to buck1 regulator output pin (BK1_VOUT).

6.5 Buck2 (BK2) Switching Regulator

The IS2083BM includes a second build in programmable output voltage regulator which converts the battery voltage to 1.8V, to supply the PMU ADC and to optionally supply stereo audio codec and/or I/O's. This converter has a high conversion efficiency and a fast-transient response.

Note: Do not connect any other devices to buck2 regulator output pin (BK2_VOUT).

6.6 Low-Dropout Regulator

The built-in Low-Dropout (LDO) regulator is used to convert the battery or adapter power to 3.3V to supply the USB transceiver and to supply the I/O's.

6.7 Battery Charging

The IS2083BM SoC has a built-in battery charger that is optimized for lithium-ion and lithium polymer batteries.

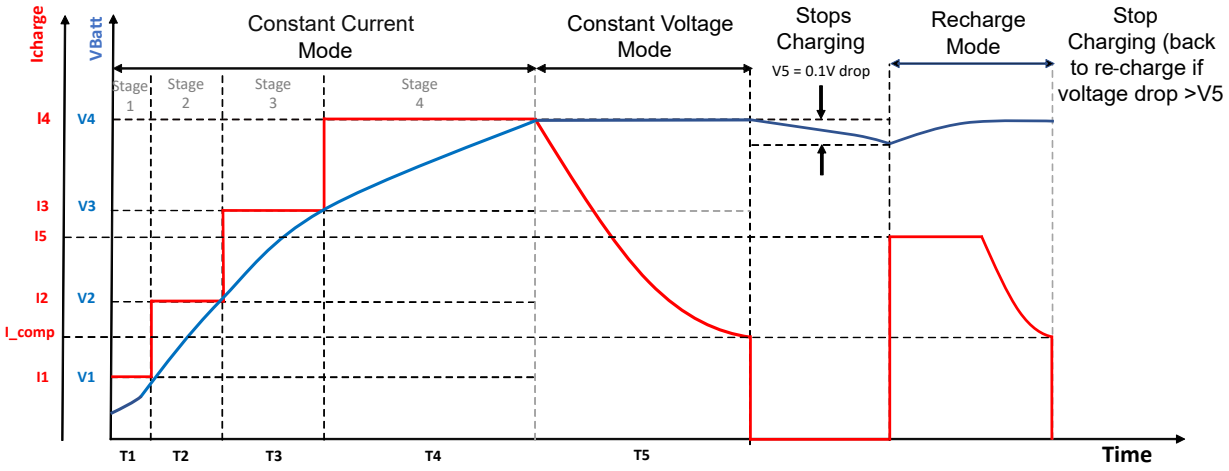
The on-chip PMU integrates the battery charger and voltage regulator. A power switch is used to switch over the power source between the battery (BAT_IN) and an adapter (ADAP_IN). The PMU provides the current to drive two LEDs.

The battery charger supports various modes with the features listed below:

- Charging control using current sensor
- User-programmable current regulation
- High accuracy voltage regulation
- Constant current and constant voltage modes
- Stop charging and re-charging modes

The following figure illustrates the charging curve of a battery.

Figure 6-2. Battery Charging Curve



Note: For more details on battery charger configuration, please refer to the *IS2083/BM83 Battery Charger Application Note (AN3490)*.

6.7.1 Battery Charger Detection

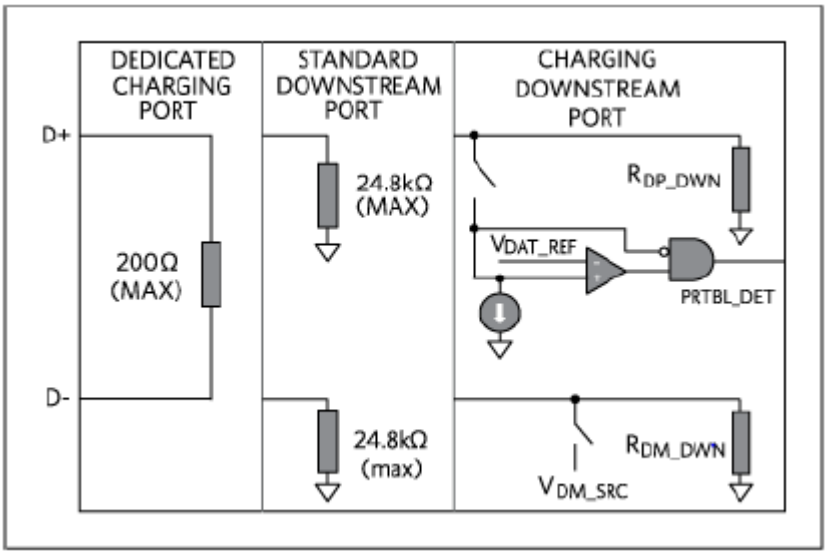
The IS2083BM USB transceiver includes built-in battery charger detection that is compatible with the following:

USB BC 1.2 Standard Downstream Port (SDP): This is the same port defined by the USB 2.0 spec and is the typical form found in desktop and laptop computers. The maximum load current is 2.5 mA when suspended, 100mA when connected and not suspended, and 500 mA (max) when connected and configured for higher power.

USB BC 1.2 Dedicated Charger Port (DCP): BC 1.2 describes power sources like wall warts and auto adapters that do not enumerate so that charging can occur with no digital communication at all. DCPs can supply up to 1.5A and are identified by a short between D+ to D-. This port does not support any data transfer, but is capable of supplying charge current beyond 1.5A.

Any device (such as the IS2083BM) that connects to any USB receptacle and uses that power to run itself or charge a battery, must know how much current is appropriate to draw. Attempting to draw 1A from a source capable of supplying only 500mA would not be good. An overloaded USB port will likely shut down or blow a fuse. Even with resettable protection, it will often not restart until the device is unplugged and reconnected. In ports with less rigorous protection, an overloaded port can cause the entire system to Reset. Once the USB transceiver determines the battery charger profile and port type (SDP, CDP, DCP), it interrupts the CPU, which then reads the battery charger profile and port type information out of the USB registers. It uses this information to program the PMU (via the 3-wire PMU interface) with the configuration corresponding to the battery charger profile and port type.

Figure 6-3. USB Battery Charger 1.2 DCP/SDP/CDP Signaling

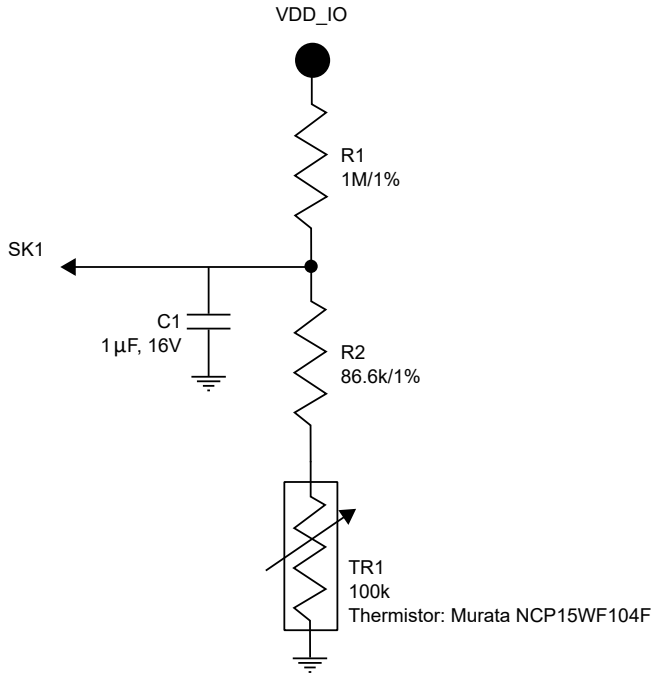


6.8 SAR ADC

The IS2083BM SoC has a 10-bit Successive Approximation Register (SAR) ADC with ENOB (Effective Number of Bits) of 8-bits; used for battery voltage detection, adapter voltage detection, charger thermal protection, and ambient temperature detection. The input power of the SAR ADC is supplied by the 1.8V output of Buck2. The warning level can be programmed by using the Config Tool or the SDK.

The SK1 and SK2 are the ADC channel pins. The SK1 is used for charger thermal protection. The following figure illustrates the suggested circuit and thermistor, Murata NCP15WF104F. The charger thermal protection can avoid battery charge in a restricted temperature range. The upper and lower limits for temperature values can be configured by using the Config Tool.

Figure 6-4. Ambient Detection Circuit



Note: The thermistor must be placed close to the battery in the user application for accurate temperature measurements and to enable the thermal shutdown feature.

The following figures show SK1 and SK2 channel behavior.

Figure 6-5. SK1 Channel

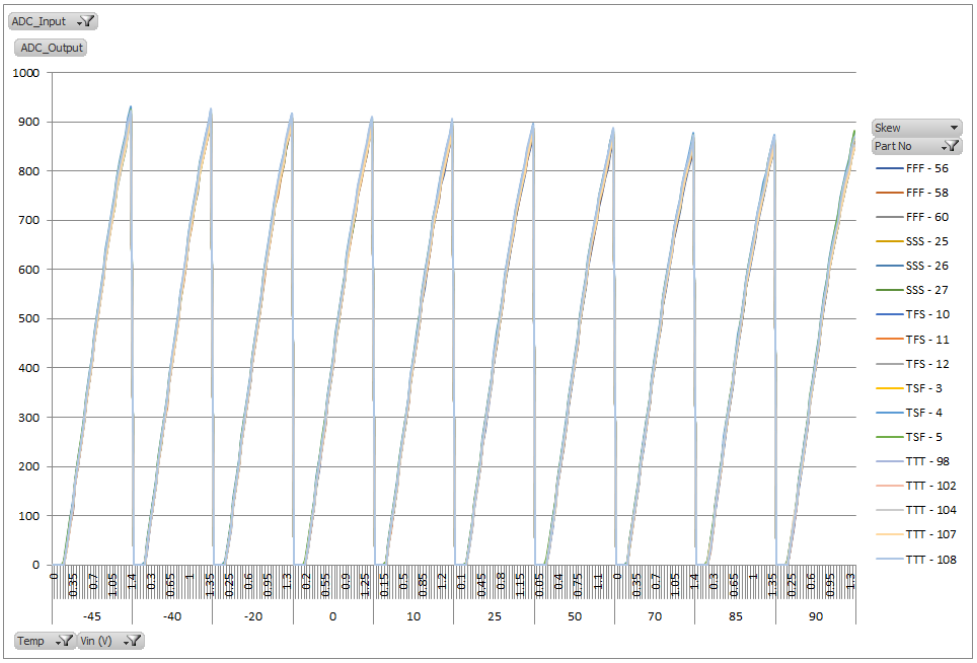
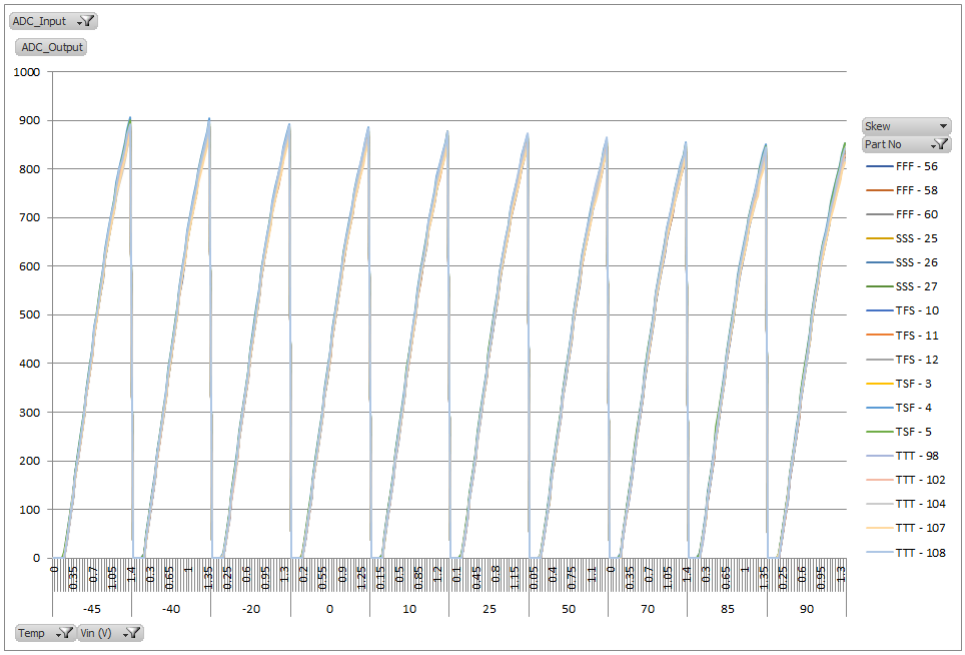


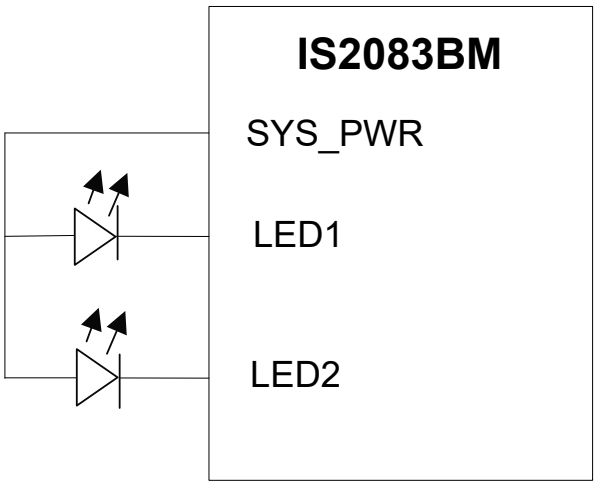
Figure 6-6. SK2 Channel



6.9 LED Driver

The IS2083BM has two LED drivers to control external LEDs. The LED drivers provide enough sink current (16-step control and 0.35 mA for each step) and the LED can be connected directly to the IS2083BM. The LED settings can be configured by using the Config Tool. The following figure illustrates the LED drivers in the IS2083BM.

Figure 6-7. LED Driver

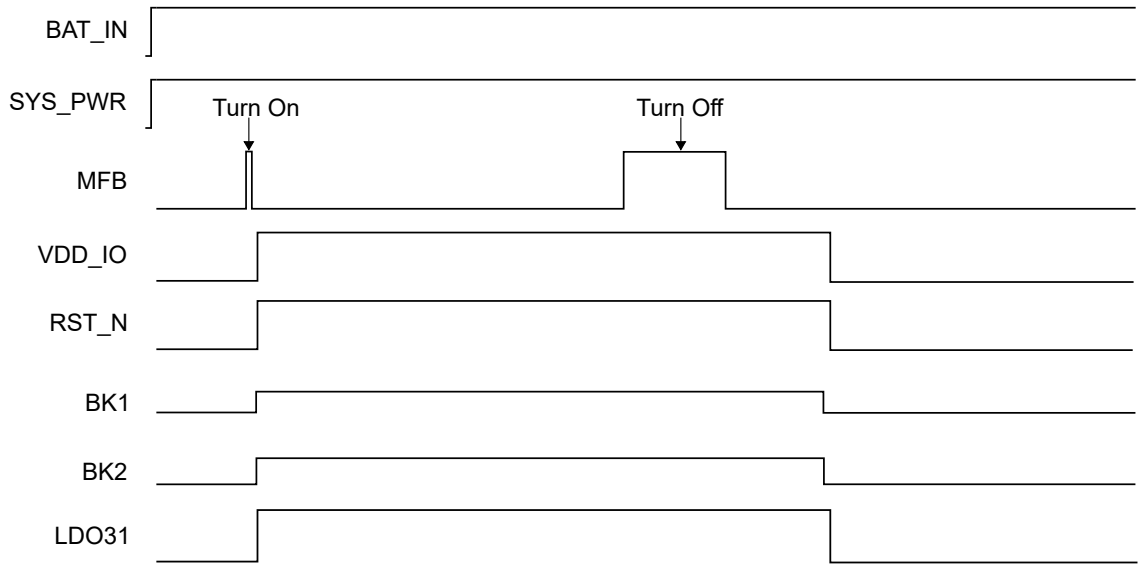


7. Application Information

7.1 Power On/Off Sequence

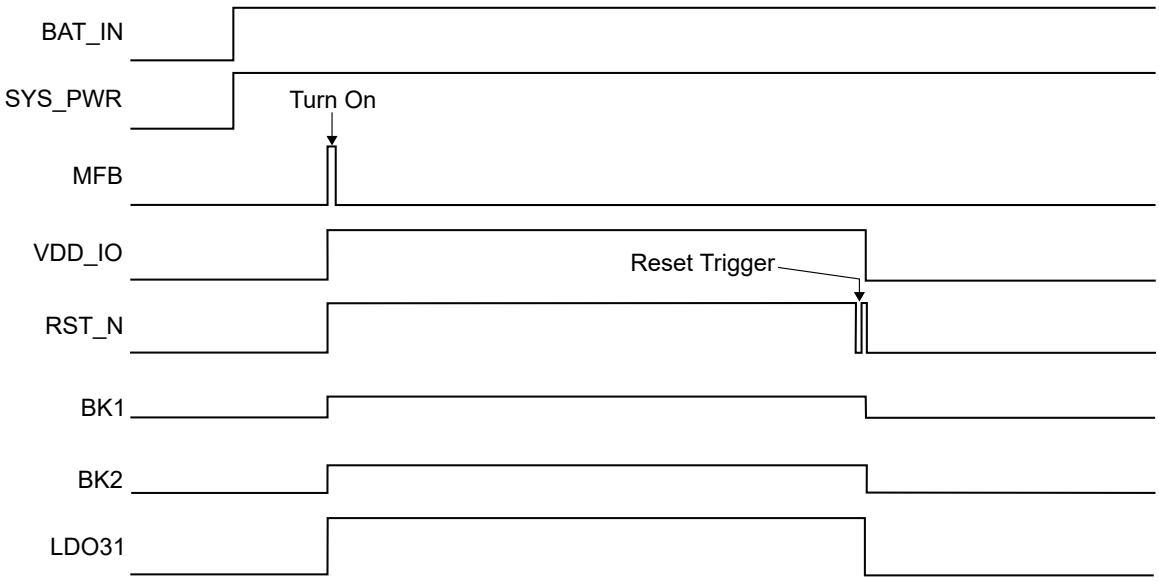
In Embedded mode, the BM83 module utilizes the MFB button to turn on and turn off the system. For Host mode, refer to 7.6 Host MCU Interface. The following figure illustrates the system behavior (Embedded mode) upon a MFB press event to turn on and turn off the system.

Figure 7-1. Timing Sequence of Power On/Off in Embedded Mode



The following figure illustrates the system behavior (Embedded mode) upon a MFB press event to turn on the system and then trigger a Reset event.

Figure 7-2. Timing Sequence of Power On and Reset Trigger in Embedded Mode

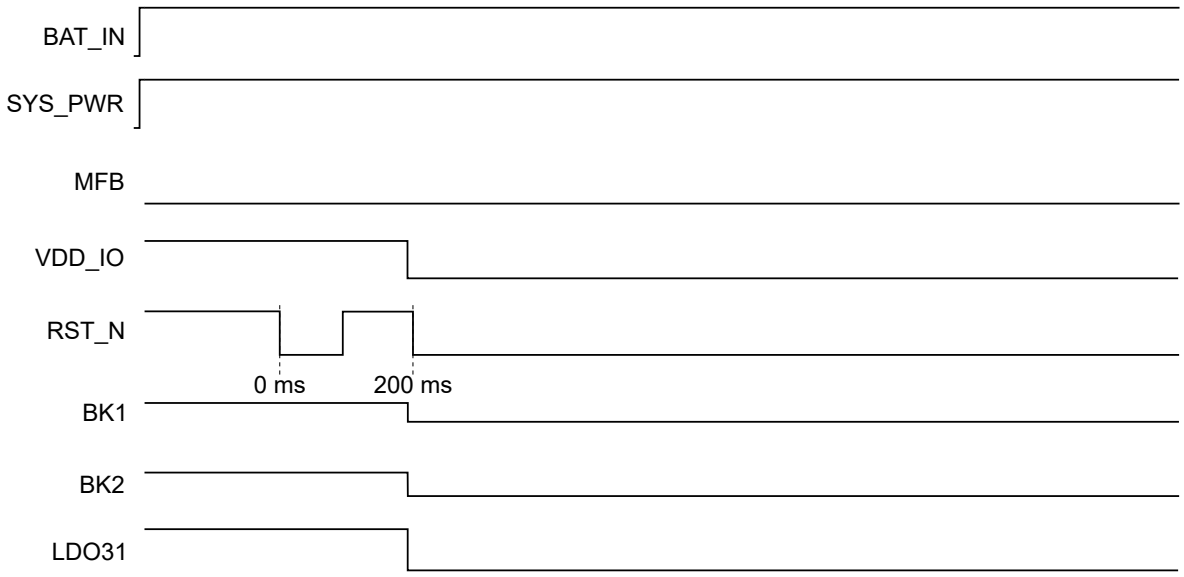


7.2 Reset

The Reset logic generates proper sequence to the device during Reset events. The Reset sources include external Reset, power-up Reset, and Watchdog Timer (WDT). The IS2083 SoC provides a WDT to Reset the chip. In addition, it has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power On state. This action can also be driven by an external Reset signal, which is used to control the device externally by forcing it into a POR state. The following figure illustrates the system behavior upon a RST_N event.

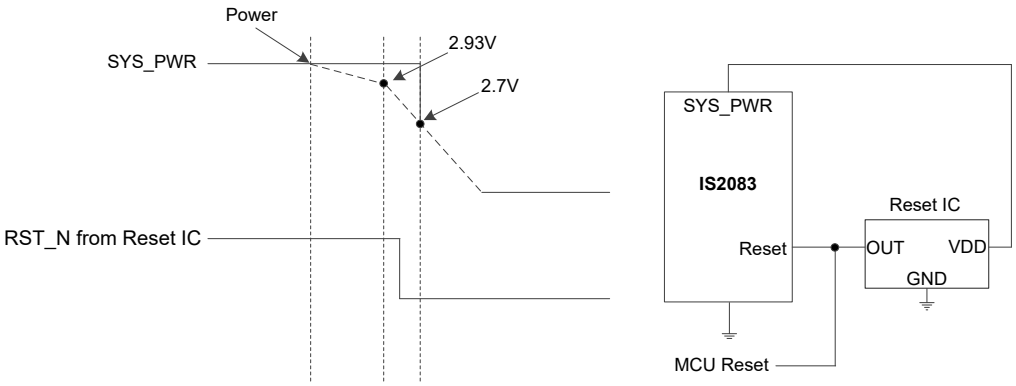
Note: The Reset (RST_N) is an active-low signal and can be utilized based on the application needs, otherwise, it can be left floating.

Figure 7-3. Timing Sequence of Reset Trigger



Note: RST_N pin has an internal pull-up, thus, RST_N signal will transition to high again upon releasing the RST_N button. This is an expected behavior of RST_N signal.

Figure 7-4. Timing Sequence of Power Drop Protection



Timing sequence of power drop protection:

- It is recommended to use the battery to provide the power supply at BAT_IN.
- If an external power source or a power adapter is utilized to provide power to BAT_IN, it is recommended to use a voltage supervisor Integrated Circuit (IC).
- The Reset IC output pin, RST_N, must be open drain type and threshold voltage as 2.93V.
- The RST_N signal must be fully pulled low before SYS_PWR power drop to 2.7V.

7.3 Programming and Debugging

The IS2083BM devices contain 2 MB of Flash memory, which is interfaced using the Serial Quad Interface (SQI). The following sections describe the Test mode programming and two-wire ICSP debug interface for the SDK user.

7.3.1 Test Mode Programming

The Test mode allows an external UART host to communicate with the device using Bluetooth vendor commands over the UART interface. Also, the host can interface with the device driver firmware to perform firmware programming using the isUpdate tool. The Test mode also supports TX/RX operations and collects/reports Bit Error Rate (BER) and other RF performance parameters. These values can, then, be used to accept/reject the device and/or calibrate the module.

Enter the Test mode by pulling the PORT3_4 pin to low during start-up/Reset when powered by ADAP_IN 5V supply. The pin PORT3_4 can be used as a GPIO pin if the pin level is high during start-up/Reset. The boot code residing in the boot ROM is responsible for identifying this event, setting the CFGMODE [TEST_MODE] bit and, then, performing a Reset of the device using the RST_N pin.

The following table provides the configurations required to set the Test mode or Application mode.

Table 7-1. Test Mode Configuration Settings

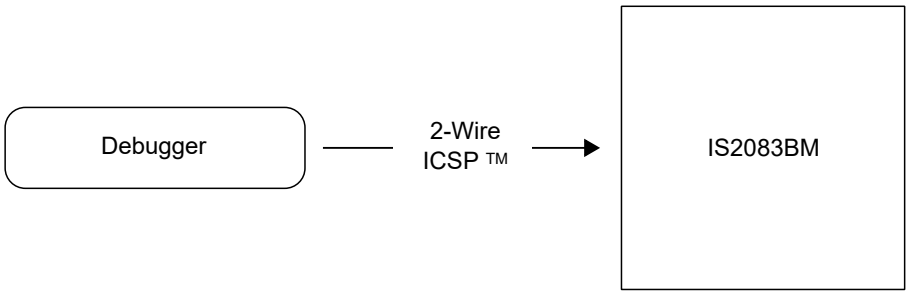
Pins	Status	Mode
P3_4	Low	Test mode
	Floating	Application mode

To exit from the Test mode (regardless of how it is entered), the firmware can clear the Test mode bit and perform a device Reset, either by asserting RST_N pin or by a Software Reset.

7.3.2 Two-Wire JTAG Debug Interface

The IS2083BM devices provide a two-wire JTAG interface for SDK debugging (see the following figure). The target device must be powered, and all required signals must be connected. In addition, the interface must be enabled through a special initialization sequence (see 7.3.3 Enabling Debugging Interface).

Figure 7-5. Two-Wire ICSP Interface



The two-wire ICSP port is used as an interface to connect a Debugger in the IS2083BM device. The following table provides the required pin connections. This interface uses the following two communication lines to transfer data to and from the IS2083BM device being programmed:

- Serial Program Clock (TCK_CPU)
- Serial Program Data (TDI_CPU)

These signals are described in the following two sections. Refer to the specific device data sheet for the connection of the signals to the chip pins. The following table describes the two-wire interface pins.

Table 7-2. Two-Wire Interface Pin Description

Pin Name	Pin Type	Description
RST_N	I	Reset pin
VDD_IO, ADAP_IN, BAT_IN	P	Power supply pins
GND	P	Ground pin
TCK_CPU	I	Serial Clock
TDI_CPU	I/O	Serial Data

Note: For more details, refer to the *IS2083 SDK Debugger User's Guide* available in the SDK package.

7.3.2.1 Serial Program Clock

The Serial Program Clock (TCK_CPU) is the clock that controls the updating of the TAP controller and the shifting of data through the Instruction or selected data registers. TCK_CPU is independent of the processor clock with respect to both frequency and phase.

7.3.2.2 Serial Program Data

Serial Program Data (TDI_CPU) is the data input/output to the instruction or selected data registers. In addition, it is the control signal for the TAP controller. This signal is sampled on the falling edge of TDI_CPU for some TAP controller states.

7.3.3 Enabling Debugging Interface

On the IS2083BM, debugging interfaces are enabled using the standard Microchip test patterns. Once RST_N is asserted (low), the user may provide an entry sequence on any TSTC2ENTRY and TSTD2ENTRY pin pair on the device. Once RST_N is de-asserted (high), the corresponding debugging interface is enabled as per the entry sequence.

The TSTC2ENTRY/TSTD2ENTRY pin pairs are mapped on top of the CPU JTAG interface so that two-wire debug interface may be enabled by controlling only 3 device pins (RST_N and 2 entry pins).

The Debugging mode entry sequence for the Two-Wire mode is shown in the following table, and the timing diagram is shown in the following figure.

Table 7-3. CPU Debugging Mode Entry

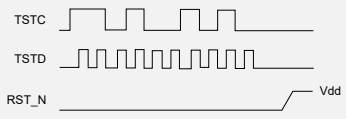
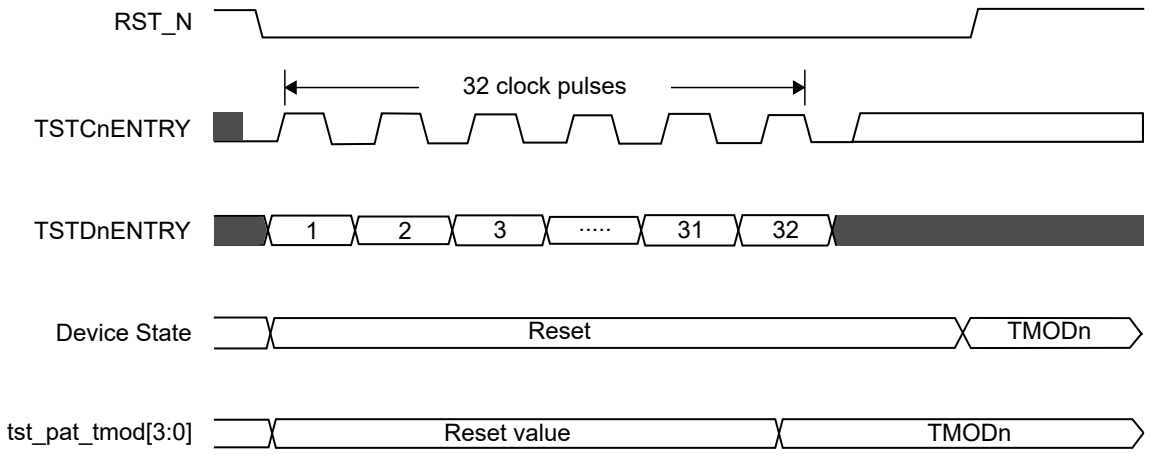
Debug Mode Entry Sequence		Mode
	4D43 4851 “MCHQ”	Two-Wire Debug mode

Figure 7-6. Two-Wire Debug Mode Entry



7.3.4 On-chip Instrumentation

The OCI unit serves as an interface for On-chip Instrumentation. The OCI provides following functions for communication with On-chip Instrumentation.

- Run/Stop control
- Single Step mode
- Software breakpoint
- Debug program
- Hardware breakpoint
- Program trace
- Access to ACC

7.3.4.1 Enabling OCI Functionality

Enabling the OCI is done by clearing the OCI_OFF bit in the OCI_DEBUG SFR register. By default, OCI is enabled after a device POR.

7.3.4.2 Entering Debug Mode

Debug mode is entered by using the CPU 2-wire Test Mode Entry interface. On entry into Debug mode, the OCI holds the CPU and Watchdog Timer in the Reset state using JReset until the external debugger asserts DebugReq using the `DebugReqOn` JTAG instruction. This allows the debugger to configure the device before the CPU boots-up.

7.3.4.3 Reading the Debug Status

There is no explicit status data register, rather, the status value is shifted out when a new JTAG Instruction Register (IR) value is shifted in.

7.3.4.4 Reading the Program Counter

The current value of the CPU program counter may be read using the `Get PC` JTAG instruction. In PC16 mode, only the least significant 16 bits (PC[15:0]) are valid.

7.3.4.5 Stopping Program Execution (Entering Debug Mode)

To enter Debug mode, the debugger issues the `DebugReqOn` JTAG instruction, which asserts the DebugReq input to the CPU core. Once the CPU enters Debug mode, the DebugAck signal is asserted, which can be determined by reading the Status. DebugAck or Result.DebugAckN register bits.

7.3.4.6 Starting Program Execution (Exiting Debug Mode)

To exit Debug mode, the debugger issues the `DebugReqOff` JTAG instruction, which negates the DebugReq input to the CPU core. Once the CPU exits Debug mode, the DebugAck signal is negated, which can be determined by reading the Status. DebugAck or Result.DebugAckN register bits.

7.3.4.7 User Single Step Mode

User Single Step mode, in which the CPU single steps through the code in Program Memory, is enabled when the debugger issues the `DebugStepUser` JTAG instruction. From Debug mode, the OCI executes one user instruction by pulsing DebugStep active for one clock (or until the first program fetch has completed). The core responds by fetching and executing one instruction, then returning to Debug mode. DebugAck is negated during the step.

7.3.4.8 OCI Single Step Mode

OCI Single Step mode, also known as Programming mode, is used to execute instructions from the debugger, typically for the purposes of programming the device. This mode is enabled when the debugger issues the `DebugStepOCI` JTAG instruction. Each instruction is fed into the CPU by writing it into the result register.

When device programming is being done over the OCI, the `DebugPswrOn` JTAG instruction may be issued to re-direct External Data Writes to Program Memory. The `DebugPswrOff` JTAG instruction may be issued to disable this re-direction. On this device, which presents a unified Program/Data memory, this re-direction is not necessary, as the Program RAM can be written via the external data bus.

7.3.4.9 Setting Software Breakpoints

Software breakpoints may be set by replacing the instruction with a `TRAP` instruction (opcode `0xA5`). Upon execution of the `TRAP` instruction, the core switches to Debug mode and asserts DebugAck. Through the JTAG port, the debugger system periodically polls Status.DebugAck (by issuing the `DebugNOP` JTAG instruction) and begins breakpoint processing when it becomes asserted. For breakpoints in read-only memories, Debug triggers may be used to set hardware breakpoints.

7.3.4.10 Simple and Complex Debug Triggers

The OCI provides a set of hardware breakpoint or trigger registers that monitor bus activity and perform various actions when specified bus events occur. Complex triggers allow a range of addresses to be matched for a trigger rather than a single address, as is the case for a simple trigger.

7.3.4.11 Reading and Writing Memory/SFR Registers

To read from or write to an internal resource, such as a memory or SFR registers, the OCI Single Step mode is used. In this mode, the external debugger can feed in an instruction sequence to perform the requested read/write operation. Read values are placed into the accumulator, which may then be read out of the result register using the `DebugNOP` JTAG instruction.

7.3.4.12 Trace Buffer

The IS2083BM 8051 MCU implements a trace buffer to trace the messages from the OCI to the off-chip debugger.

7.3.4.13 Instruction Trace

The trace buffer memory stores the branches executed by the core. At every change of flow, the most recent PC from the old code sequence and the first PC from the new sequence are stored together as a trace record (frame). Change of flow events include branches, calls, returns, interrupts, and resets.

7.4 General Purpose I/O Pins

The IS2083BM provides up to 19 GPIOs that can be configured by using the Config Tool. The MFB (PWR) pin must be configured as the power On/Off key, and the remaining pins can be configured for any one of the default functions as provided in the following table.

Table 7-4. GPIO Assigned Pins Function(1)

Pin Name	Function Assigned (in Embedded Mode)
P0_0	External codec reset
P0_1	Forward (FWD) button
P0_2	Play or pause (PLAY/PAUSE) button
P0_3	Reverse (REV) button
P0_5	Volume decrease (VOL_DN) button

.....continued	
Pin Name	**Function Assigned (in Embedded Mode)**
P0_6	Available for user configuration
P0_7	Available for user configuration
P1_2	I^2C SCL (muxed with 2-wire CPU debug data)
P1_3	I^2C (muxed with 2-wire CPU debug clock)
P1_6	PWM
P2_3	Available for user configuration
P2_6	Available for user configuration
P2_7	Volume increase (VOL_UP) button
P3_2	Line-In detect
P3_4	SYS_CFG (muxed with UART_RTS)(2)
P3_5	Available for user configuration
P3_7	Available for user configuration
P8_5	UART_TXD(3)(4)
P8_6	UART_RXD(3)(4)

1. This table reflects the default IO assignment as per the Embedded mode. The GPIOs are user configurable by Config Tool.
2. GPIO P3_4 is used to enter Test mode during reset. If the user wants to use this pin to control external peripherals, care must be taken to ensure this pin is not pulled LOW and accidentally enters Test mode.
3. Microchip recommends to reserve UART port (P8_5 and P8_6) for Flash download in Test mode during production.
4. Currently, GPIOs ports P8_5 and P8_6 APIs (button detect driver) are not implemented.

7.5 I^2S Mode Application

The IS2083BM SoC provides one I^2S digital audio I/O interface to connect with an external codec or DSP. It provides 8, 16, 44.1, 48, 88.2 and 96 kHz sampling rates for 16- and 24-bit data formats. The I^2S settings can be configured by the Config Tool. The I^2S pins are as follows:

- SCLK1: Serial/Bit clock (IS2083BM input/output)
- RFS1: Receive frame sync (IS2083BM input/output)
- MCLK: Primary clock (IS2083BM output)
- DR1: Receive data (IS2083BM input)
- DT1: Transmit data (IS2083BM output)

The MCLK is the primary clock output provided to an external I^2S device to use as its system clock. This signal is optional and is not required if the external I^2S device provides its own system clock. This signal is not used with the internal audio codec.

The following figures illustrate the I^2S signal connection between the IS2083BM and an external DSP. The Config Tool can be used to configure the IS2083BM as a host or client.

Note: In this context, the terms “host” and “client” refer to the I^2S clocks and frame syncs, not to the audio data itself.

Figure 7-7. IS2083BM in I²S Host Mode

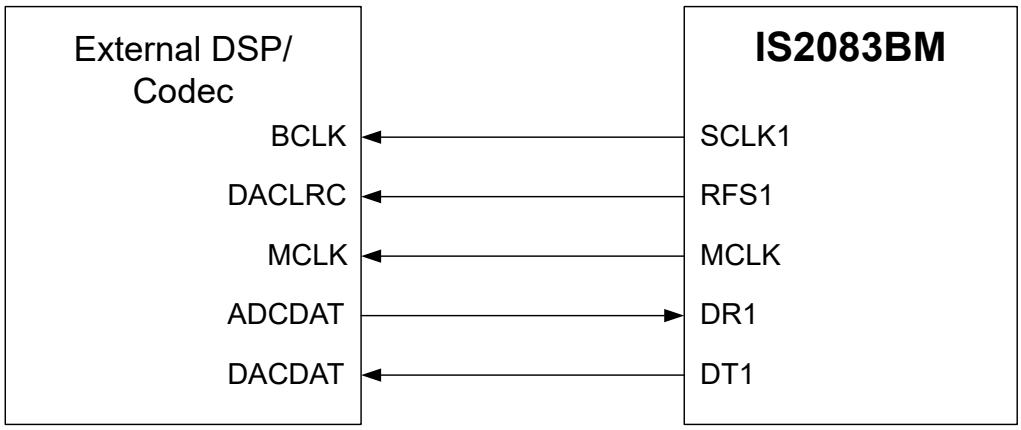
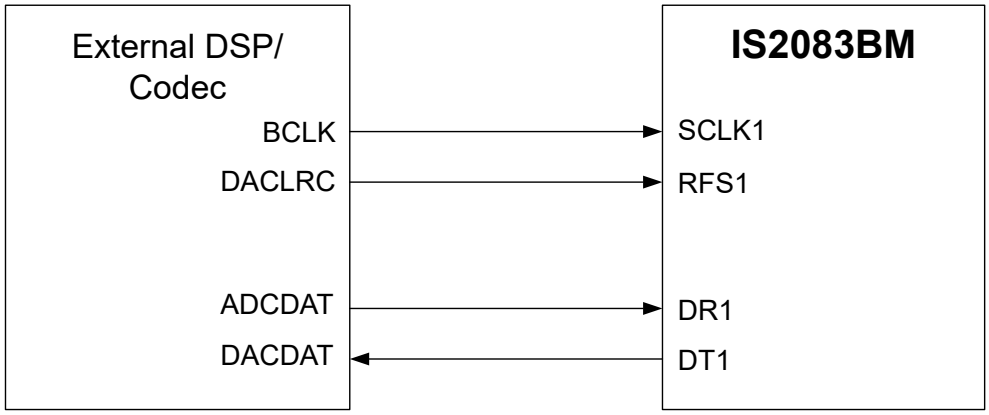


Figure 7-8. IS2083BM in I²S Client Mode



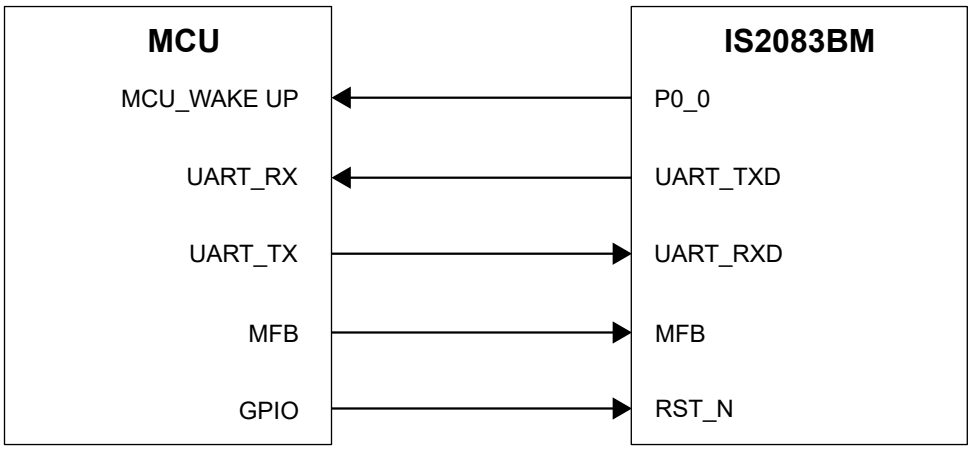
7.6 Host MCU Interface

The IS2083BM multi-speaker firmware supports following modes of operation:

- Embedded mode
  - In this mode, an external microcontroller (MCU) is not required. The multi-speaker (MSPK) firmware is integrated on the IS2083BM to perform application specific controls.
- Host mode:
  - Requires an external MCU for application specific system control. The host MCU can control IS2083BM through UART command set.

The following figure illustrates the UART interface between the IS2083BM and an external MCU.

Figure 7-9. Host MCU Interface Over UART



Note: For more details, refer to the *IS2083 Bluetooth® Audio Application Design Guide Application Note*.

All registers and flip-flops are synchronously Reset by an active-high internal Reset signal. External hardware Reset, or Watchdog Timer Reset can activate the Reset state. A high on RST_N pin or Watchdog Reset request for two clock cycles, while the oscillator is running, resets the device. The falling edge of clock is used for synchronization of the Reset signal. It ensures that all flip-flops are triggered by system clock and gated clocks are properly Reset.

Although a device POR (from the on-chip CLDO) does not explicitly drive the reset tree, but rather causes the assertion of the RST_N pin as follows:

1. POR causes the RST_N pad to drive '0' out.
2. Since the RST_N input buffer is always enabled, during a POR, the ‘0’ propagates to the RST_N input buffer.
3. The RSTGEN modules see the RST_N pin asserted.

8. Electrical Specifications

This section provides an overview of the IS2083BM device's electrical characteristics.

Table 8-1. Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Ambient temperature under bias ($T_{AMBIENT}$)	-40	—	+85	ºC
Storage temperature ($T_{STORAGE}$)	-65	—	+150	ºC
Digital core supply voltage (VDD_CORE)	0	—	1.35	V
RF supply voltage (VCC_RF)	0	—	1.35	V
SAR ADC supply voltage (SAR_VDD)	0	—	2.1	V
Codec supply voltage (VDDA/VDDAO)	0	—	3.3	V
I/O supply voltage (VDD_IO)	0	—	3.6	V
Buck1 and Buck2 supply voltage (BK1_VDD and BK2_VDD)	0	—	4.3	V
Supply voltage (LDO31_VIN)	0	—	4.3	V
Battery input voltage (V_{BAT_IN})	0	—	4.3	V
Adapter input voltage (V_{ADAP_IN})	0	—	7.0	V
Junction operating temperature ($T_{JUNCTION}$)	-40	—	+125	ºC

⚠ CAUTION Stresses listed on the preceding table cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification are not implied. Exposure to maximum rating conditions for extended periods affects device reliability.

The following tables provide the recommended operating conditions and the electrical specifications of the IS2083BM SoC.

Table 8-2. Recommended Operating Condition

Parameter	Min.	Typ.	Max.	Unit
Digital core supply voltage (VDD_CORE)	1.14	1.2	1.26	V
RF supply voltage (VCC_RF)	1.22	1.28	1.34	V
SAR ADC supply voltage (SAR_VDD)	1.62	1.8	1.98	V
Codec supply voltage (VDDA)	1.62	1.8	1.98	V
I/O supply voltage (VDD_IO)	3.0	3.3	3.6	V
Buck1 supply voltage (BK1_VDD)	3.0	3.8	4.25	V
Buck2 supply voltage (BK2_VDD)	3.0	3.8	4.25	V
Supply voltage (LDO31_VIN)	3.0	3.8	4.25	V
Input voltage for battery (V_{BAT_IN})	3.2	3.8	4.2	V
Input voltage for adapter (V_{ADAP_IN}[(1)])	4.5	5	5.5	V
Operation temperature ($T_{OPERATION}$)	-40	+25	+85	ºC

1. ADAP_IN is recommended only for charging the battery in the battery-powered applications.

Table 8-3. Buck1 (RF/Core/ULPC) Switching Regulator(1)

Parameter	Min.	Typ.	Max.	Unit
Input voltage	3.0	3.8	4.25	V
Output voltage (I_{load} = 70 mA and V_{IN} = 4V)	1.4	1.5	1.75	V
Output voltage accuracy	—	±5	—	%
Output voltage adjustable step	—	50	—	mV/Step
Output adjustment range	-0.1	—	+0.25	V
Average load current (I_{load})	120	—	—	mA
Conversion efficiency (V_{BAT_IN} = 3.8V and I_{load} = 50 mA)	—	88 (2)	—	%
Quiescent current (PFM)	—	—	40	µA
Output current (peak)	200	—	—	mA
Shutdown current	—	—	<1	µA

1. These parameters are characterized but not tested on the production device.
2. Test condition: Temperature +25ºC and wired inductor 10 µH.

Table 8-4. Buck2 (Audio Codec) Switching Regulator(1)

Parameter	Min.	Typ.	Max.	Unit
Input voltage	3.0	3.8	4.25	V
Output voltage (I_{load} = 70 mA, V_{IN} = 4V)	1.7	1.8	2.05	V
Output voltage accuracy	—	±5	—	%
Output voltage adjustable step	—	50	—	mV/Step
Output adjustment range	-0.1	—	+0.25	V
Average load current (I_{load})	120	—	—	mA
Conversion efficiency (V_{BAT_IN} = 3.8V, I_{load}= 50 mA)	—	88(2)	—	%
Quiescent current (PFM)	—	—	40	µA
Output current (peak)	200	—	—	mA
Shutdown current	—	—	<1	µA

1. These parameters are characterized but not tested on the production device.
2. Test condition: Temperature +25ºC and wired inductor 10 µH.

Table 8-5. LDO Regulator(1)

Parameter		Min.	Typ.	Max.	Unit
Input voltage		3.0	3.8	4.25	V
Output voltage	LDO31_VO	—	3.3	—	V
Output accuracy (V_{IN}= 3.7V, I_{load}= 100 mA and +27ºC)		—	±5	—	%
Average output current		—	—	100	mA

.....continued				
Parameter	**Min.**	**Typ.**	**Max.**	**Unit**
Drop-out voltage (I_{load} = maximum output current)	—	—	300	mA
Quiescent current (excluding load and I_{load} < 1 mA)	—	45	—	µA
Shutdown current	—	—	<1	µA

1. These parameters are characterized but not tested on production device.
2. Test condition: Temperature +25ºC. The above measurements are done at +25ºC.

Table 8-6. Battery Charger(1)

Parameter		Min.	Typ.	Max.	Unit
Adapter input voltage (V_{ADAP_IN})		4.6(2)	5.0	5.5	V
Supply current (only charger)		—	3	4.5	mA
Maximum battery fast charge current	Headroom(3) > 0.7V (V_{ADAP_IN} = 5V)	—	350	—	mA
	Headroom = 0.3V to 0.7V (V_{ADAP_IN} = 4.5V)	—	175(4)	—	mA
Trickle charge voltage threshold		—	3	—	V
Battery charge termination current (% of fast charge current)		—	10	—	%

1. These parameters are characterized but not tested on production device.
2. It needs more time to get the battery fully charged when ADAP_IN = 4.5V.
3. Headroom = $V_{ADAP\_IN} – V_{BAT\_IN}$.
4. When $V_{ADAP\_IN} – V_{BAT\_IN}$ > 2V, the maximum fast charge current is 175 mA for thermal protection.

Table 8-7. SAR ADC Operating Conditions

Parameter	Condition	Min.	Typ.	Max.	Unit
Shutdown current (I_{OFF})	PDI_ADC = 1	—	—	1	µA
Resolution	—	—	10	—	bits
Effective Number of Bits (ENOB)	—	7	8	—	bits
SAR core clock (F_{CLOCK})	—	—	0.5	1	MHz
Conversion time per channel (T_{CONV})	10 F_{CLOCK} cycles	10	20	—	µs
Offset error (E_{OFFSET})	—	-5	—	+5	%
Gain error (E_{GAIN})	—	—	—	+1	%
ADC SAR core power-up (t_{PU})	PDI_ADC transitions from 1 to 0	—	—	500	ns

.....continued					
Parameter	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Input voltage range (V_{IN})	Channel 8 (SK2 Pin)	0.25	—	1.4	V
	Channel 9 (SK1 Pin)	0.25	—	1.4	V
	Channel 10 (OTP)	0.25	—	1.4	V
	Channel 11 (ADAP_IN Pin)	2.25	—	12.6	V
	Channel 12 (BAT_IN Pin)	1.0	—	5.6	V

Table 8-8. LED Driver(1)

Parameter	Min.	Typ.	Max.	Unit
Open-drain voltage	—	—	3.6	V
Programmable current range	0	—	5.25	mA
Intensity control	—	16	—	step
Current step	—	0.35	—	mA
Power-down open-drain current	—	—	1	µA
Shutdown current	—	—	1	µA

1. These parameters are characterized but not tested on production device.

Table 8-9. Audio Codec Digital-to-Analog Converter

Parameters		Min.	Typ.	Max.	Unit
DC Specifications					
Shutdown mode current		—	—	2	µA
Over-sampling rate		—	128	—	fs
Sample width resolution		16	—	20	Bits
Output sample rate		8	—	48	kHz
Digital gain		-54	—	4.85	dB
Digital gain resolution		2	6	0	dB
Analog gain		-28	—	3	dB
Analog gain resolution		—	1	—	dB
Turn ON/OFF click and pop level	Single-ended	—	—	2	mV
	Capless	—	—	1	mV
Gain pop		—	1	1	mV
Allowed load	Resistive	16	—	—	Ω
	Capacitive	—	—	500	pF
AC Specifications(1)					
SNR – Capless mode	AVDD = 1.8V	93	—	—	dB
SNR – Cap mode	AVDD = 1.8V	95	—	—	dB

.....continued					
Parameters		**Min.**	**Typ.**	**Max.**	**Unit**
Output voltage full-scale swing		495 (1.4)	742.5 (2.1)	—	mV rms (Vpp)
Total harmonic distortion	AVDD = 1.8V	—	-80	—	dB
Inter-channel isolation		–90	–80	—	dB
Dynamic range	Capless and Single-ended	—	95	—	dB
Playback Mode Power					
Stereo mode current (16Ω or unload)	Capless	—	2	—	mA
	Single-ended	—	1.85	—	
Mono mode current (16Ω or unload)	Capless	—	1.55	—	mA
	Single-ended	—	1.40	—	
Maximum output power (AVDD = 1.8V)	Capless	—	14	—	mW
	Single-ended	—	14	—	mW

1. f_{in} = 1 kHz, bandwidth = 20 Hz to 20 kHz, A-weighted, THD+N < 0.01%, 0 dBFS signal, load = 100 kΩ.

Table 8-10. Audio Codec Analog-to-Digital Converter

Parameter (Condition)	**Min.**	**Typ.**	**Max.**	**Unit**
DC Specifications				
Shutdown mode	—	1	2	µA
Sample width resolution	—	—	16	Bits
Input sample rate	8	—	48	kHz
Digital gain	-54	—	4.85	dB
Digital gain resolution	2	6	—	dB
Microphone boost gain	—	20	—	dB
Analog gain step	—	1	—	dB
Input full-scale at maximum gain (Differential)	—	4	—	mV rms
Input full-scale at minimum gain (Differential)	—	800	—	mV rms
3 dB bandwidth	—	20	—	kHz
Microphone mode input impedance (Resistance)	—	6	10	kΩ
Microphone mode input impedance (Capacitance)	—	—	20	pF
AC Specifications(1)				
SNR (AVDD = 1.8V)	88	—	—	dB
Total harmonic distortion (AVDD = 1.8V)	—	-70	—	dB
Dynamic range (AVDD = 1.8V)	—	-88	—	dB
THD+N (microphone input) at 30 mVrms input	—	0.02	—	%
Record Mode Power				

.....continued				
Parameter (Condition)	**Min.**	**Typ.**	**Max.**	**Unit**
Stereo Record mode current	—	1.75	—	mA
Mono Record mode current	—	0.95	—	mA

1. f_{in} = 1 kHz, bandwidth = 20 Hz to 20 kHz, A-weighted, THD+N <1%, 150 mVPP input.

Table 8-11. Transmitter Section Class1 (MPA Configuration) for BDR and EDR(1, 2)

Parameter(3, 4)	Bluetooth Specification	Min.	Typ.	Max.	Unit
Transmit power BDR	0 to 20	10.5	11	11.5	dBm
Transmit power EDR 2M	0 to 20	9	9.5	10	dBm
Transmit power EDR 3M	0 to 20	9	9.5	10	dBm

1. These parameters are characterized but not tested on production device.
2. Test condition: VCC_RF = 1.28V, temperature +25ºC.
3. The RF transmit power is the average power measured for the mid-channel (Channel 39).
4. The RF transmit power is calibrated during production using the MP tool software and MT8852 Bluetooth test equipment.

Table 8-12. Transmitter Section Class2 (LPA Configuration) for BDR and EDR(1, 2)

Parameter(3, 4)	Bluetooth Specification	Min.	Typ.	Max.	Unit
Transmit power BDR	-6 to 4	1.5	2	2.5	dBm
Transmit power EDR 2M	-6 to 4	0	0.5	1	dBm
Transmit power EDR 3M	-6 to 4	0	0.5	1	dBm

1. These parameters are characterized but not tested on production device.
2. Test condition: VCC_RF = 1.28V, temperature +25ºC.
3. The RF transmit power is the average power measured for the mid-channel (Channel 39).
4. The RF transmit power is calibrated during production using the MP tool software and MT8852 Bluetooth test equipment.

Table 8-13. Receiver Section for BDR, EDR, Bluetooth Low Energy(1, 2)

Parameter	Packet Type	Bluetooth Specification	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	GFSK	≤-70	—	-88	—	dBm
Sensitivity at 0.01% BER	π/4 DQPSK	≤-70	—	-90	—	dBm
	8 DPSK	≤-70	—	-84	—	dBm
Sensitivity at 0.1% BER	Bluetooth Low Energy	≤-70	—	-92	—	dBm

1. These parameters are characterized but not tested on production device.
2. Test condition: VCC_RF = 1.28V, temperature +25ºC.

Table 8-14. IS2083BM System Current Consumption(1)

Modes	Condition	Role	Packet Type	Current (Typ.)	Unit
A2DP mode	Internal codec, iOS Central	Peripheral	2DH5/3DH5	12.0576	mA
	Internal codec, Android™ Peripheral	Central	3DH5	12.3218	mA
Sniff mode(2)	Internal codec, Bluetooth Low Energy disabled	Peripheral	DM1	547.232	µA
		Central	2DH1/3DH1	555.7494	µA
	Internal codec, Bluetooth Low Energy enabled	Peripheral	DM1	832.109	µA
		Central	2DH1/3DH1	863.8432	µA
SCO/eSCO connection	Mute at both far end and near end	Peripheral	2EV3	14.1004	mA
		Central	2EV3	13.9436	mA
Inquiry scan	Bluetooth Low Energy disabled	—	—	1.354	mA
	Bluetooth Low Energy enabled	—	—	1.704	mA
Standby mode	System off	Peripheral	—	2.8162	µA
		Central	—	2.855	µA
RF modes(3)	Continuous TX mode	Modulation OFF, PL0		59	mA
		Modulation ON, PL0		30	mA
		Modulation OFF, PL2		35.5	mA
		Modulation ON, PL2		22	mA
	Continuous RX mode	Packet count disable		49	mA
		Packet count enable		38.5	mA

1. Measurement conditions are:
   – V_{BAT_IN} = 3.8V; current measured across BAT_IN
   – Standalone BM83 DVT3 module used for measurements; no LEDs, no speaker load
   – iPhone 6 (iOS v12.2) and OnePlus 6 (Android Oxygen version 9.0.3) used for measurements
   – Current measurements average over a period of 120 secs
   – Distance between DUT (BM83) and Bluetooth source (smartphone) is 30 cms
   – All measurements are taken inside a shield room
2. Internal Codec mode enabled, UART disabled, Auto-Unsniff mode is disabled.
3. RF TX power is set to 10 dBm.

8.1 Timing Specifications

The following figures illustrate the timing diagram of the IS2083BM/BM83 in I^2S and PCM modes.

Figure 8-1. Timing Diagram for I²S Modes (Host/Client)

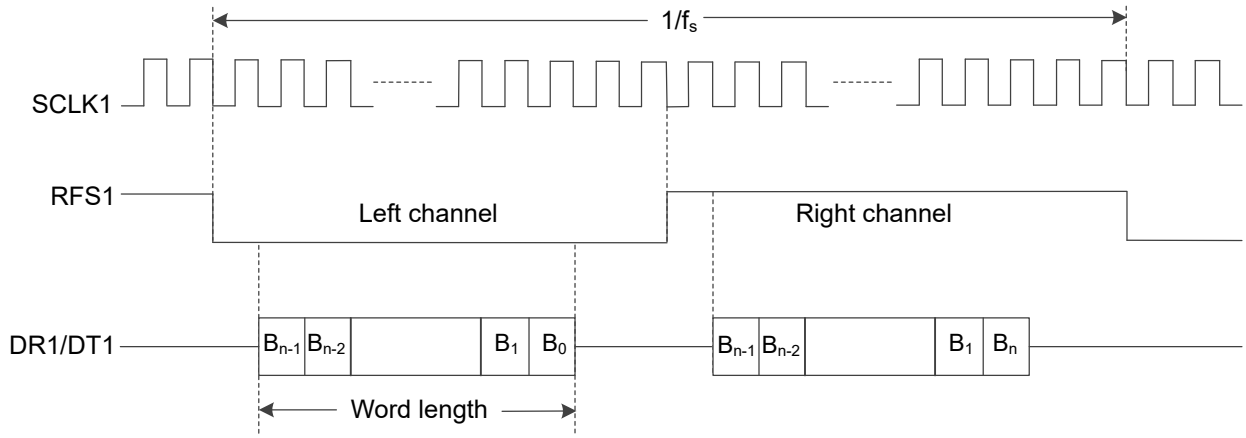
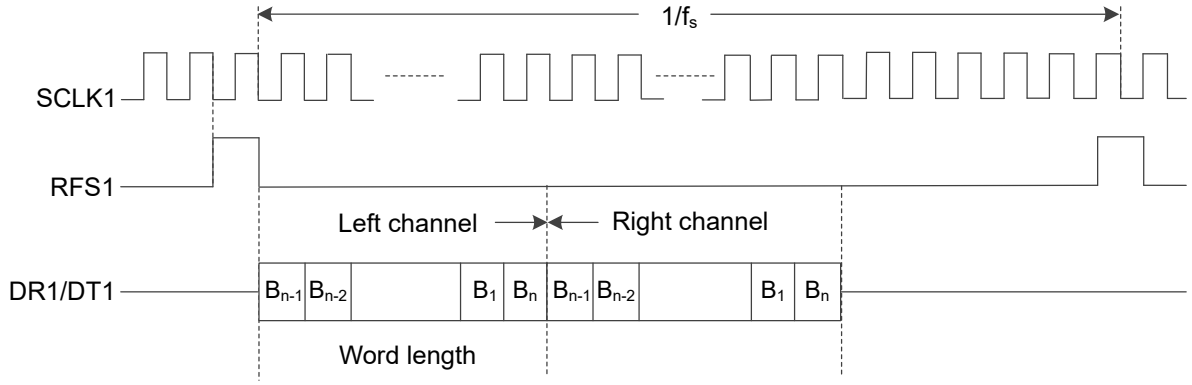
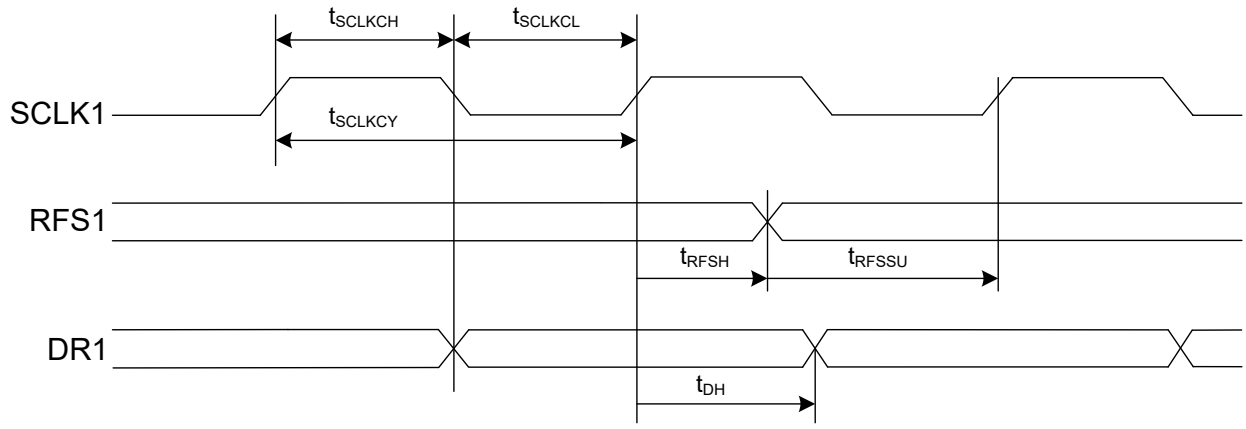


Figure 8-2. Timing Diagram for PCM Modes (Host/Client)



The following figure illustrates the timing diagram of the audio interface.

Figure 8-3. Audio Interface Timing Diagram



The following table provides the timing specifications of the audio interface.

Table 8-15. Audio Interface Timing Specifications(1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK1 duty ratio	d_{SCLK}	—	50	—	%

.....continued					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
SCLK1 cycle time	t_{SCLKCY}	50	—	—	ns
SCLK1 pulse width high	t_{SCLKCH}	20	—	—	ns
SCLK1 pulse width low	t_{SCLKCL}	20	—	—	ns
RFS1 setup time to SCLK1 rising edge	t_{RFSSU}	10	—	—	ns
RFS1 hold time from SCLK1 rising edge	t_{RFSH}	10	—	—	ns
DR1 hold time from SCLK1 rising edge	t_{DH}	10	—	—	ns

1. Test Conditions: Client mode, *f*s = 48 kHz, 24-bit data and SCLK1 period = 256 *f*s

9. Package Information

Note: For the most recent package drawings, see the Microchip Packaging Specification located at www.microchip.com/packaging.

Figure 9-1. 82-Ball Very Thin Fine Pitch Ball Grid Array (3MX) - 5.5x5.5 mm Body [VFBGA]

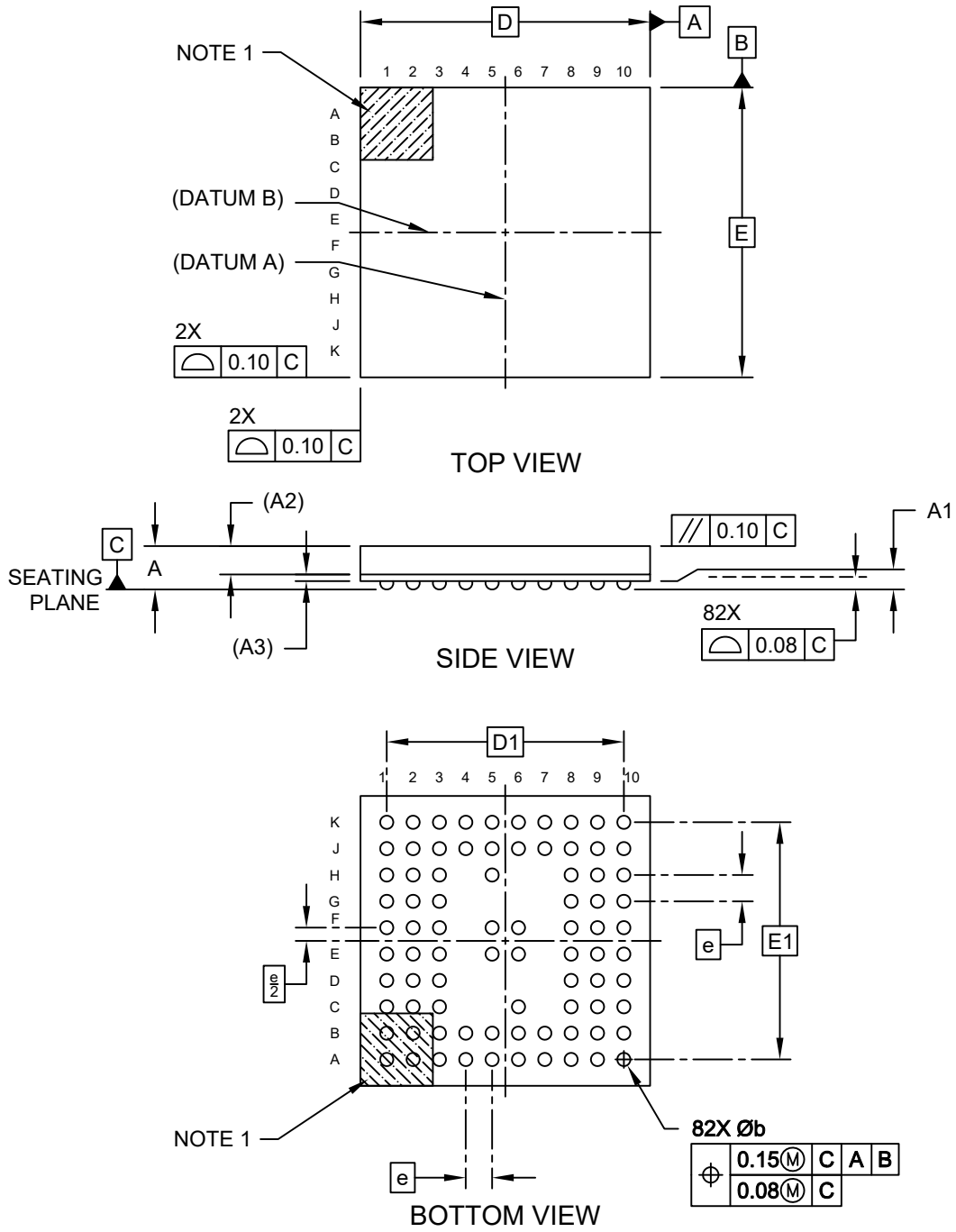
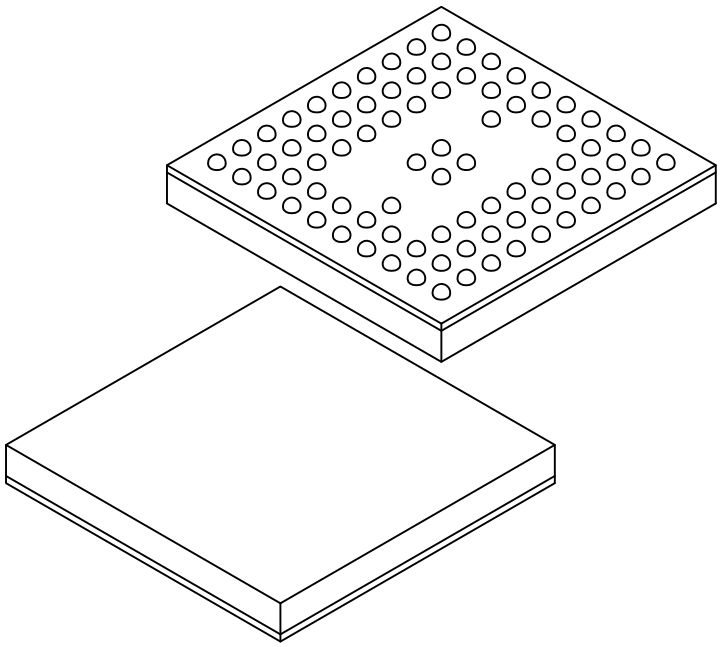


Figure 9-2. 82-Ball Very Thin Fine Pitch Ball Grid Array (3MX) - 5.5x5.5 mm Body [VFBGA]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		82	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	0.90
Standoff	A1	0.11	-	0.21
Mold Thickness	A2		0.54 REF	
Substrate Thickness	A3		0.125 REF	
Overall Length	D		5.50 BSC	
Overall Terminal Spacing	D1		4.50 BSC	
Overall Width	E		5.50 BSC	
Overall Terminal Spacing	E1		4.50 BSC	
Terminal Diameter	b	0.20	0.25	0.30

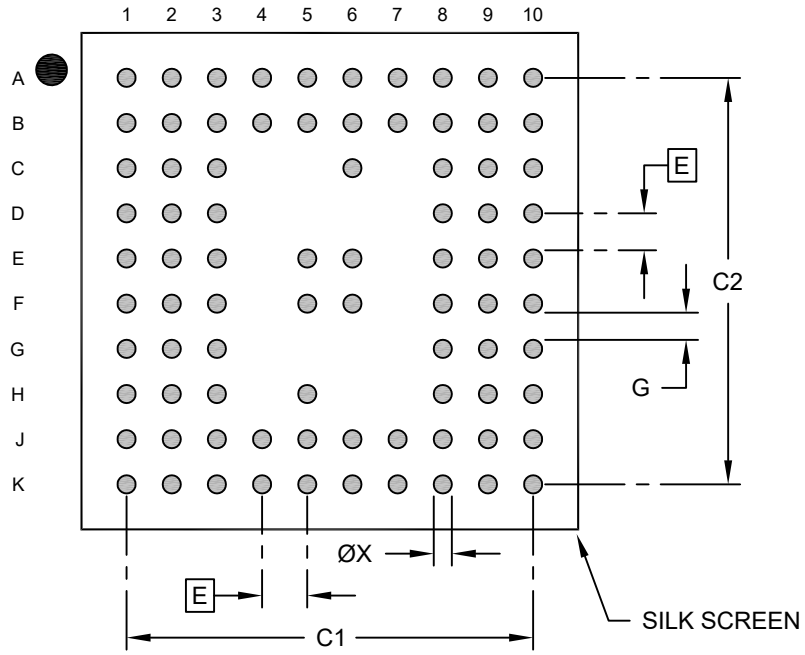
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Figure 9-3. IS2083BM Recommended Land Pattern



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Overall Contact Pad Spacing	C1		4.50	
Overall Contact Pad Spacing	C2		4.50	
Contact Pad Width (X82)	X			0.20
Contact Pad to Contact Pad	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Figure 9-4. IS2083BM Package Marking Information

XXX: Chip serial number version and (e1) Pb-free JEDEC designator for SAC305

YY: Year code (last 2 digits of calendar year)
WW: Week code (week of January 1 is week "01")
NNN: Alphanumeric traceability code

Note:
(1) SAC305 is the pre-solder version. Customer needs to take care solder paste before screen printing.

10. Ordering Information

Table 10-1. Ordering Information

Device	Description	Package Details	Part Number	Packing Media
IS2083BM	Bluetooth Audio Dual mode Flash SoC, 2 microphones, 1 stereo digital microphone, analog and I^2S output	5.5 mm X 5.5 mm X 0.9 mm, 82 LD VFBGA	IS2083BM-232	Tape and reel
			IS2083BM-232-TRAY	Tray
	Bluetooth Audio Dual mode, Flash SoC, 2 microphones, 1 stereo digital microphone, LDAC support and I^2S output	5.5 mm X 5.5 mm X 0.9 mm, 82 LD VFBGA	IS2083BM-2L2	Tape and reel
			IS2083BM-2L2-TRAY	Tray

11. Document Revision History

Revision	Date	Section	Description
D	10/2021	Document	Updated with new terminologies. For more details, see the following note.
		7.3.1 Test Mode Programming	Updated the Test mode information
		10. Ordering Information	Updated with new Part Number and Packaging Media details
		Features	Updated HFP version and other minor edits, and added compliance information
		7.3 Programming and Debugging	Updated the contents.
		7.3.2 Two-Wire JTAG Debug Interface	Updated the contents.
		7.3.3 Enabling Debugging Interface	Updated the contents.
C	06/2020	Document	Minor edits
		Introduction	Updated with minor edits
		Features	Added MSPK and AT solution
		6.7 Battery Charging	Updated Figure 6-2
		3.4 Microphone Inputs	Updated the Note related to PDM Digital Microphone
B	09/2019	Document	Minor edits
		6.1 Device Operation	Updated Figure 6-1
		6.7 Battery Charging	Updated Figure 6-2
		6.8 SAR ADC	• Changed the section title to SAR ADC from Battery Voltage Monitoring and combined Ambient Temperature Detection Section. • Updated contents.
		7. Application Information	• Reorganized sections in this chapter. • Added 7.1 Power On/Off Sequence section. • Updated 7.2 Reset section. • Updated 7.4 General Purpose I/O Pins.
		8. Electrical Specifications	Added Table 8-7
A	07/2019	Document	Initial Revision

Note: *Microchip is aware that some terminologies used in the technical documents and existing software codes of this product are outdated and unsuitable. This document may use these new terminologies, which may or may not reflect on the source codes, software GUIs, and the documents referenced within this document. The following table shows the relevant terminology changes made in this document.*

Table 11-1. Terminology Related Changes

Old Terminology	New Terminology	Description
Master	Central	The following section and table is updated with these terminologies: • Features • Table 8-14
Host	Peripheral	
Master	Host	The following sections are updated with these terminologies: • Features • 7.5 I2S Mode Application
Host	Client	
Master clock	Primary clock	The following sections are updated with these terminologies: • Features • 1.2 Acronyms/Abbreviations • 2.2 IS2083BM Device Ball Description

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